Effective Utilization of Battery Banks in Multi-level Inverters for a Residential Photovoltaic Applications

MEHER KALYAN UPPALURI

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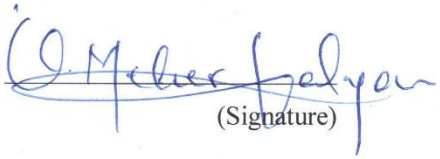

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MEHER KALYAN U

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Approval Sheet

This thesis entitled Effective Utilization of Battery Banks in Multilevel inverters for a Residential Photovoltaic Applications by Meher Kalyan Uppaluri is approved for the degree of Master of Technology from IIT Hyderabad.

R. Prasantha Kumar

-Name and affiliation-

Examiner

-Name and affiliation-

Ketan IITH.

Examiner

K. SIVAKUMAR. IITH.

-Name and affiliation-

Adviser

-Name and affiliation-

Co-Adviser

R. Prasantha Kumar

-Name and affiliation-

Chairman

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Dedicated to

To Almighty and my parents

List of Tables

List of Figures

Abstract

Distributed generation is key to improve reliability, reduced emission and improve power quality. In spite of high initial cost PV is forefront in renewable energy generation. For a residential PV installed application complete utilization of battery banks is key to reduce grid dependency and improve reliability. The present work introduces a novel methodology which leads to reduce the grid dependency and improve reliability for customer by making effective use of battery banks. In order to achieve above objective it's important to keep battery banks difference or state of charges with in a threshold limit. This objective is attained by switching/shifting isolated panels. Selection of isolated panels through optimization by considering irregularity of roof top and worst case conditions. In addition, a control strategy is developed for switching isolated panels depending on difference in discharge levels. In addition, to decrease grid reliance and improve reliability a switching pattern is developed for a household installed PV system considering generation and load pattern. The present work is verified in MATLAB/Simulink environment.

Nomenclature

I_{sat} PV cell reverse saturation current

I_{sa} Module output current

V_{sa} Module output voltage

k_0 AKT/q

A Ideality factor of diode

K Boltzmann's constant (=1.3805 X 10^{-23} N-m/K)

q Charge of electron (= 1.6 X 10^{-19} C)

R_s Series resistance

R_{sh} Shunt resistance

Tr Reference Temperature = 298K

T Module operating temperature in kelvin

k Boltzmann constant = 1.3805 X 10^{-23} J/K

q Charge of electron = 1.6 X 10^{-19} C

B Diode ideality factor

G Irradiation in W/m^2

Ki Short circuit temperature coefficient

Eg_0 Band gap for silicon

Contents

Chapter 1

Introduction

It is become increasingly difficult to meet energy needs through traditional generation. To meet ever increasing demand distributed generation is answer. Renewables are clean source of energy. Among the all renewable solar is abundant. As solar energy reduces reliance on non-renewable sources of energy and reduce in greenhouse gas emissions eventually contribute to energy security. With the increasing per unit price of grid, solar power can be on par with traditional coal fuels [1]. The cost of solar energy is now truly competitive with traditional coal fired electricity and expected to achieve grid parity by 2020 i.e, supplying solar electricity at levelised cost to the price of grid [1]. Many nations have pledged to reduce the emissions of greenhouse gas and to produce no less than 20% of its energy consumption from renewable sources by 2020 [1]. In this context, photovoltaic (PV) power generation has an important role to play due to the fact that it is a green source. The only emissions associated with PV power generation are those from the production of its components. After their installation they generate electricity from the solar irradiation without emitting greenhouse gases. Also they can be installed in places with no other use, such as roofs and deserts, or they can produce electricity for remote locations, where there is no electricity network. The latter type of installations is known as off-grid facilities and sometimes they are the most economical alternative to provide electricity in isolated areas. Solar energy can offer an economically viable means of providing connections to un-electrified areas. Some of the renewable energy technologies that are used in rural areas as decentralized systems are Solar street lighting systems, Solar lanterns and solar home lighting systems, Solar water heating systems, Solar cookers.

India being located in equatorial belt, clear sun is expected 250 to 350 days a year in most parts. The total irradiant energy varies from 1600 to 2200 kWh/m^2 [2]. Implying a potential of 6000 million GWh of energy per year [2]. The Ministry of New and Renewable Energy has planned to install 10 GW utility scale solar projects and 1 GW off-grid solar power projects by the end of 2017 [3].

1.1 Types of Solar Cells

In the last few decades, silicon is mostly used material for manufacturing solar cells. Almost 90% photovoltaic's today based on some variation of silicon [4]-[5]. Many other materials have been developed but silicon stands apart because of many advantages. The domination of silicon is because of its most abundant material on the earth in form of silicon oxide. Efficiency of solar cell depends on purity of silicon used. Processes to improve the silicon efficiency are much expensive. Trade-off between cost and efficiency of solar cell makes efficiency not a primary concern. Efficiency of solar cell i.e. how much percent of incident radiation is converted to electricity is determined under STC (Standard test conditions). The standard test conditions for determining efficiency are 1000 W/m^2, cell temperature is 25^0C and air mass A.M1.5 [6] (air mass). Higher the efficiency lower is the material required to give same power.

Crystalline silicon forms the basis of mono- and polycrystalline silicon solar cells. Mono and polycrystalline are major sources of solar cells/panels production today. In addition Thin-flim solar cells (TFSC's) and Amorphous Silicon (a-Si) Solar cells are also there [5]. In this section advantages and disadvantages of above mentioned solar cells are discussed below.

1.1.1 Monocrystalline silicon:

Monocrystalline solar cells are made out of silicon ingots, which are cylindrical in shape. To optimize performance and lower costs of a single monocrystalline solar cell, four sides are cut out of the cylindrical ingots to make silicon wafers, this gives monocrystalline solar panels their characteristic look. Fig. 1 showing a mono crystalline PV panel.

Fig 1: A mono crystalline solar panel

A good way to separate mono- and polycrystalline solar panels is that polycrystalline solar cells look perfectly rectangular with no rounded edges [5].

Advantages

- Monocrystalline solar panels have the highest efficiency rates since they are made out of the highest-grade silicon. The efficiency rates of monocrystalline solar panels are typically 15-20%.
- Monocrystalline silicon solar panels are space-efficient. Since these solar panels yield the highest power outputs, they also require the least amount of space compared to any other types. Monocrystalline solar panels produce up to four times the amount of electricity as thin-film solar panels.
- Monocrystalline solar panels live the longest. Most solar panel manufacturers put a 25-year warranty on their monocrystalline solar panels.
- Tend to perform better than similarly rated polycrystalline solar panels at low-light conditions.

Disadvantages

- Monocrystalline solar panels are the most expensive. From a financial standpoint, a solar panel that is made of polycrystalline silicon (and in some cases thin-film) can be a better choice for some home applications.
- If the solar panel is partially covered with shade, dirt or snow, the entire circuit can break down. Consider getting micro-inverters instead of central string inverters will be a problem. Micro-inverters will make sure that not the entire solar array is affected by shading issues with only one of the solar panels.
- The Czochralski process is used to produce monocrystalline silicon. It results in large cylindrical ingots. Four sides are cut out of the ingots to make silicon wafers. A significant amount of the original silicon ends up as waste.
- Monocrystalline solar panels tend to be more efficient in warm weather. Performance suffers as temperature goes up, but less than polycrystalline solar panels. For most, temperature is not a concern.

1.1.2 Polycrystalline silicon

The first solar panels based on polycrystalline silicon, which also is also known as multi-crystalline silicon (mc-Si) introduced to the market in 1981. Unlike monocrystalline-based solar panels, polycrystalline solar panels do not require the Czochralski process. Raw silicon

is melted and poured into a square mold, which is cooled and cut into perfectly square wafers [5]. Fig. 2 showing a polycrystalline PV panel.

Fig 2: A Polycrystalline solar panel

Advantages

- The process used to make polycrystalline silicon is simpler and cost less. The amount of waste silicon is less compared to monocrystalline.
- Polycrystalline solar panels tend to have slightly lower heat tolerance than monocrystalline solar panels. This technically means that they perform slightly worse than monocrystalline solar panels in high temperatures. Heat can affect the performance of solar panels and shorten their lifespans. However, this effect is minor, and most homeowners do not need to take it into account.

Disadvantages

- The efficiency of polycrystalline-based solar panels is typically 13-16%. Because of lower silicon purity, polycrystalline solar panels are not quite as efficient as monocrystalline solar panels.
- Lower space-efficiency. It is generally need to cover a larger surface to output the same electrical power as compared to solar panel made of monocrystalline silicon.

- Monocrystalline and thin-film solar panels tend to be more aesthetically pleasing since they have a more uniform look compared to the speckled blue color of polycrystalline silicon.

1.1.3 Thin-Flim Solar cells (TFSC)

Depositing one or several thin layers of photovoltaic material onto a substrate is the basic gist of how thin-film solar cells are manufactured. They are also known as thin-film photovoltaic cells (TFPV). The different types of thin-film solar cells can be categorized by which photovoltaic material is deposited onto the substrate:

- Amorphous silicon (a-Si)
- Cadmium telluride (CdTe)
- Copper indium gallium selenide (CIS/CIGS)
- Organic photovoltaic cells (OPC)

Depending on the technology, thin-film module prototypes have reached efficiencies between 7–13% and production modules operate at about 9%. Future module efficiencies are expected to climb close to the about 10–16%.

Advantages

- Mass-production is simple. This makes them and potentially cheaper to manufacture than crystalline-based solar cells.
- Their homogenous appearance makes them look more appealing.
- Can be made flexible, which opens up many new potential applications.
- High temperatures and shading have less impact on solar panel performance.
- In situations where space is not an issue, thin-film solar panels can make sense.

Disadvantages

- Thin-film solar panels are in general not very useful in most residential applications. In spite of being economical they occupy more space compared to crystalline solar panels. Monocrystalline solar panels produce up to four times the amount of electricity as thin-film solar panels for the same amount of space.
- Low space-efficiency also means that the costs of PV-installation will increase.
- Thin-film solar panels tend to degrade faster than mono- and polycrystalline solar panels, which is why they typically come with a shorter warranty.

Solar panels based on amorphous silicon, cadmium telluride and copper indium gallium selenide are currently the only thin-film technologies that are commercially available in the market.

1.1.4 Amorphous Silicon (a-Si) Solar cells

Because of the low output electrical power, solar cells based on amorphous silicon have traditionally used for small-scale applications such as in pocket calculators. However, recent innovations have made them more attractive for some large-scale applications too.

With a manufacturing technique called "stacking", several layers of amorphous silicon solar cells can be combined, which results in higher efficiency rates (typically around 6-8%). Only 1% of the silicon used in crystalline silicon solar cells is required in amorphous silicon solar cells. On the other hand, stacking is expensive [5].

1.1.5 Cadmium Telluride (CdTe) Solar Cells

Cadmium telluride is the only thin-film solar panel technology that has surpassed the cost-efficiency of crystalline silicon solar panels in a significant portion of the market (multi-kilowatt systems).The efficiency of solar panels based on cadmium telluride usually operates in the range 9-11%.

1.1.6 Copper Indium Galnium Selenide (CIS/CIGS) Solar cells

Compared to the other thin-film technologies above, CIGS solar cells have showed the most potential in terms of efficiency. These solar cells contain less amounts of the toxic material cadmium that is found in CdTe solar cells. Commercial production of flexible CIGS solar panels was started in Germany in 2011.The efficiency rates for CIGS solar panels typically operate in the range 10-12 %. Many thin-film solar cell types are still early in the research and testing stages. Some of them have enormous potential, and we will likely see more of them.

1.2 Selection of Solar for Residential application

Price per unit is less incase of Thinflim Solar cells but occupies more space i.e. less efficient cheap panels. In case if space constrain is there crystalline solar cells are preferred. Both mono- and polycrystalline solar panels are good choices and offer similar advantages. Monocrystalline solar panels are slightly more expensive, but also slightly more space-efficient. If you had one polycrystalline and one monocrystalline solar panel, both rated 220-watt, they would generate the same amount of electricity, but the one made of monocrystalline

Silicon would take up less space but higher cost.

1.3 Photovoltaic Array Mathematical Modeling

Solar cells are the basic components of photovoltaic panels. Most are made from silicon even though other materials are also used. Solar cell is basically a p-n junction fabricated in a thin wafer of semiconductor. Solar cells take advantage of the photoelectric effect. The electromagnetic radiation of solar energy can be directly converted to electricity through photovoltaic effect. Being exposed to the sunlight, photons with energy greater than the band-gap energy of the semiconductor creates some electron-hole pairs proportional to the incident irradiation. The current source I_s represents the cell photocurrent. R_p and R_s are the intrinsic shunt and series resistances of the cell, respectively. Usually the value of R_p is very large and that of R_s is very small, hence they may be neglected to simplify the analysis. A single diode model of solar cell is as show in fig. 3.

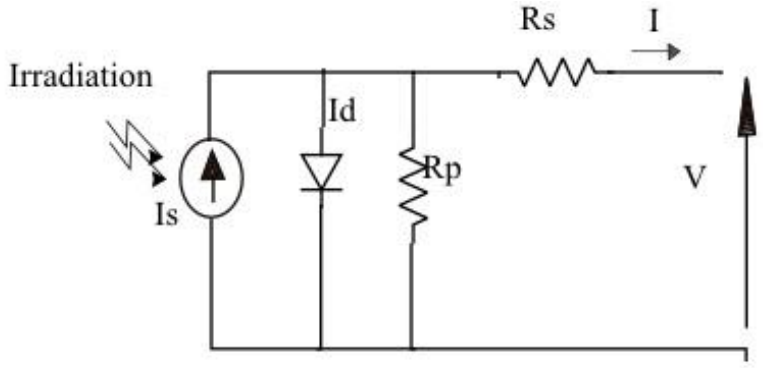

Fig 3: A single diode model of Solar cell

A single diode modeling of PV module as shown in fig. 4 with Np and Ns number of parallel, series of PV cells respectively [7]-[8].The equations governing the output current of PV module with Ns number of series connected PV cells and Np number of PV cells connected in parallel is shown in equations (1)-(4) [17].

PV Module output current:

$$I_{sa} = N_p I_{ph} - N_p I_{sat}\left\{\exp\left(\frac{V_{sa}}{N_s K_o} + \frac{I_{sa} R_s}{N_p K_0}\right) - 1\right\} - \frac{1}{R_{sh}}\left(\frac{V_{sa}}{N_s} + \frac{I_{sa} R_s}{N_p}\right) \qquad (1)$$

I_{ph} is output current of each PV cell

$$I_{ph} = [I_{scr} + K_i(T - 298)] * \frac{G}{1000} \quad (2)$$

$$I_{rs} = \frac{I_{scr}}{[\exp\left(\frac{qV_{oc}}{N_s kAT}\right) - 1]} \quad (3)$$

$$I_{sat} = I_{rs}\left[\frac{T}{T_r}\right]^3 \left[\exp\frac{qEg0}{Bk}\left\{\frac{1}{T} - \frac{1}{T_r}\right\}\right] \quad (4)$$

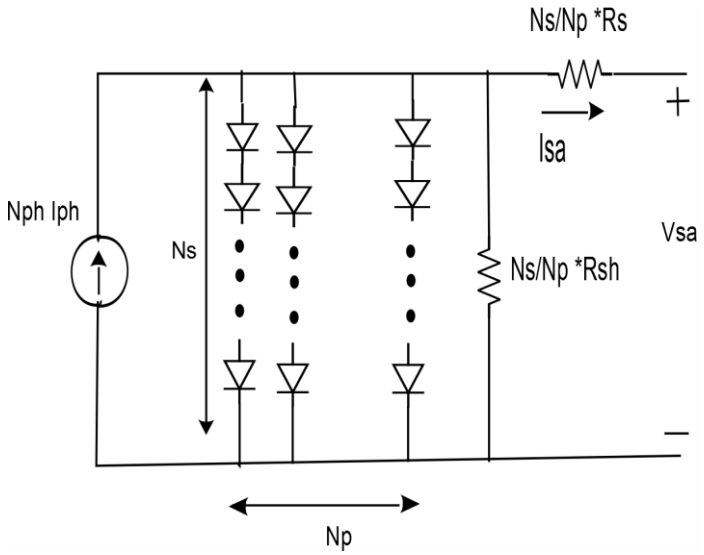

fig 4: Single diode model of PV array

P versus V and I versus V for different irradiations are shown in figures 5(a) and 5(b) respectively.

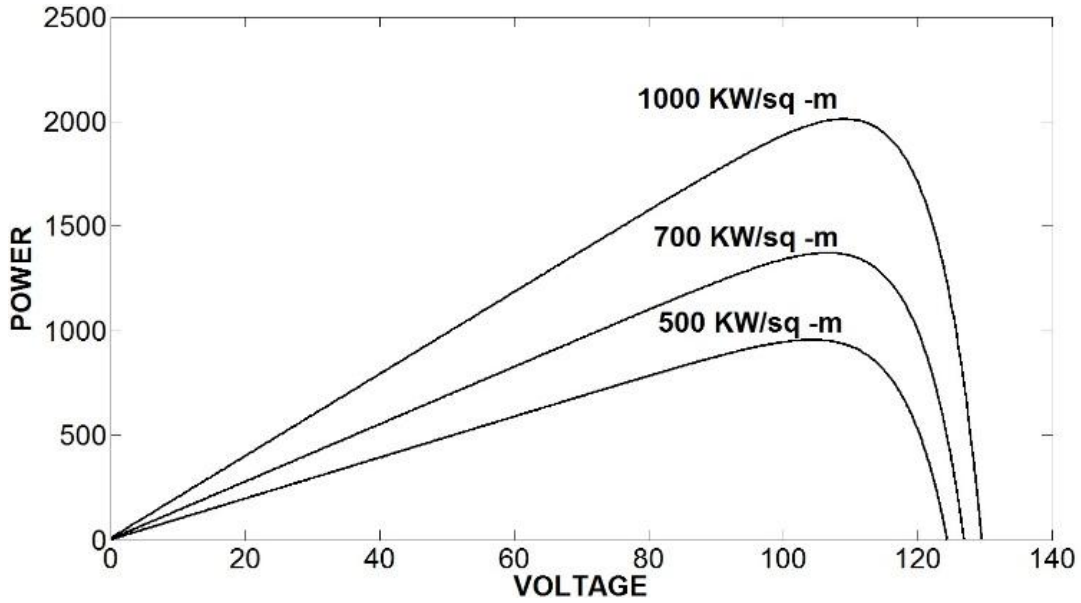

Fig 5(a): P Vs V Under different irradiations

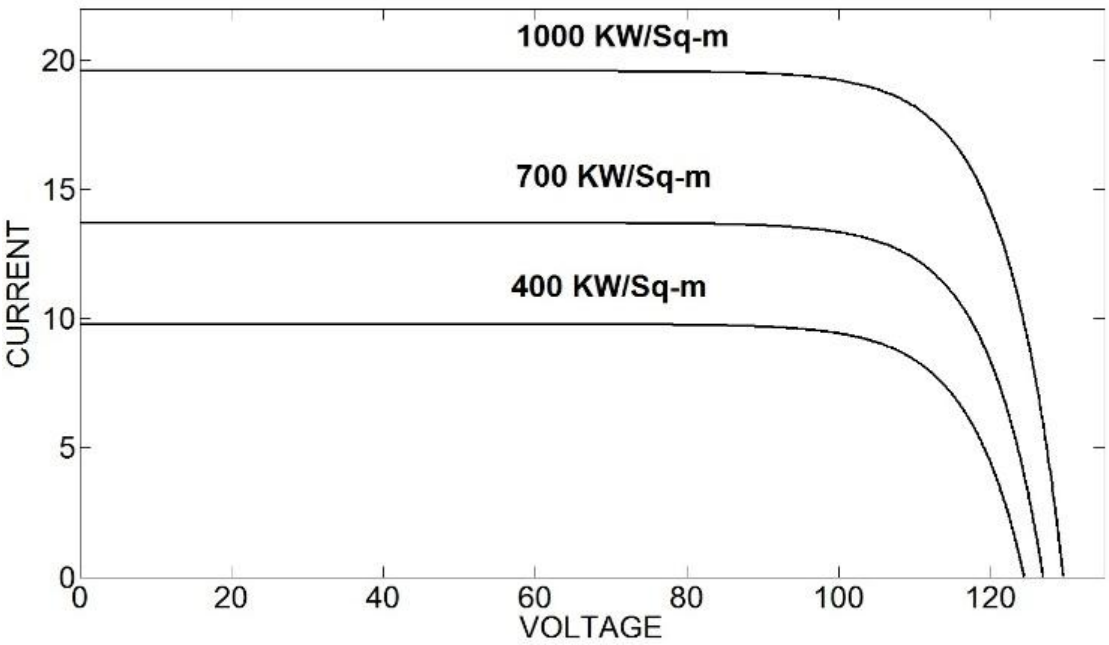

Fig 5(b): I Vs V Under different irradiations

1.4 Maximum Power Point Tracking

As mentioned before, the temperature and the irradiation depend on the atmospheric conditions, which are not constant during the year and not even during a single day; they can vary rapidly due to fast changing conditions such as clouds. This causes the MPP to move constantly, depending on the irradiation and temperature conditions. If the operating point is not close to the MPP, more power losses occur. Hence it is essential to track the MPP in any

conditions to assure that the maximum available power is obtained from the PV panel. In a modern solar power converter, this task is entrusted to the MPPT algorithms.

Over the past decades many methods to have been developed to find the MPP were published. These techniques differ in many aspects such as in terms of required sensors, complexity, cost, range of effectiveness, convergence speed, correct tracking when irradiation and/or temperature change, hardware needed for the implementation or popularity, among others. A complete review of 19 different MPPT algorithms can be found in [9].

Among these techniques, the P&O and the InCond algorithms are the most common. These techniques have the advantage of an easy implementation but they also have drawbacks, as will be shown later. Other techniques based on different principles are fuzzy logic control, neural network, fractional open circuit voltage or short circuit current, current sweep, etc. Most of these methods yield a local maximum and some, like the fractional open circuit voltage or short circuit current, give an approximated MPP, not the exact one. In normal conditions the V-P curve has only one maximum, so it is not a problem. However, if the PV array is partially shaded, there are multiple maxima in these curves.

1.4.1 Perturb and observe

The P&O algorithm is also called "hill-climbing", but both names refer to the same algorithm depending on how it is implemented. Hill-climbing involves a perturbation on the duty cycle of the power converter and P&O a perturbation in the operating voltage of the DC link between the PV array and the power converter. In case of the Hill-climbing, perturbing the duty cycle of the power converter implies modifying the voltage of the DC link between the PV array and the power converter, so both names refer to the same technique. From Fig.7(a), it can be seen that, incrementing (decrementing) the voltage increases (decreases) the power when operating on the left of the MPP and decreases (increases) the power when on the right of the MPP. Therefore, if there is an increase in power, the subsequent perturbation should be kept the same to reach the MPP and if there is a decrease in power, the perturbation should be reversed. In this method, the sign of the last perturbation and the sign of the last increment in the power are used to decide what the next perturbation should be. If there is an increment in the power, the perturbation should be kept in the same direction and if the power decreases, if not then the next perturbation should be in the opposite direction. Based on these facts, the algorithm is implemented [9]. The process is repeated until the MPP is reached. Then the operating point oscillates around the MPP. This problem is common also to the InCond

method. A scheme of the algorithm is shown in Fig 6. The tracking of different maximum power under different irradiations are shown in fig 7.

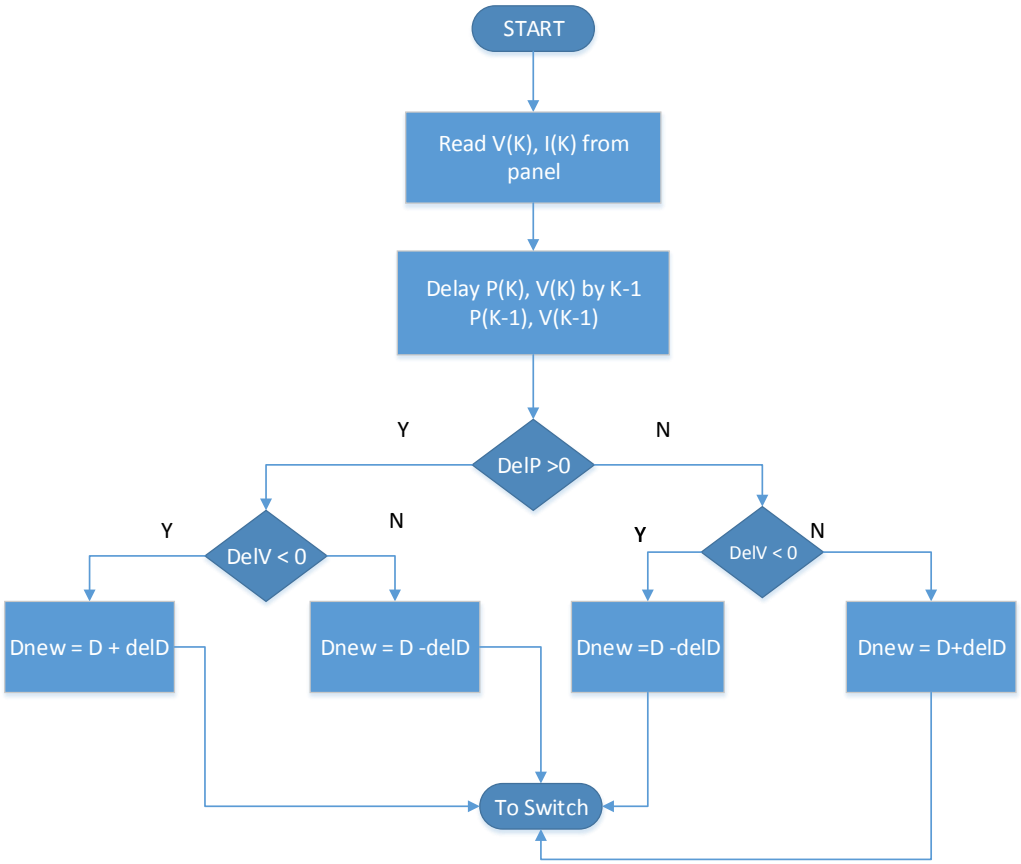

Fig 6: Algorithm for Perturb and Observe Method

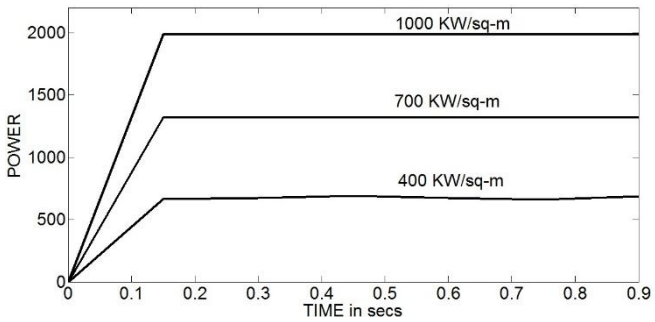

Fig 7: Maximum power point tracking under different irradiations

1.5 Effects of Partial Shading

Non-uniform partial shading has effects like hot spots which cause permanent damage to PV panel [10]. Apart from that there is drastic decrease in output of PV panel. Shading may be due

to reasons like adjacent buildings, clouds, shading of one panel on others etc. Since there's a decrease in output, which results battery banks to start/more discharge to meet load. The below fig 12 shows two isolated PV array's (single PV array is divided into two) supplying to three-level cascaded inverter along with two battery banks.

One of the main reasons for partial shading is due to shading of one panel on other in early and late hours. So it is crucial to have critical clearance between the panels to be free from shading. Clearance distance between panels varies from location to location because angle at which panel is mounted depends on latitude at which they are installed [11]-[12]. For instance in geometric location 17.36^{o} N, 78.47^{o} the optimum angle for panel is 17.3 degrees.

Shading due to clouds can't be determined as it varies from time to time but shading of one panel on other can be determined if one knows latitude and longitude information. With given coordinates, one can determine max shadow cast by an object with sun's latitude and azimuth angle as given by the following formulae's [13]-[15]

Solar Elevation angle:

$\alpha=\sin^{-1}[\sin\delta*\sin\varphi+\cos\delta*\cos\varphi*\cos(HRA)]$ [wiki]

Where α_s is the solar elevation angle

HRA is the hour angle

δ is the current declination of sun

φ is the local latitude

Solar Azimuth angle

Øs = acos[(sinδ*cos φ –cos δ * sin φ * cos(HRA))/cos α] [wiki]

Øs is the solar azimuth angle

A shadow cast by an object depends on the angle at which it is inclined. Since we are trying to measure the shadow of one PV panel on other we need to find at what angle PV panel is inclined. Generally there are two types of mounting of panel's one is fixed and another is changing angle for tracking the sun's position using a micro-controller .The later one need much clearance between the panels cause as they are changing position continuously also needs timely maintenance and it is not economical. Later one where panels are fixed at certain

angle for optimum illumination throughout the year, panels are inclined at altitude angle (location at which the panels are installed) facing towards south. To decide spacing between the panels, we need to take max shadow which occurs on winter solstice mostly on December 21st (in which sun is at minimum altitude)

H_{res} = H * sin (angle of panel)

Where H is the height of panel

Hres is the resultant height of panel

Therefore,

Shadow length= h*tan(angle at elevation of sun)

* Orientation of shadow depends on azimuth angle
* If they are place at certain height using a support then one can calculate the Shadow according to that

If you take generation starts at 8:00 AM according to data at 8 :00 AM in hyderabad on Dec 18 Shadow length would be 3.501 times the height of object

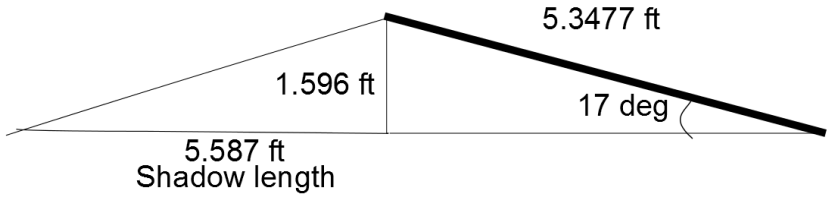

Fig 8: Shadow cast by 5.3477 feet panel at 8:00 AM on Dec 18, 2013

Fig 8 shows shadow cast by panel on December 18 is 5.587ft. Since it's not economical to leave the 5.587 ft between the panels there is definitely effect of one panel shadow on other as shown in fig 9. In Urban scenario where with constrains like minimum space, high demand one can't leave high space between the panels to clear the shadow . Therefore, trade-off between the loss, spacing, angle of inclination is necessary as shown in fig 9.

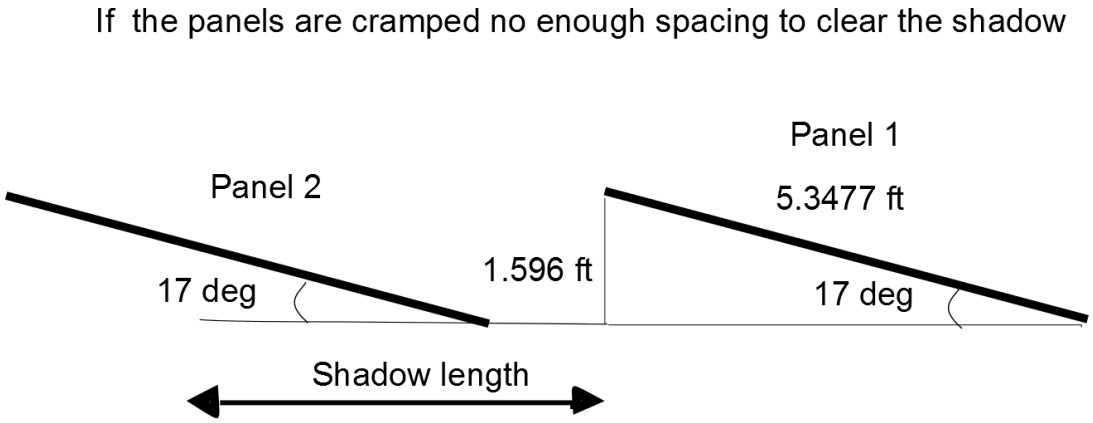

Fig 9: Effect of One panel on other

As discussed previously, uneven partial shading on PV array (each array taken as single unit) results in different SOC's of NPC batteries .One of the case of uneven partial shading of array due to shadow of one panel on other panel can be irregular roof tops as shown in fig. 10(a), 10(b), 10(c).

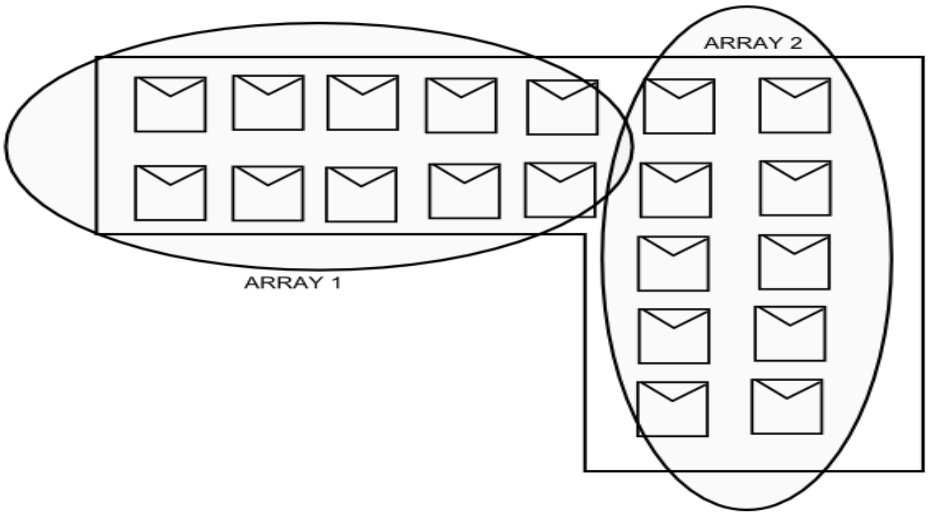

Fig 10(a): One of probable case of uneven partial shading

As we can see shadow of Array-1 is not equal to Array-2 because in Array-1 five panels are subjected to partial shading unlike Array-2 where eight panels are subjected to shading .As we know difference in shading results in difference in SOC's of batteries. Here battery-2 is more discharging than battery-1.

Uneven Partial Shading can occur in case Gabel and Hipped roof PV applications

Fig 10(b): Gabble Roof top

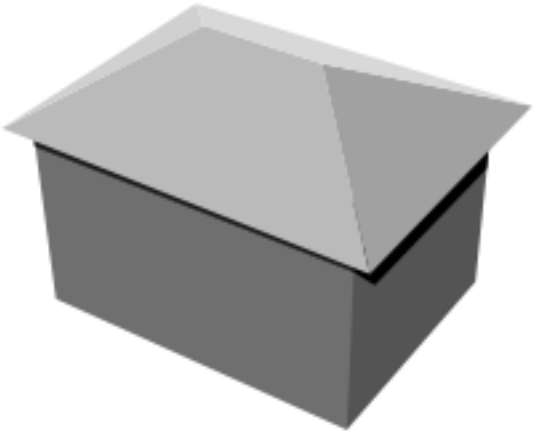

Fig 10(c): Hipped roof Top

Chapter 2

Multi-level Inverters for Photo-Voltaic applications

2.1 Conventional Implementation

A conventional way of extracting solar energy is a two stage conversion to supply grid or consumer [16]. First stage is DC-DC conversion and followed by DC-AC as shown in fig.11

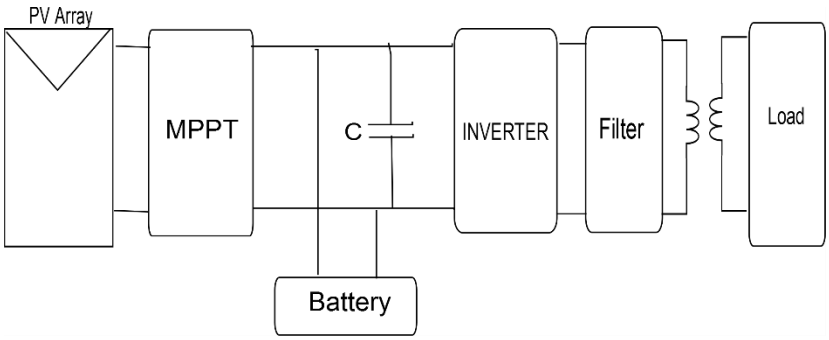

Fig 11: Two stage extraction of solar energy

To implement above modelling of PV array, a MPPT algorithm, battery and converter is needed. A detailed mathematical Modeling of PV array is discussed in [7]-[8] by considering various factors like reverse saturation current, irradiance and temperature. As generation of solar power is in DC, a two-stage conversion is employed to supply consumer or grid. First stage is extracting maximum power from solar which can be attained by MPPT. In [9] many MPPT configurations were shown starting from OC, SC methods, hill climbing, incremental conductance methods, algorithms based on ANN and fuzzy logic. Second stage is conversion of DC to AC. Multi-level inverters have advantage of low harmonic distortion, low dv/dt values, good Electromagnetic compatibility(EMC) and lower filtering L and C requirements on AC side compared to conventional two-level inverter [17]. Many topologies were proposed to have higher power quality as shown in [17]. To attain a multi-level voltage waveform, small steps of DC voltages should be provided by capacitor banks or isolated DC voltages. In [18], a three–level configuration is achieved using cascaded bridge configuration. Using same configuration a three-level voltage wave form is attained by dividing total PV array in two equal parts. The output of PV array decreases sharply with partial shading [10].

Use of bypass diode or connecting more number of panels in parallel is effective way to decrease reduction in output due to non-uniform partial shading [10][19].The present work uses P&O algorithm for MPPT tracking and cascade inverter configuration. Main aim of this paper is to improve reliability and reduce the grid dependency by developing a switching pattern which leads to efficient use of stored energy in battery banks.

Using two-level topology in DC to AC conversion is conventional way of extracting power for PV array. Conventional two-level inverters mostly used today to generate an AC voltage from a DC voltage. A two-level inverter has two output switching voltages + Vdc/2 and – Vdc/2 (total DC link voltage is Vdc). To generate AC output voltage a PWM (modulating signal is compared with carrier wave) used to switch the inverter legs so as to create output wave form similar/close to modulating signal [20]. Advantage of PWM is dominant harmonics are multiples of frequency modulation order ($jm_f \pm 1$) resulting higher frequency harmonics and eventually reducing filtering requirements. Higher the carrier frequency leads to higher order harmonics and lower filtering requirements [21]. Depending on the switching capability of IGBT/MOSFET carrier frequency is determined. Switching frequency for any device is determined by turn-off characteristics which is sum of gate recovery time (Tgr) and reverse recovery time (Trr). Disadvantages of two-level topology is high dv/dt, high EMI, higher filtering requirement on AC side (i.e. large L and C values). For some applications where constrain of space (lower filtering requirements) and stringent EMI/EMC needed to be met where two-level is not advisable [20]-[21]. The disadvantages of two-level topology is outlined as follows

I . High THD [4][9]

II. High dv/dt ratio[4][9]

III. High rating of filter i.e large L and C

IV. High rating switches[4][9]

The above disadvantages can be overcome by use of multi-level inverter configurations i.e., a three-level configuration as shown in fig. 12.

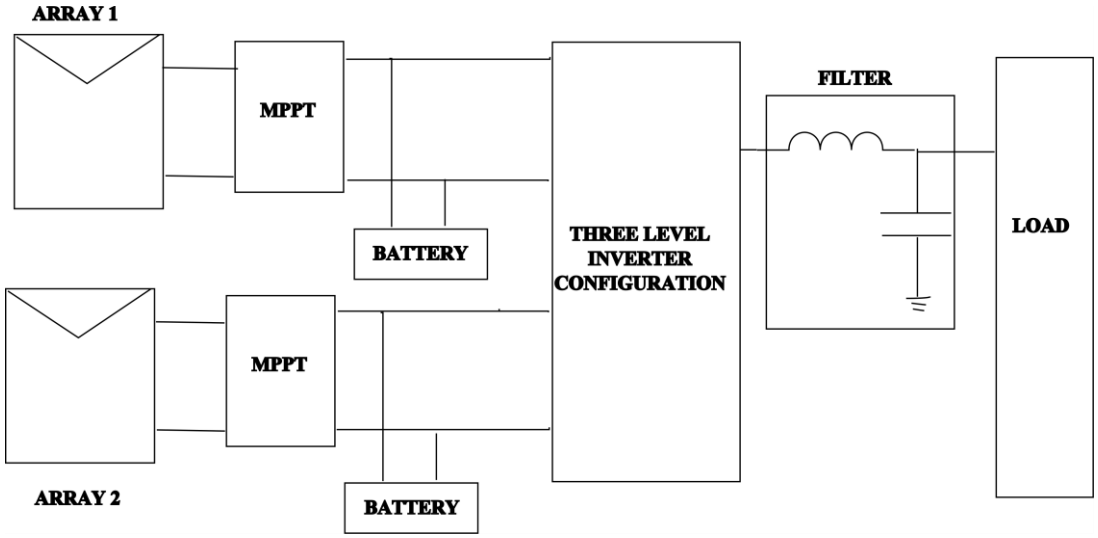

Fig 12. Solar energy extraction from a three-level inverter

2.2 Configurations of Multi-level inverters

The multilevel waveform starts from three level in output. It was first introduces by Nabae with Neutral Point Clamped inverter [24]. By increasing the number of levels in the inverter, the output voltages have more steps generating a staircase waveform, which has a reduced harmonic distortion. However, a high number of levels increases the control complexity and introduces voltage imbalance problems. Three different topologies have been proposed for multilevel inverters: diode-clamped (neutral-clamped), capacitor-clamped (flying capacitors) and cascaded inverters with separate dc sources. In addition, several modulation and control strategies have been developed or adopted for multilevel inverters including the following: multilevel sinusoidal pulse width modulation (PWM), and space-vector modulation (SVM).The most attractive features of multilevel inverters are as follows [17].

1) They can generate output voltages with extremely low distortion.
2) Draw input current with very low distortion.
3) Generate smaller common-mode (CM) voltage, In addition, using different modulation methods, CM voltages can be eliminated.
4) Can operate with a lower switching frequency.

2.2.1 H-bridge inverters

Cascaded H-bridge (CHB) multilevel inverter is one of the popular converter topologies used. It is composed of a multiple units of single-phase H-bridge power cells. The H-bridge cells are normally connected in cascade on their ac side to achieve required voltage and low harmonic distortion. The use of identical power cells leads to a modular structure, which is an effective means for cost reduction. The cascaded -bridge multilevel inverter requires a number of isolated dc supplies, each of which feeds an H-bridge power cell. The dc supplies are normally obtained from diode rectifiers. A single-phase H-bridge power cell, which is the building block for the CHB inverter is shown in fig. 13 PWM schemes can be phase-shifted and level-shifted modulations.

Figure shows a simplified circuit diagram of a single-phase H-bridge inverter. It is composed of two inverter legs with two IGBT devices in each leg. The inverter dc bus voltage V_{dc} is usually fixed, while its ac output voltage V_{AB} can be adjusted by either bipolar or unipolar modulation schemes. Table 1 showing switching states and corresponding outputs.

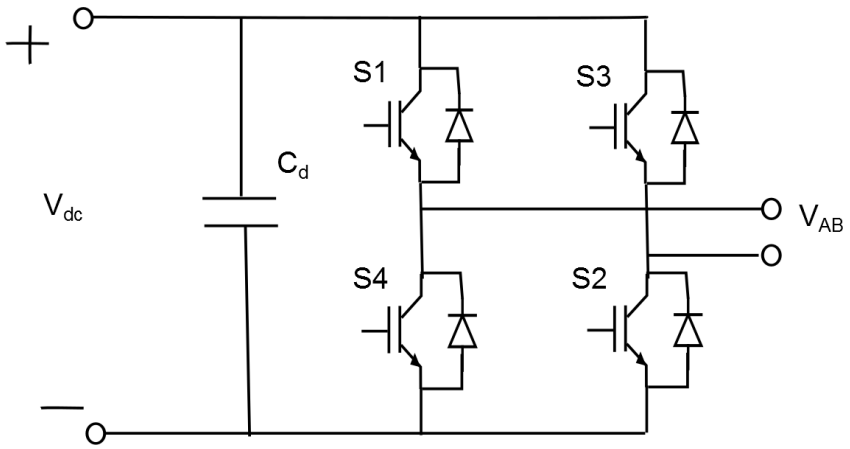

Fig 13: Single phase H- bridge power cell

The number of voltage levels in a CHB inverter can be found from

$$m = (2H + 1)$$

where *H* is the number of H-bridge cells per phase leg. The voltage level *m* is always an odd number for the CHB inverter while in other multilevel topologies such as diode-clamped inverters, it can be either an even or odd number.

Table 1: A single cell H-bridge switching states and corresponding outputs

SWITCHES				OUTPUT
S1	S2	S3	S4	VAB
ON	ON	OFF	OFF	$+\mathbf{V_{dc}}$
OFF	OFF	ON	OFF	$-\mathbf{V_{dc}}$
ON	ON	OFF	OFF	**0**
OFF	OFF	ON	ON	**0**

Fig. 14 showing a three-level 3 phase H bridge configuration and corresponding phase to neutral output in fig. 15

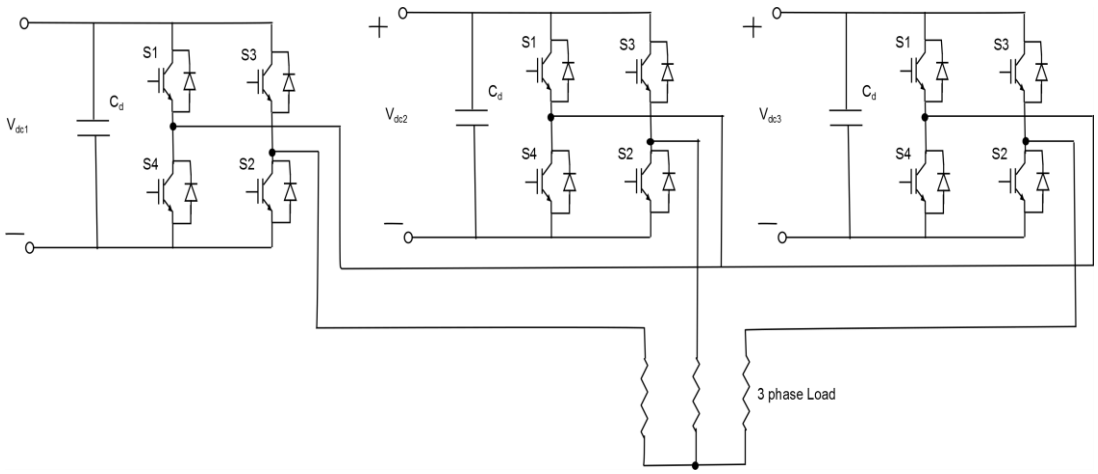

Fig 14: A three-level three phase H-bridge configuration

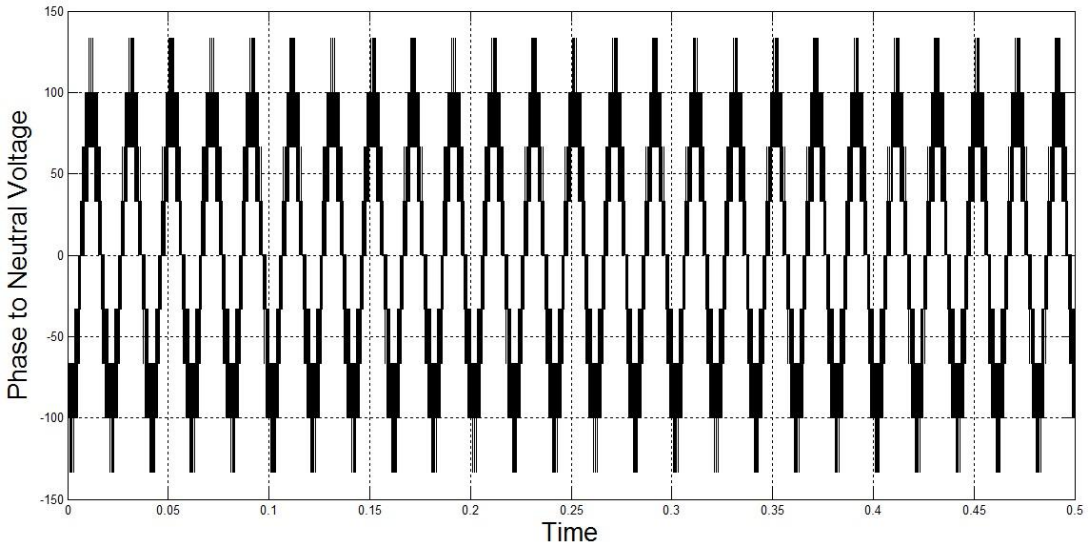

Fig 15: Phase to Neutral Voltage H-bridge inverter

2.2.2 Neutral Point Clamped

Three-level inverter which found wide applications is Neutral point clamped (NPC).The Neutral point clamped inverter employs clamping diodes and cascaded DC capacitors to produce ac three-level voltage waveform. Fig.16 shows the simplified circuit diagram of a three-level NPC inverter. The inverter leg A is composed of four active switches *S*1 to *S*4.

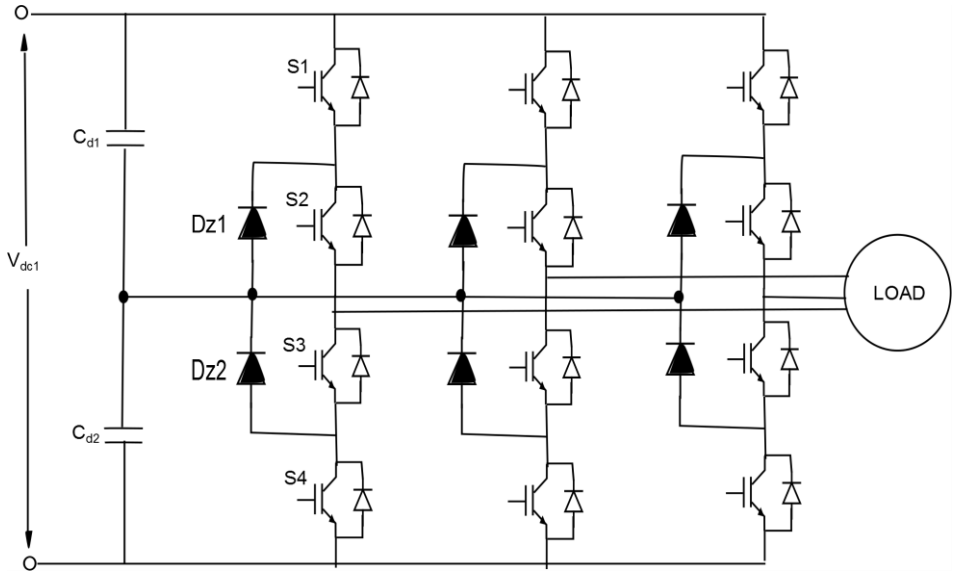

Fig 16: Three Phase NPC inverter

On the DC side of the inverter, the dc bus capacitor is split into two, providing a neutral point *Z*. The diodes connected to the neutral point, D_{Z1} and D_{Z2}, are the clamping diodes. When switches *S*2 and *S*3 are turned on, the inverter output terminal A is connected to the neutral point through one of the clamping diodes. The voltage across each of the DC capacitors is E, which is normally equal to half of the total DC voltage V_{dc}. With a finite value for C_{d1} and C_{d2}, the capacitors can be charged or discharged by neutral current *i.e.*, causing neutral-point voltage deviation. The operating status of the switches in the NPC inverter can be represented by switching states shown in Table 2. Switching state 'P' denotes that the upper two switches in leg A are on and the inverter terminal voltage $\mathbf{V}_{AZ}$, which is the voltage at terminal *A* with respect to the neutral point Z, is $+V_{dc}/2$, whereas 'N' indicates that the lower two switches conduct, leading to $\mathbf{V}_{AZ} = -V_{dc}/2$. Switching state 'O' signifies that the inner two switches *S*2 and *S*3 are on and $\mathbf{V}_{AZ}$ is clamped to zero through the clamping diodes. Depending on the direction of load current i_A, one of the two clamping diodes is turned on. For instance, a positive load current ($i_A > 0$) forces D_{Z1} to turn on, and the terminal *A* is connected to the neutral point *Z* through the conduction of D_{Z1} and S_2.

It can be observed from Table 2 that switches S1 and S3 operate in a complementary manner. With one switched on, the other must be off. Similarly, S2 and S4 are a complementary pair as well. The waveform for V_{AZ} has three voltage levels, +Vdc, 0, and –Vdc, based on which the inverter is referred to as a three-level inverter. As the currents leaves and enters capacitors causing charging and discharging of capacitors which results in unstable neutral point . To maintain neutral point voltage constant a complex switching control along with feedback is needed. Fig 17(a) and 17(b) showing Pole voltage and Phase to Neutral Voltage for a NPC inverter.

Table 2: Three phase three-level NPC switching states and corresponding outputs

SWITCHES				OUTPUT VOLTAGE
S1	S2	S3	S4	V_{AN}
ON	ON	OFF	OFF	$\mathbf{+V_{dc}/2}$
OFF	OFF	ON	ON	$\mathbf{-V_{dc}/2}$
OFF	ON	ON	OFF	**0**

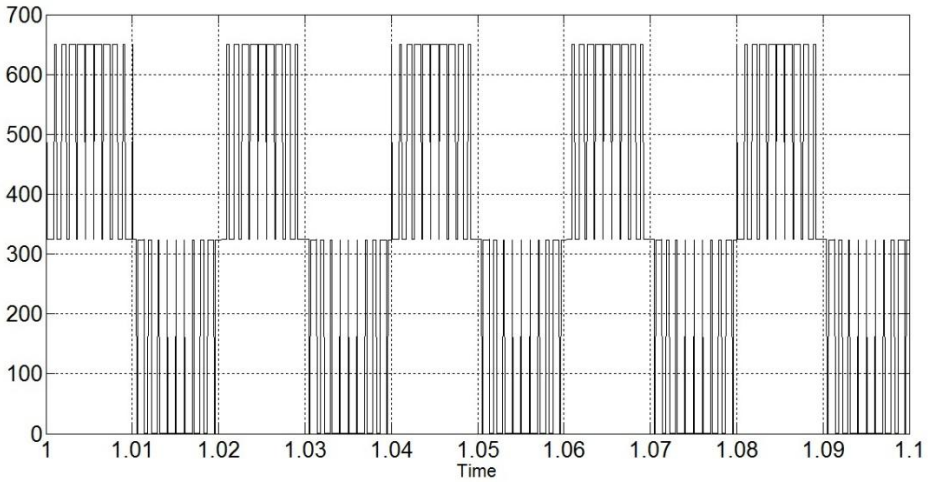

Fig 17(a): Output Pole Voltage of NPC inverter

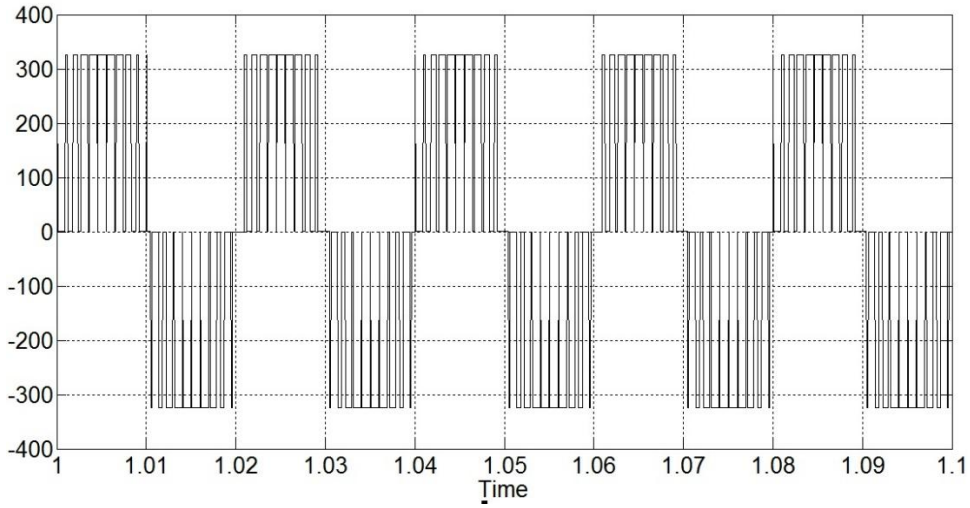

Fig 17(b): Output Phase to Neutral Voltage of three phase NPC inverter

2.2.3 Flying-Capacitor Inverters

Fig.18 shows a typical configuration of a three-level flying-capacitor inverter configuration. It is evolved from the two-level inverter by adding/subtracting DC capacitors. Table 3 showing switching states and corresponding outputs. Fig 19 showing output phase to neutral voltage for a three-level flying-capacitor configuration.

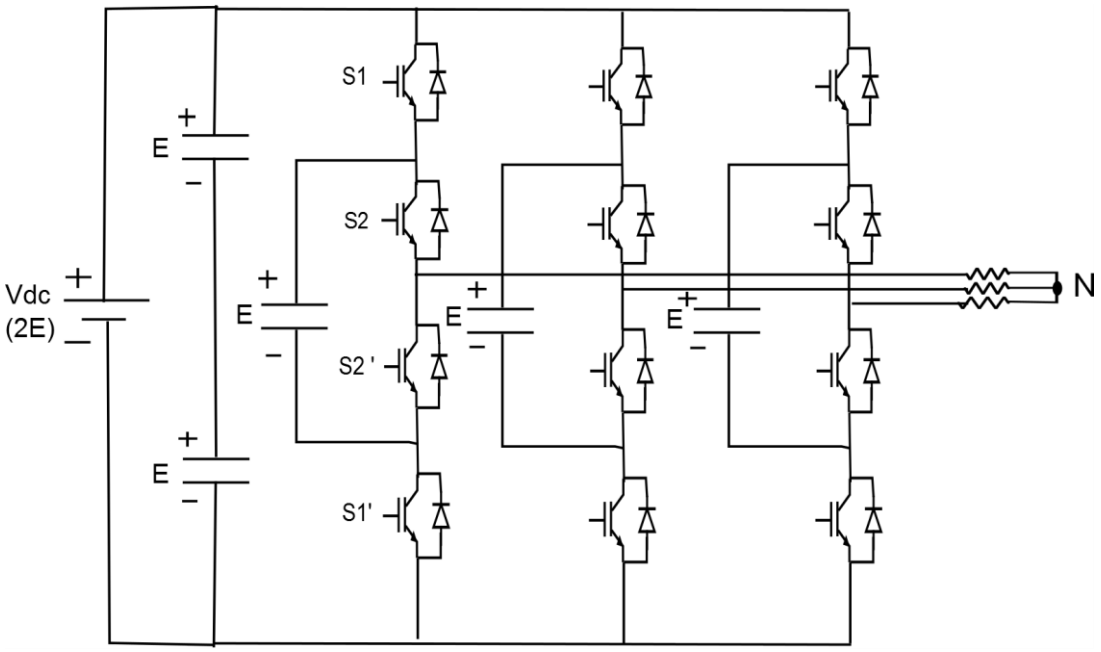

Fig 18: Three-level flying bridge inverter

Table 3: A three-level flying capacitor switching states and outputs

SWITCHES				OUTPUT VOLTAGE
S1	S2	S2’	S1’	V_{AN}
ON	ON	OFF	OFF	**+2E**
ON	OFF	ON	OFF	**+E**
OFF	ON	OFF	ON	**+E**
OFF	OFF	ON	ON	**0**

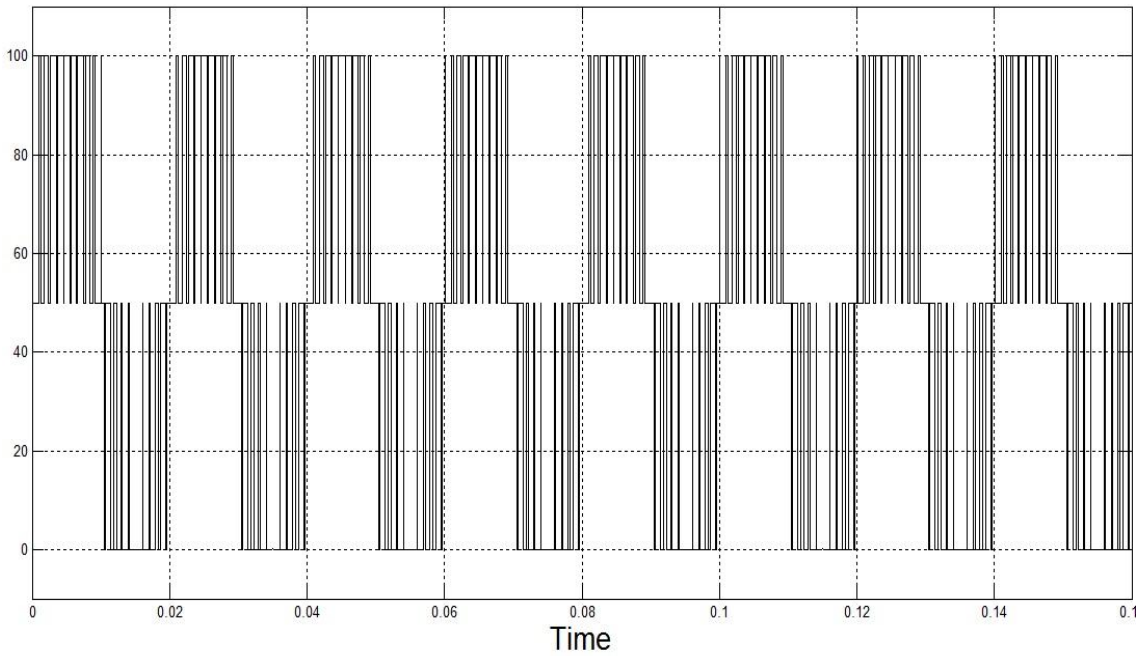

Fig 19: output phase voltage of three-level flying-capacitor inverter

2.2.4 Cascaded Two-level inverters

A novel topology was proposed by cascading two two-level inverter was introduced in [18]. For same three-level output H-bridge topology requires six isolated sources which is a much expensive and huge backset for H-bridge topologies. The main disadvantage of Neutral point inverter is because of capacitors continuous charging and discharging addition control needed to maintain neutral point voltage at $V_{dc}/2$. In [18] a three-level is achieved by cascading two individual two-level inverters as shown in fig 20. Each inverter is supplied by isolated source of $V_{dc}/2$.

A line to Neutral voltage of " Vdc/2" is obtained if

(a) The top switch of that leg in inverter-1 is turned ON,
(b) The top switch of the leg in inverter-2 is turned ON

A line to Neutral voltage of "-Vdc/2" is obtained if

(a) The top switch of that leg in inverter-1 is turned OFF and
(b) The bottom switch of the inverter-2 is turned ON

A line to Neutral voltage of "0" is obtained if

(a) The bottom switch of inverter-1 is switched ON

(b) The top switch of inverter-2 is switched ON

Fig. 21(a) and 21(b) shows Phase voltage and line to line voltage for a three-level cascaded inverter. Table 4 showing switching states and corresponding outputs.

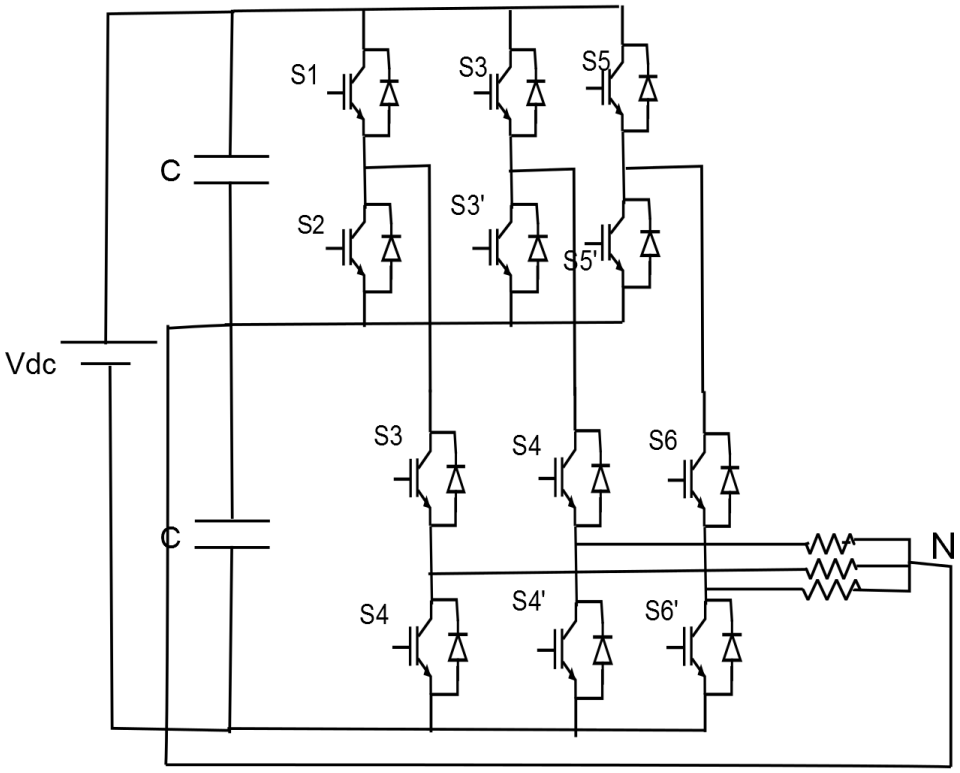

Fig 20: Three phase three-level Cascade Bridge inverter

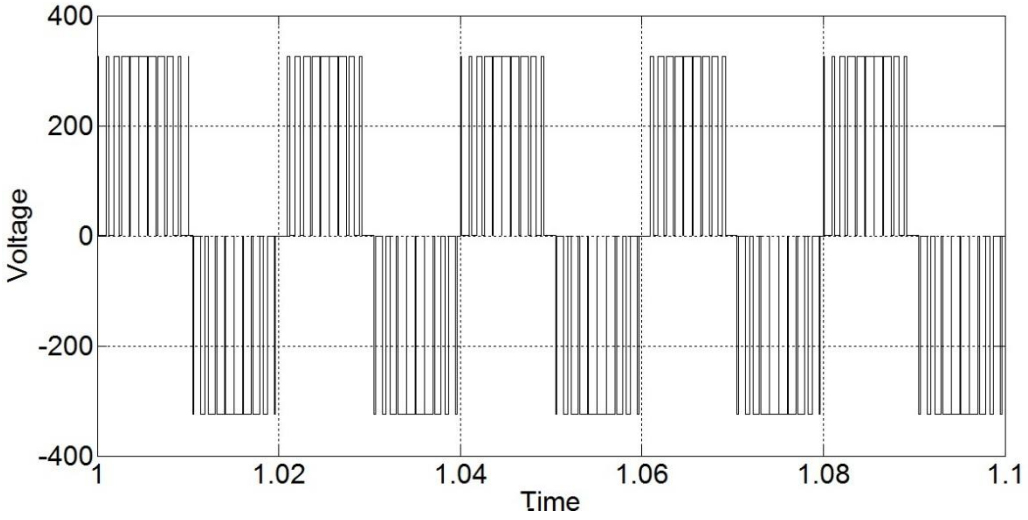

Fig 21(a): Phase Voltage of cascaded bridge inverter

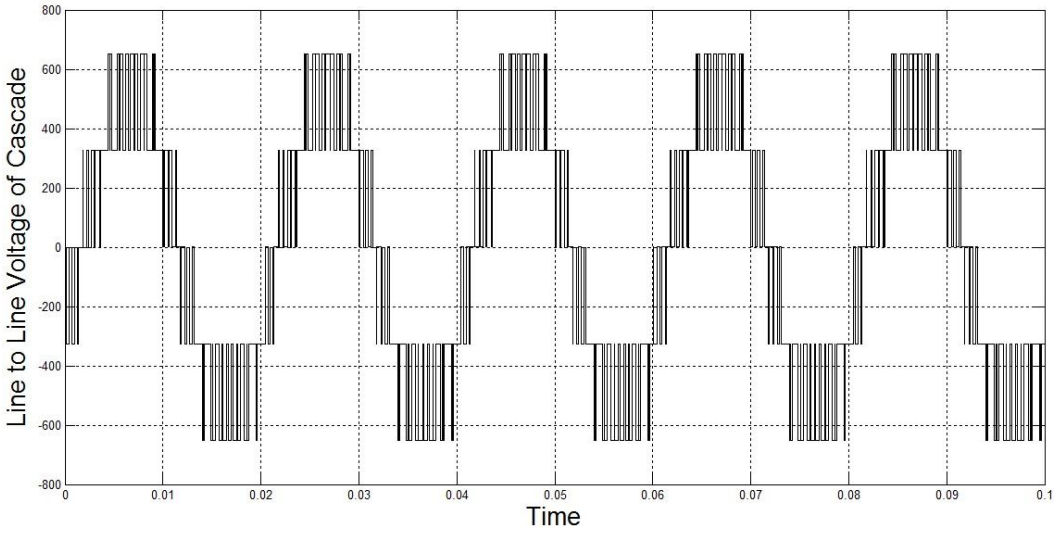

Fig 22(b): Line to line voltage cascaded bridge inverter

Table 4: Switching states and corresponding outputs for three-level cascaded inverter

SWITCHES				OUTPUT VOLTAGE
S1	S2	S3	S4	V_{AN}
ON	OFF	ON	OFF	$+V_{dc}/2$
OFF	OFF	OFF	ON	$-V_{dc}/2$
OFF	ON	ON	OFF	**0**

2.3 Carrier Based PWM Techniques for Multi-level inverters

The carrier-based modulation schemes for multilevel inverters can be generally classified into two categories: phase-shifted and level-shifted modulations.

2.3.1 Phase shifted Multicarrier Modulation

In general, a multilevel inverter with m voltage levels requires (m – 1) triangular carriers. In the phase-shifted multicarrier modulation, all the triangular carriers have the same frequency and the same peak-to-peak amplitude, but there is a phase shift between any two adjacent carrier waves, given by

$$\text{Phase Shift} = 360^0/(\text{m} - 1)$$

For a three-level inverter

m=3

Number of carrier waves = 2

Phase Shift between carrier waves = $360^0/(3\text{-}1) = 180^0$

Following fig.22 (a) shows Phase shift for a three-level inverter

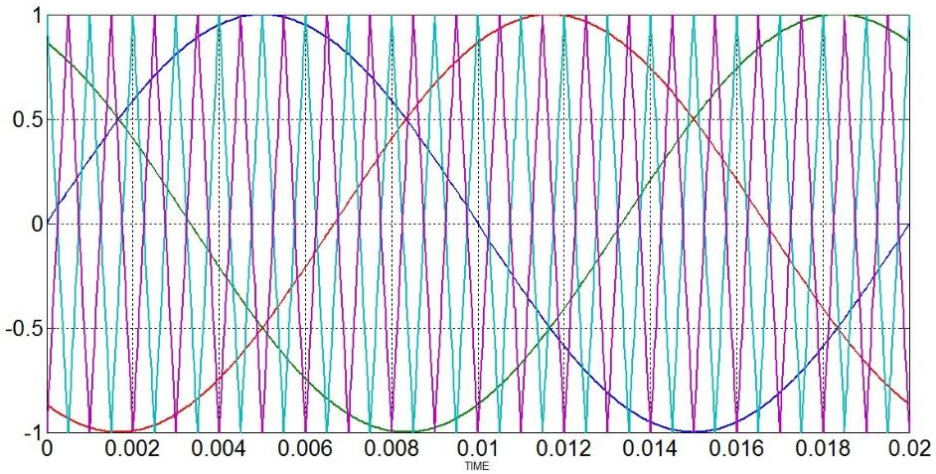

Fig 22(a): Phase shift for a three-level inverter

2.3.2 Level-Shift Multilevel carrier wave

Similar to the phase-shifted modulation, an m-level CHB inverter using level-shifted multicarrier modulation scheme requires (m – 1) triangular carriers, all having the same frequency and amplitude. The (m – 1) triangular carriers are vertically disposed such that the bands they occupy are contiguous. The frequency modulation index is given by m_f = fcr/fm, which remains the same as that for the phase-shifted modulation scheme whereas the amplitude modulation index is defined as where V_m is the peak amplitude of the modulating wave V_m and V_{cr} is the peak amplitude of each carrier wave.

$$m_a = \frac{V_m}{V_{cr}(m-1)}$$

Following fig 22 (b) shows level shift for a three-level inverter

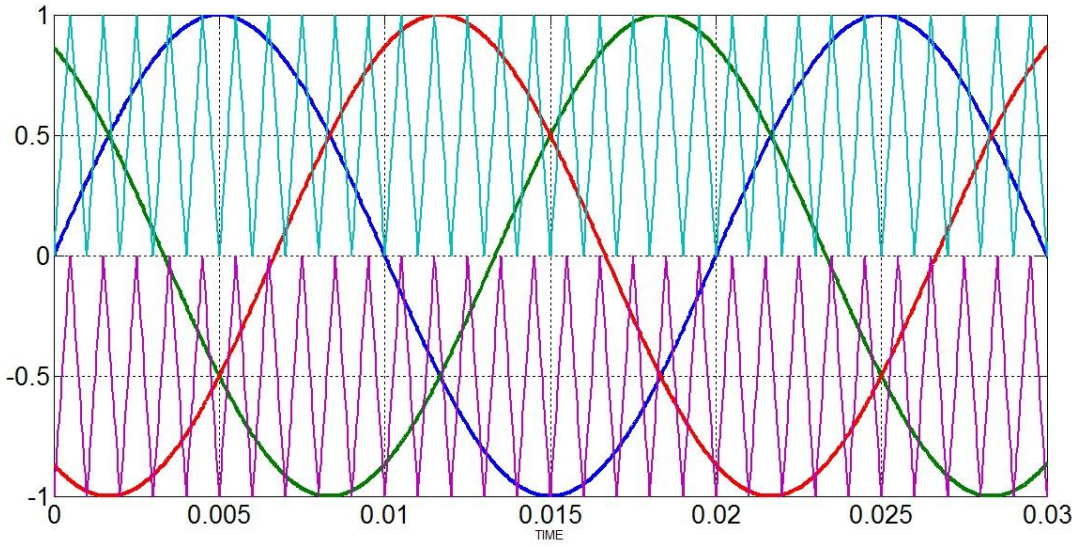

Fig 22(b): level shifted for a three-level inverter

Chapter 3

Output Filter design and Modes of Operation

Output of inverter contains high harmonic distortion. So there is a need to filter out this harmonics before giving to load or grid. This filtering action is done by second order filter as shown in fig 23. This second order filter is typical low pas filter. The values of L (Inductance) and C (Capacitance) depends on required attention by filter. Higher quality of output required higher is filtering requirements.

Table 5: Properties of filter

Filter	**Order**	**Attenuation**	**Resonating Frequency**
L	First	-20 dB/decade	----
LC	Second	-40 dB/decade	$f_o = \frac{1}{2\pi\sqrt{LC}}$
LCL	Third	-60 dB/decade	$f_o = \frac{1}{2\pi}\sqrt{\frac{L_1 + L_2}{L_1 L_2 C}}$

Following is procedure to design L and C values for filtering

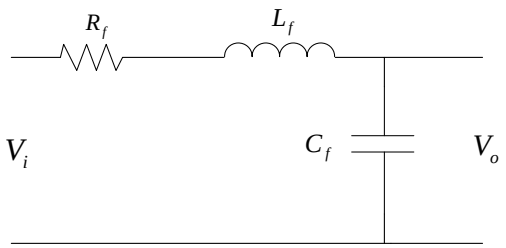

Fig 23: Second order filter

3.1 Design Procedure

Transfer function of second order filter

$$G(s)=\frac{V_o(s)}{V_i(s)}=\frac{1}{L_f C_f s^2+R_f C_f s+1} \qquad (1)$$

Comparing it with standard second order characteristic equation

$$s^2+2\xi\omega_n s+\omega_n^2=s^2+\frac{R_f}{L_f}s+\frac{1}{L_f C_f}$$

Resonating frequency $\omega_o=\frac{1}{\sqrt{L_f C_f}}$, Resonant peak $Q=\frac{1}{R_f}\sqrt{\frac{L_f}{C_f}}$

Voltage drop in the filter is expressed as

$$V=L_f\frac{\Delta I}{\delta T_s}+(\Delta I)R_f$$

Where ΔI is the maximum allowable current ripple in the inductor

δ is the duty ratio.

T_s is switching time period.

$$I=\frac{S}{V}$$

Where S and V are apparent power and voltage rating of load respectively.

Select resonating frequency f_o to be $\frac{1}{10}$ of switching frequency f_s to get 40 dB attenuation.

$$20\log\left(\frac{\omega_s}{\omega_o}\right)^2=40.$$

Choose ξ in the limits $0<\xi<1$ to get stable response.

Inverter specifications:

Rating of inverter	=	20 KVA
RMS output voltage	=	400 V
Switching frequency	=	2 kHz

DC bus voltage	=	825 V
Modulation index	=	0.97
AC system frequency	=	50 Hz
Duty ratio of pulses	=	0.75
Damping ratio	=	0.5
Percentage of current ripple	=	15%

Calculated filter parameters:

$R_f = 0.29488\Omega$

$L_f = 1.47441mH$

$C_f = 0.4294963mF$

3.2 Modes of Operation

There are basically two modes of operation namely

(i) Islanded Mode

(ii) Grid Connected Mode

PV can operate in either mode depending on conditions and requirements

3.2.1 Islanded mode of operation

Islanded Mode Control Consists of two loops as shown in fig.24 and fig.25. One is voltage control loop use to maintain required voltage. Secondly, current loop use to regulate current going to load [22]. In case of microgrid, distributed generation units are operated by micro-control units. These micro-control units in turn receive set points from central-controller. For a single load and single generation unit with battery backup these set points are constant i.e. to supply constant voltage and frequency to load irrespective of load. These fixed points are desired voltage and desired frequency.

Voltage control

The idea of voltage control scheme is obtained from the current relation of interface filter between inverter and the system. Voltage controller process the error signal between target voltage command and output voltage and generates target current command. Basic Proportional Integrator (PI) compensator can be used to process the error signal. The compensator gains are tuned using classical control techniques such that the closed loop system turns out to be linear. Under steady state the compensator will push the error signal close to zero. The dq components are decoupled by adjusting current terms (VqωCf) and (VdωCf) in d and q current components respectively. Feed forward output dq current components mainly contribute targets current commands in steady state. The output currents are varied with the load variation. Voltage controller will adjust the target current command with the adjustment of feed forward output current according to the load variation. A dq based voltage controller is shown in below fig. 24.

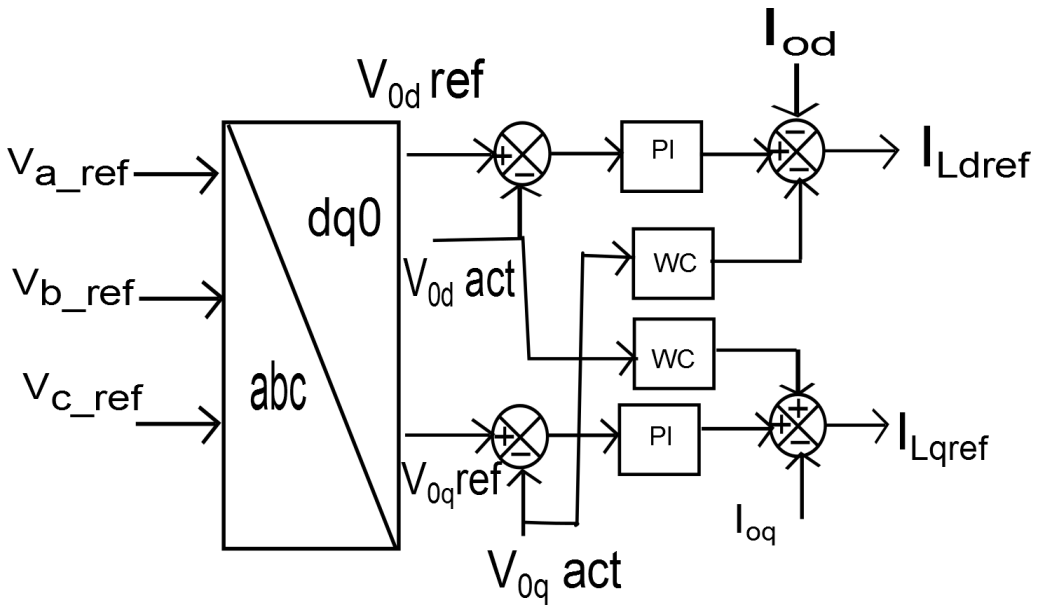

Fig. 24 Voltage control for islanded mode control

Current Control:

The voltage relation of interface filter form the basis for current control of PV unit. The compensator of current controller process the error signal and generates reference voltage signal for inverter operation of PV unit. This reference signal is given to SPWM circuit to generate the required gate pulses. Current controller forms the inner loop with outer voltage

control loop in the closed loop control. Stability of closed loop plant with both voltage and current control loops is enhanced by proper tuning of voltage and current controllers. This can be done by performing stability analysis using available control techniques. Another important feature of current controller is its inherent capability to limit the PV unit output current. Current controller will push the error signal to zero in steady state. Therefore, the reference voltage signal is mainly due to feed forward voltage terms. Here, the dq components are decoupled by adjusting the voltages (IqωLf) and (IdωLf) in Vd and Vq respectively. A dq based current controller is shown in below fig. 25.

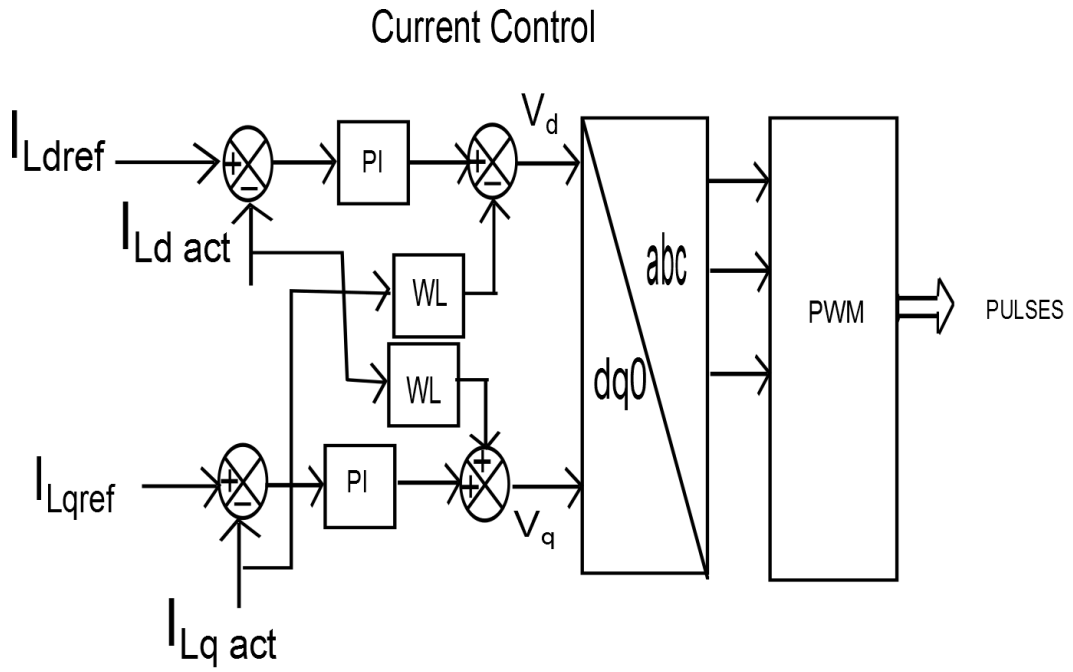

Fig 25: Current Control for Islanded Mode Operation

Overall control structure for Islanded mode of operation with outer voltage loop and inner current control is shown in fig. 26.

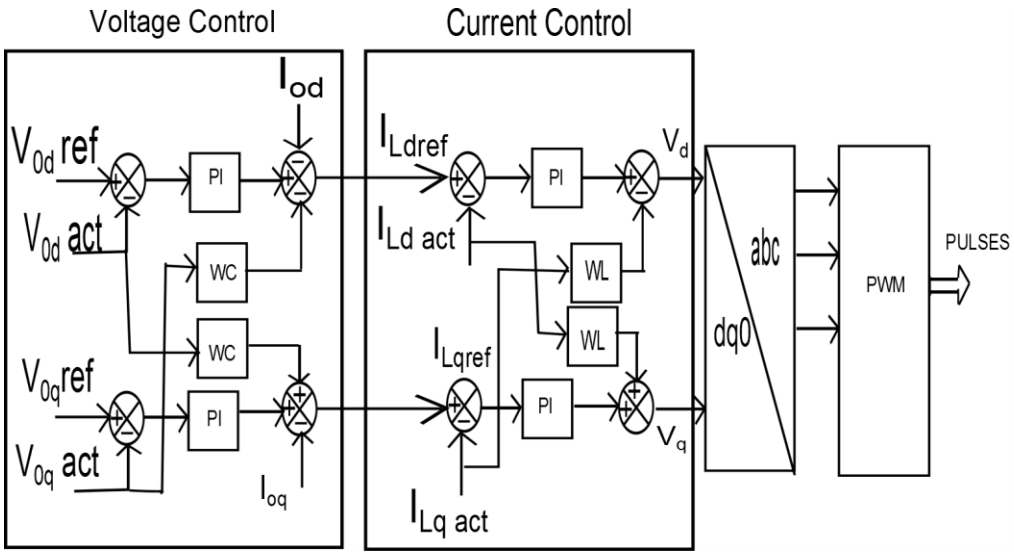

Fig 26(a) : Overall control in Islanded mode operation

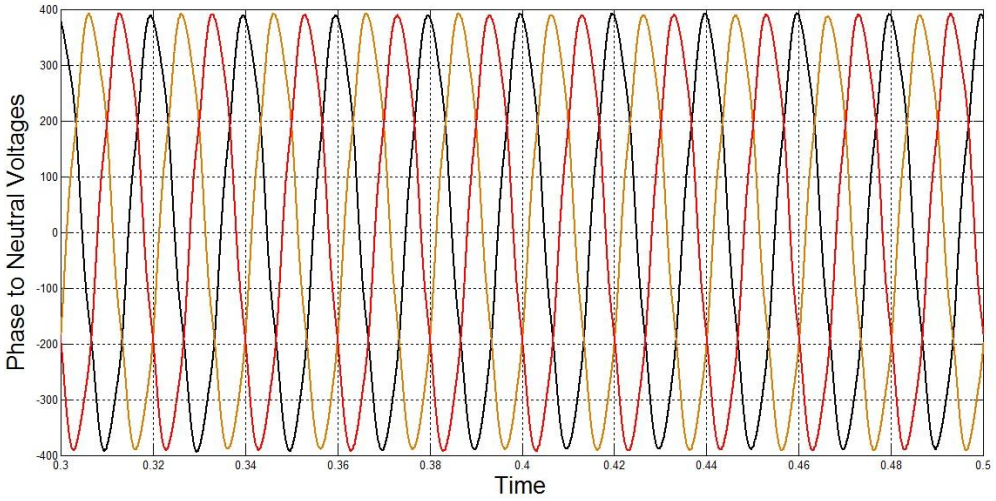

Fig 26(b) : Phase to neutral voltages in Islanded mode operation

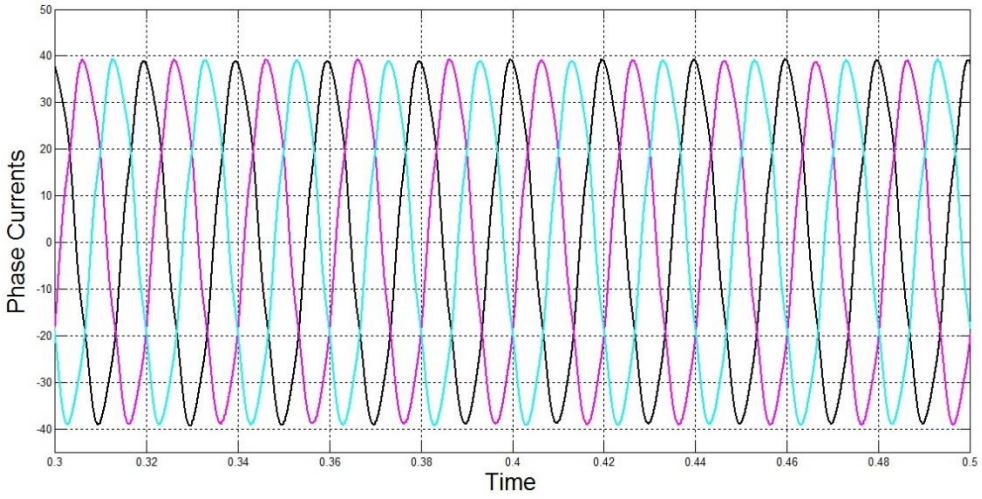

Fig 26(c) : Three phase currents in Islanded mode operation

3.2.2 Grid mode of operation

The control for grid connected PV system is done by maintaining DC link voltage constant. The governing equation for DC link control. The capacitor voltage is maintained constant using droop control. Fig. 28 shows mathematical block diagram of DC voltage link control for grid connected mode.

$$I_{dref} = kp * \left(V_{dcref} - V_{dc}\right) + Ki \int (Vdcref - Vdc)\ \ dt \qquad (5)$$

Voltage controller can be neglected in grid connected mode of operation. The design of current controller is similar to the earlier case as explained in autonomous mode. The primary objective in this mode is to control is to send to power generated by PV source instantaneously. Mathematically this objective is achieve by keeping capacitor voltage constant. The reactive power reference is taken as zero in order to achieve unity power factor.

$$P = \frac{3}{2}\left(V_d I_d - V_q I_q\right)$$

$$Q = \frac{3}{2}(V_q I_d - V_d I_q)$$

Steady state q-component of voltage is assumed to be zero. Therefore, we can directly get the current components

$$I_d^* = \frac{2P_{ref}}{3I_d}$$

$$I_q^* = -\frac{2IQ_{ref}}{3I_q}$$

Block diagram of DC link Voltage control is as shown in fig. 27(a)

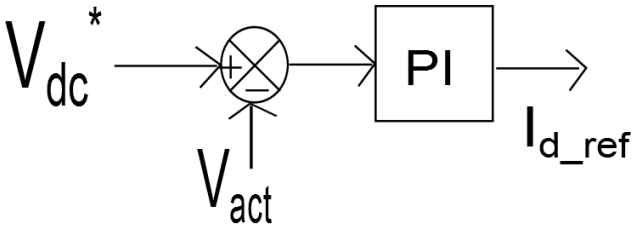

Fig 27(a): DC link Voltage control for grid connected PV system

Reactive Power control block diagram for grid connected PV is shown in fig. 27 (b)

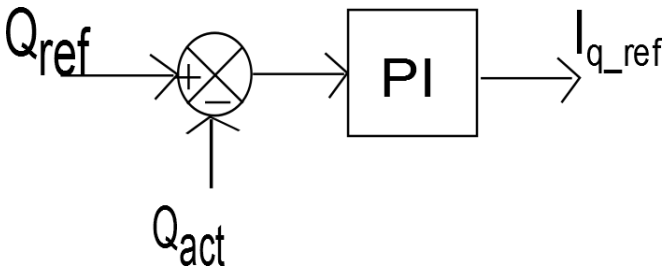

Fig 27(b): Reactive control for grid connected PV system

Overall DC link voltage control and Reactive power control in grid connected mode is shown in fig 28.

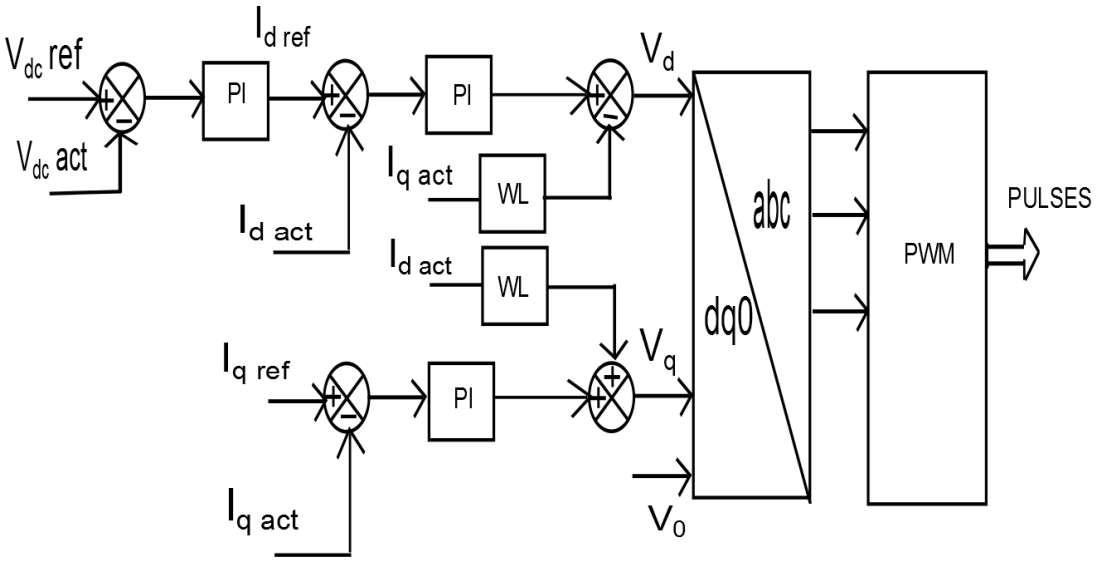

Fig 28: Grid connected PV system with DC-link Voltage and reactive power control

Fig. 29 showing DC link voltage maintained at constant 650V and injected current into grid in fig. 30 with better harmonic profile compared two-level.

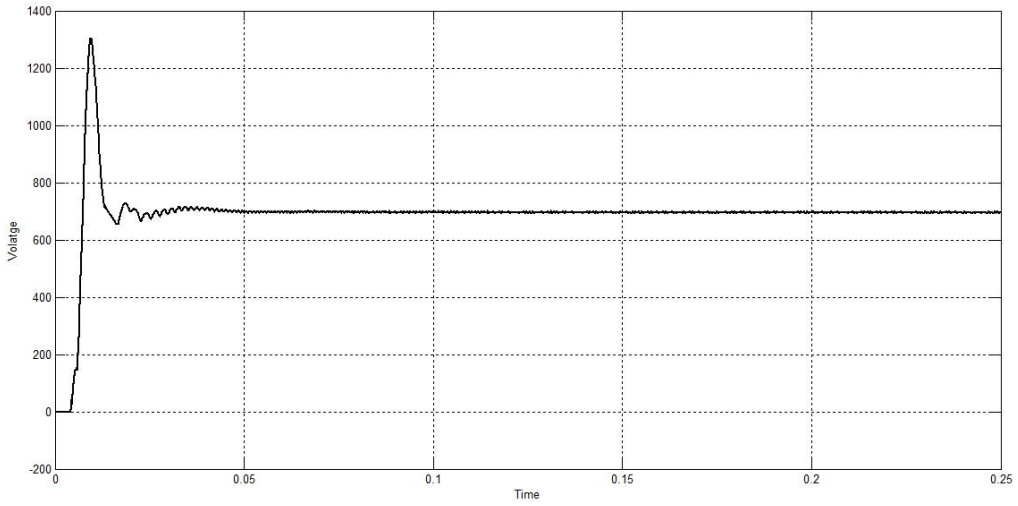

Fig 29: DC-link/Capacitor voltage for a grid connected PV systems

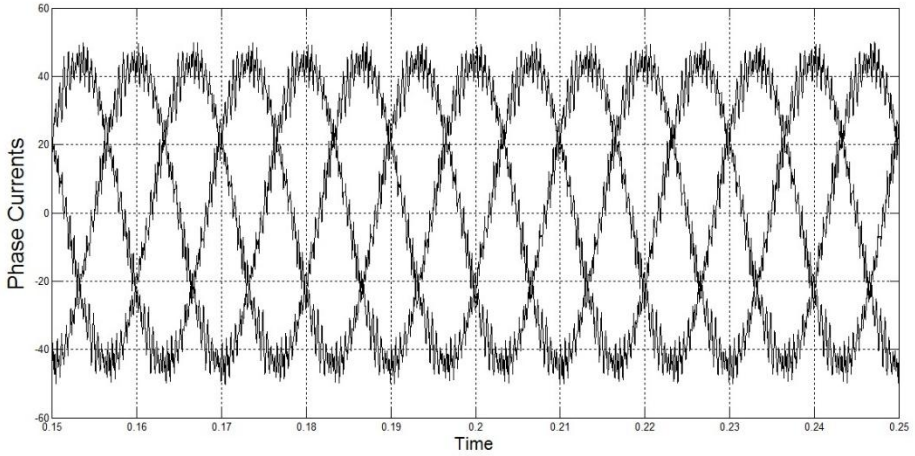

Fig 30: Injected three phase current for three-level inverter Grid connected PV systems

Chapter 4

Proposed Scheme to Keep Battery Banks within Threshold and Efficient Use of Stored Energy

4.1 Logic to keep battery banks with in threshold

For complete utilization of battery banks to run more time the following scheme is proposed. The total number of panels are 2N (N each in top and bottom). Out of N in array-A, N_A are isolated similarly N_B from array-B as shown in fig 31. Note that depending on the irregularity of roof top N_A may or may not equal to N_B [25].

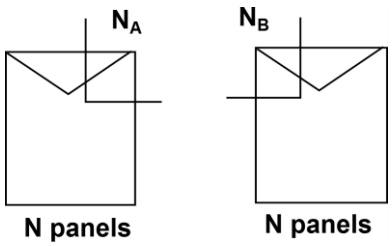

Fig 31: Proposed Scheme

Unequal SOC's are result of uneven partial shading on top and bottom arrays. For selection of N_A and N_B max unevenness in power output of top and bottom arrays has to be determined (worst case conditions are to be taken). Assuming linearly each panel in array-A and array-B are delivering P_A and P_B respectively [25].

Event 1: For ($P_A > P_B$)

Implies array-A is delivering more power than array-B. In order to minimize the difference in SOC's Ax panels are taken from array-A and connected to array-B .To know Ax optimize the following equation

Minimize $\{|[N - A_X]\ P_A - [N*P_B + P_A A_X]|\}^2$

Event 2: For ($P_A < P_B$)

It is exact contrast to of above case where array-B is supplying more than array-A. In this case N_B number of panels are taken from array-B and connected to array-A. For selection of Bx optimize following equation

Minimize $\{|[N - B_X] P_B - [N*P_A + P_B B_X]|\}^2$

Depending of the irregularity of the roof top there might be anyone case or both cases. According to proposed scheme, now the system becomes as shown in fig. 30 with switches S1 and S4 complimentary to S2 and S3.

After isolating Ax and Bx, controlling of Ax and Bx is vital depending on the conditions. Selection of threshold is trade-off between minimizing the difference of SOC's and switching frequency of isolated panels. To avoid continues switching i.e. instead of making the error signal to operate on verge of threshold it is taken to opposite threshold value. Following are possible occurrences and corresponding switching action [25]

Case I : (SOC A - SOC B) < (-Threshold)

Connect Ax to Array A
Connect Bx to Array A

Case II : (SOC A - SOC B) > (+Threshold)

Connect Ax to Array B
Connect Bx to Array B

Case III : (-Threshold)<(SOC A - SOC B)< (+Threshold)

Connect Ax to Array A

Connect Bx to Array B

Embedded MATLAB Programme to implement Switching panels logic

```
function [s1, s4, cid1] = fcn(command,v1,v2,cid)

if isempty(cid)
    cid=0;
end

if (command == 0)
    s1=1;
    s4=1;
    cid1=0;

else

 if (v1-v2)>1
     s1=0;
     s4=1;
     cid1=1;

 elseif (v1-v2)<-1
     s1=1;
     s4=0;
     cid1=2;

 elseif (cid==1 && (v1-v2)>-1)
     s1=0;
     s4=1;
     cid1=1;

     if ((v1-v2) >-1 && (v1-v2)<-0.99)
         cid1=0;
     end

 elseif (cid==2 && (v1-v2)<1)
     s1=1;
     s4=0;
     cid1=2;

         if ((v1-v2)<1 && (v1-v2)>0.99)
             cid1=0;
         end

 else
     s1=1;
     s4=1;
     cid1=0;


 end

end

 end
```

4.1 Efficient utilization of stored energy in battery banks from sunset

Once the battery banks are kept within threshold next step would be effective use of stored energy in battery banks. Since from sunset demand is met by battery banks or connecting to grid. Efficient use of stored energy can lead to improve in reliability and reducing dependency. To achieve this objectives a logic is developed which takes care of changing between island and grid connection mode. The switching pattern leads to more reliable supply and reduce grid dependency. The objective is achieved by operating mostly in islanded mode by considering demand pattern. Fig.32 shows a most common demand pattern for any house hold [24]. For example a consumer of 2KW of peak load and total number of units consumed in day is 18.5 Kwhrs is considered. From fig.9 peak demand occurs from 7:00 PM to 10:00 PM. Fig. 33 shows generation pattern of PV systems which starts around 8:00 AM and lasts until 6:30 PM with peak generation at noon times. PV generation minus load curve is shown in Fig. 34. From fig.34 it can be observed that PV generation is more than load only between 10:00 AM to 5:30 PM. The positive curve represents excess power which is stored in battery banks. From evening 6:00 PM curve enters negative reason which means load needed to be supplied by stored either by battery banks or connecting to grid.

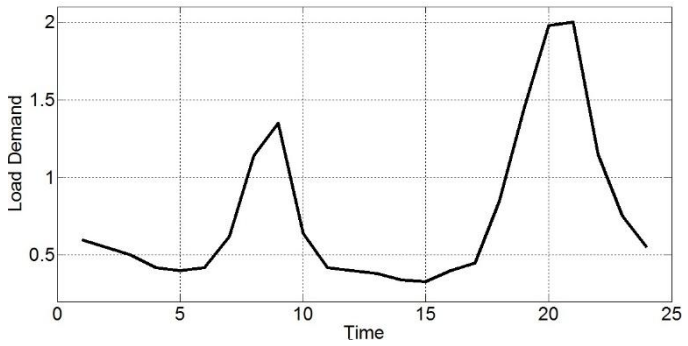

Fig 32: Generic demand pattern of household

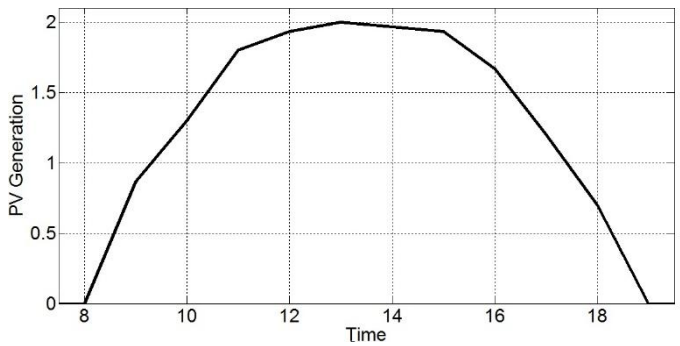

Fig 33: PV generation from 8AM to 19 PM

For the best utilization of stored energy which would benefit both consumer and utility company is using this stored energy during peak hours in dynamic tariff system time at which tariff rate is maximum. The alternative way is using this stored energy to improve reliability and reduce grid reliance for flat rate consumers. This can be done by using an algorithm which will keep tracking of energy stored (SOC *Ah of battery bank) and compare with required energy until next day 10:00 AM. As algorithm keeps track of PV generation minus load curve shown in fig.34 whenever this curve enters negative region it is changes to grid mode.

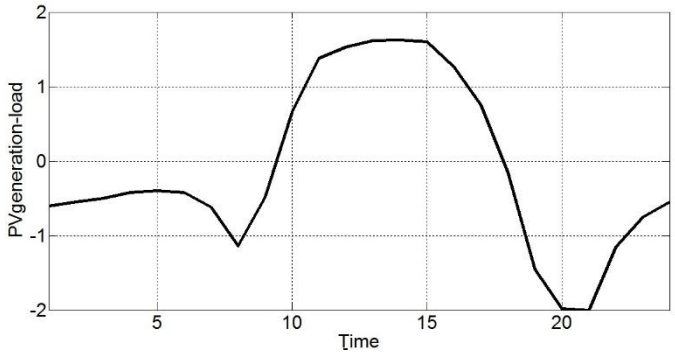

Fig 34: Difference of PV Generation and Load Curve

Transition from grid to islanded mode is done based on energy requirement. Fig.35 shows variation of requirement starting from 6:00PM to 10:00 AM. As battery banks are already taken care to have nearly equal charge by switching isolated panels. It is needless to mention that automatic islanding is done in case of grid failure.

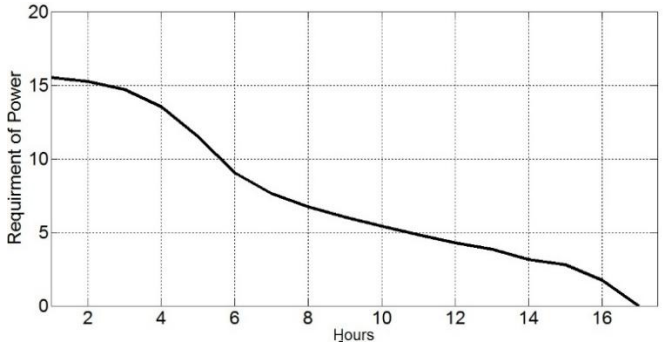

Fig 35: Power Demand from 6:00PM to 10:00AM

Chapter 5

Results

The proposed scheme is simulated and verified in MATLAB/SIMULINK environment. Taking the favorable condition as +/- 1 (Threshold – of total battery capacity) with in which battery banks should operate and following cases were simulated. Simulations were carried assuming the SOC's of batteries are outside the favorable band. For all the cases, error is taken in Y-axis and Time in seconds on X-axis.

Case 1: Initially battery bank A is leading the battery bank B and it is outside the threshold band. Corresponding switching action was taken by control switches S1 and S4 and error is minimized as shown in fig. 36(a). The SOC's of batteries were also shown in fig. 36(b).

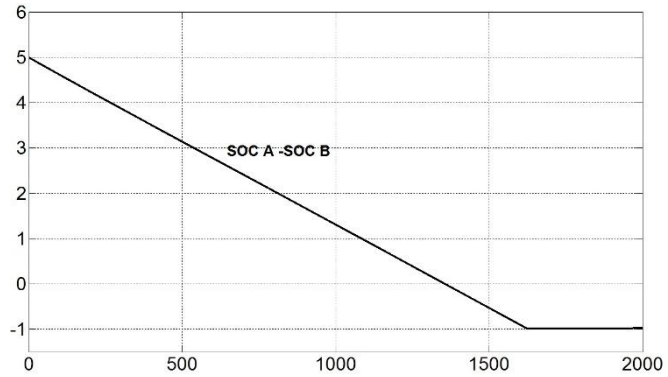

Fig 36(a): Error signal or Difference in SOC's of two battery banks in case 1

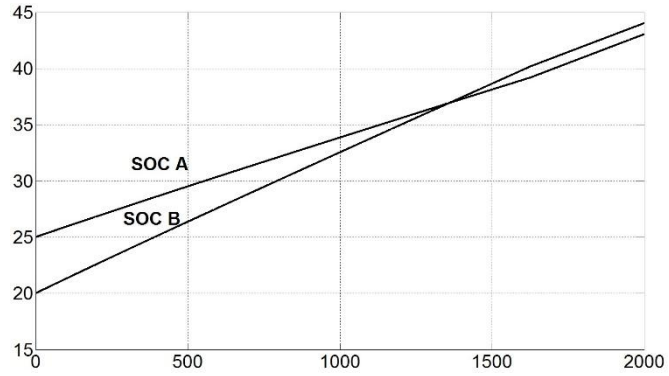

Fig 36(b): SOC's of battery banks A and B

Results 36(a) showing error signal i.e., difference in battery levels of two batteries is gradually approached to negative threshold by switching the isolated panels from array- A and connecting to array-B. Corresponding change in SOC's are shown in fig. 36(b).

Case 2: It is exact contrary to above case where battery bank B is leading to battery bank A and outside the threshold. The error signals minimized by control block by switching S1 and S4 as shown in fig. 37(a).

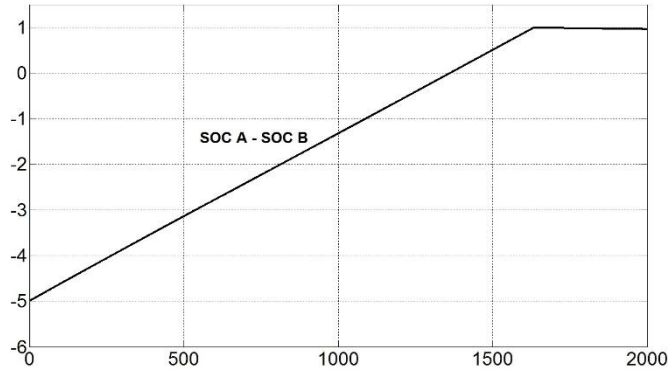

Fig 37(a): Error signal or Difference in SOC's of two battery banks in case 2

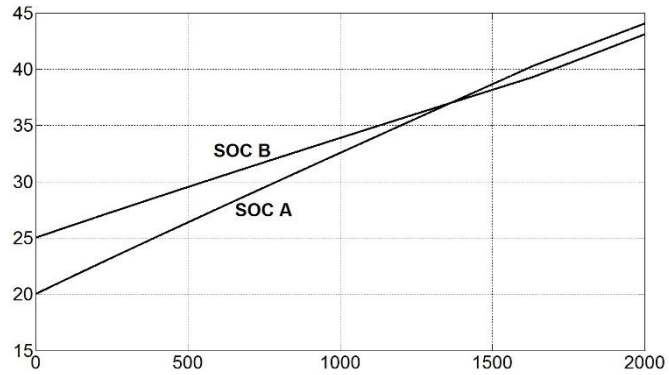

Fig 37(b): SOC's of battery banks A and B

From fig. 37(a) one can observe error is minimized and taken to opposite threshold to avoid continuous switching and corresponding change in SOC's in fig. 37(b)

Case 3: There is need for test to verify control action if battery banks operate within threshold band. The case where battery bank B is leading battery bank A and the error is with in threshold. Ax, Bx connected to array-A and array-B and error remains same as shown in fig. 38(a) and SOC's are shown in fig. 38(b).

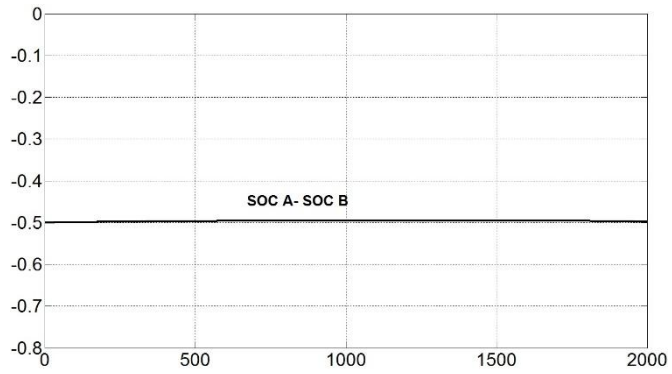

Fig 38(a): Error signal or Difference in SOC's of two battery banks in case 3

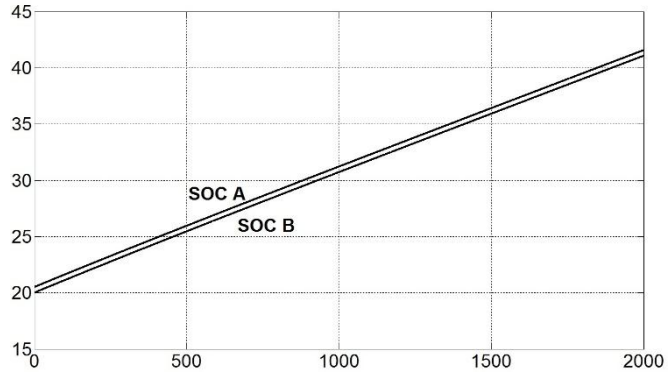

Fig 38(b): SOC's of battery banks A and B

From figures 38(a), 38(b) one can notice isolated panels were connected to corresponding arrays from where they were taken and error remains constant.

Case 4: In this case battery bank A is leading battery bank B and error is with in threshold. Ax, Bx connected to array-A and array-B and error remains same as shown in fig. 39(a) and SOC's are shown in fig. 39(b).

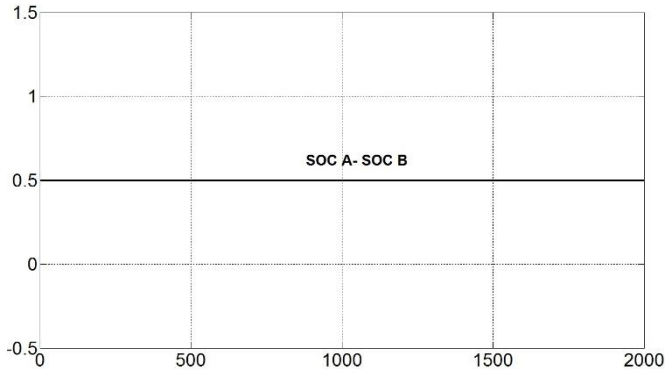

Fig 39(a): Error signal or Difference in SOC's of two battery banks in case4

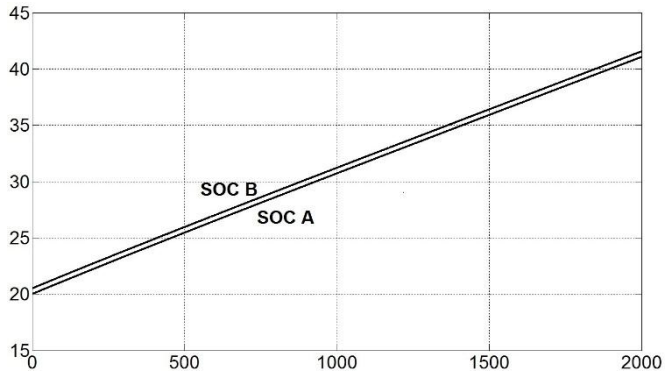

Fig 39(b): SOC's of battery banks A and B

It can be clear from figures 39(a), 39(b) isolated panels are connected to arrays from which they were isolated. Since error is with in threshold no switching takes place and difference in SOC's is maintained constant.

To validate the proposed scheme a household system is considered with 18.5 KWhrs of consumption per day is considered. As mentioned earlier fig. 3(a) shows generation minus load curve. In same fig. 3(a) curve is positive from 10:00 AM to 5:30 PM which implies excess energy stored in battery banks. For considered example by simple integration total stored energy is 10.5 KWhrs. The demand pattern starting from 6:00 PM shown in fig. 3(b) with initial requirement of 15.5 KWhrs.

For assumed household system with 18.5 Kwhrs of consumption per day. From fig.11 battery banks stores between 10:00 AM to 5:30 PM a total of 10.5 Kwhrs units. But for a reliable

supply 15.5 kwhrs is required which is more than stored energy in batteries during day time. Algorithm which keeps on comparing required energy with stored energy in battery banks.

The resultant switching pattern is shown in fig.40 for assumed example.

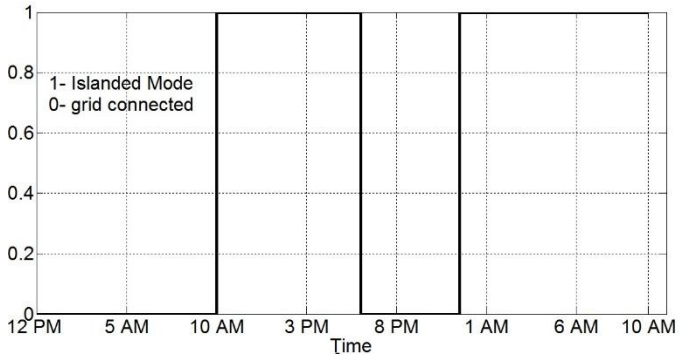

Fig 40: Switching pattern for assumed example

As demand is more than stored energy, system will operate in grid connected mode considering grid is always reliable. As the time progresses desired point is met after 4.5 hours i.e., stored energy is equal or greater than demand. The resultant switching pattern in fig.39 shows change to islanded mode at 10:30 PM.

Chapter 6

Conclusion

A PV system was proposed which allows complete utilization of battery banks by minimizes the difference in discharge levels of battery banks. Selection of isolated panels was described taking worst case deviation of SOC's between top and bottom battery banks. A control policy was developed for switching selected isolated panels depending on present SOC's. In addition a switching technique to switch between islanded and grid mode utilize energy stored in battery banks to improve reliability and reduce grid dependency. To achieve this objective a logic was developed to switch between island and grid connect mode considering generation and load pattern. By making effective utilization of stored energy, user can able to operate more time in islanded mode and improved reliability and reduction in grid dependency may be achieved. By making use of few switches, the proposed scheme can able to operate two battery banks within desired threshold thereby making complete utilization of battery banks. Although proposed technique was implemented on three-level inverter, this can be extended to multi-level inverters with more than two battery banks.

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