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Implementation of Cascade Multilevel Inverter-based STATCOM

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Implementation of Cascade Multilevel Inverter-based STATCOM

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ABSTRACT

This paper deals with the real time implementation of 11-level cascade multilevel inverter-based STATCOM using personal computer (PC) and ADD-ON cards for power system voltage control at the point of common coupling. Complete hardware and software development procedures have been explained in depth for direct as well as indirect control schemes. Experimental results are presented and it is shown that voltage control is achieved using cascade multilevel inverter based STATCOM, thus verifying the very basic purpose of STATCOM. Real time implementation using PC-based control technique has certain merits over digital signal processor based implementation, and some of these merits are high processing speed and low cost of implementation; therefore, PC-based implementation can be used in industry as well as for utility applications.

Keywords:
Capacitor charge balancing, Cascade multilevel inverter, Modulation index, Static synchronous compensator, Total harmonic distortion.

1. INTRODUCTION

Static Synchronous Compensator (STATCOM) is a power electronics-based flexible alternating current transmission systems (FACTS) device extensively used for the purpose of reactive power compensation in the power system. The main component of STATCOM is a voltage source inverter (VSI), which may be of multipulse or multilevel type. For high power applications, multipulse inverter is generally not considered suitable due to the cost, size and complexity of zigzag transformer used for generating multipulse output voltage using basic unit of six/twelve pulse unit [1,2]. As compared to the hard-switched two-level pulse width modulation inverters, multilevel inverters offer several advantages such as their capabilities to operate at high voltage with lower *dv/dt* per switching, high efficiency, low electromagnetic interference etc [1-4]. Apart from being used in STATCOM, the multilevel inverters can provide important applications in distributed energy systems where ac voltage can be obtained by connecting dc sources such as batteries, fuel cells, solar cells, rectified wind turbines etc at input side of the inverters [2-4].

The multilevel inverters are further classified into (i) diode-clamped, (ii) flying capacitors, and (iii) cascade multilevel inverter (CMLI). Among these three, CMLI has a modular structure and requires least number of components as compared to other two topologies; as a result, it is widely used for high power applications [4]. The work presented in this paper uses cascade multilevel inverter for real time application of STATCOM using personal computer (PC) and ADD-ON cards.

2. MULTILEVEL STATCOM OPERATION

2.1 Basics

The basic operating configuration of a STATCOM is given in Figure 1. It consists of a voltage source inverter (VSI), dc side equivalent capacitor (*C*) with voltage v_{dc} on it and a coupling reactor (L_C). The ac voltage difference across the coupling reactor produces reactive power exchange between STATCOM and the power system load bus at the point of common coupling (PCC). If the output voltage of the STATCOM (v_c) is more than the system bus voltage (v_l), reactive power is supplied to the power system and; reactive power goes to STATCOM if

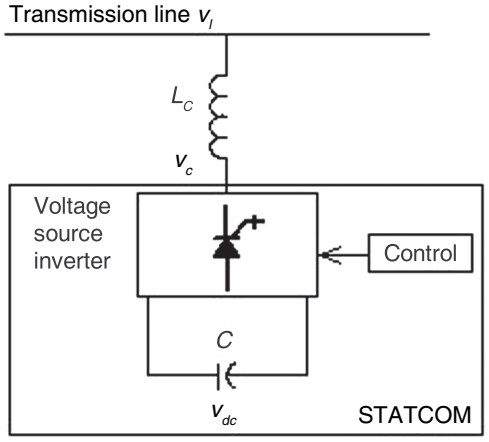

Figure 1: Basic STATCOM configuration.

v_c is less than that of v_l. To take effect of this bidirectional flow of reactive power, the STATCOM output voltage should be varied according to requirement of reactive power compensation, and this can be accomplished in two ways: i) by changing the switching angles of multilevel inverter devices (i.e. varying the modulation index) while maintaining the dc capacitor voltage at a constant level (inverter type I control/ direct control) or ii) keeping the switching angles fixed and varying the dc capacitors voltages (inverter type II control/indirect control) [5]. The variation of dc capacitors voltages is simply achieved by varying the active power transfer between STATCOM and power system by adjusting phase angle difference between v_c and v_l. All these control schemes have their own merits and demerits. In general, inverter type I control is preferred where very fast voltage control is required but THD of v_c varies with modulation index, thereby producing more harmonic distortion in the v_l at low modulation index. On contrary to this, inverter type II operation is slow as ac output voltage of STATCOM varies according to variation of dc capacitor voltages (i.e. presence of capacitor dynamics make the response slow) but harmonic injection in the power system bus voltage can be kept at very low level by operating the inverter at high modulation index where THD of v_c is least.

2.2 Cascade Multilevel Inverter

The CMLI consists of a number of H-bridge inverter units with separate dc source for each unit and is connected in cascade or series as shown in Figure 2. Each H-bridge can produce three different voltage levels: $+V_{dc}$, *0*, and $-V_{dc}$ by connecting the dc source to ac output side by different combinations of the four switches S_1, S_2, S_3, and S_4. The ac output of each H-bridge is connected in series such that the synthesized output voltage waveform is the sum of all of the individual H-bridges' outputs [2-4].

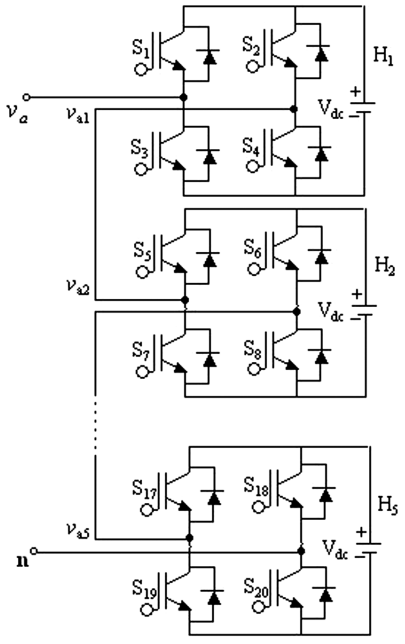

Figure 2: Configuration of single-phase 11-level CMLI.

By connecting the sufficient number of H-bridges in cascade and using proper modulation scheme, a nearly sinusoidal output voltage waveform can be synthesized. The number of levels in the output phase voltage is given as 2s+1, where *s* is the number of H-bridges used per phase. Figure 3 shows an 11-level output phase voltage waveform using five H-bridges, where angles α_1, α_2, α_3, α_4, and α_5 are switching angles of H-bridges H_1, H_2, H_3, H_4, and H_5 respectively. The magnitude of the ac output phase voltage is given by $v_{an} = v_{a1}+v_{a2}+v_{a3}+v_{a4}+v_{a5}$ [3].

2.3 Switching Angles Selection

To synthesize multilevel ac output voltage using different levels of dc inputs, the semiconductor devices must be switched on and off in such a way that desired fundamental voltage obtained is nearly sinusoidal i.e. having minimum harmonic distortions. Different switching techniques are available for computing switching angles for the semiconductor devices [4-6]. For power system applications, generally fundamental frequency switching scheme is considered most suitable; in this scheme the devices are switched on and off once in every cycle, thereby producing less switching losses (more efficiency) [6]. Generally, the switching angles at fundamental frequency are computed by solving a set of nonlinear equations known as selective harmonic elimination (SHE) equations [3-4]. Different approaches, for solutions of these equations, are described in [6-8]. In SHE technique, in general, lower order harmonics are eliminated at the cost of generation of higher order harmonics, thereby increasing the total harmonic distortion (THD) in v_c. In the present work, an optimization technique is used for computation of switching angles which minimize THD due to all harmonic components up to 49th order; as a result,

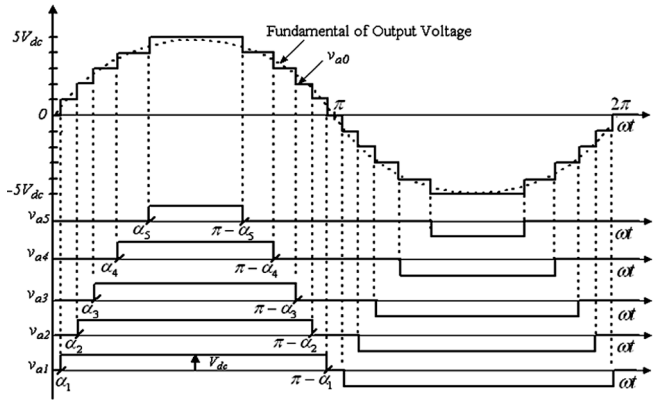

Figure 3: Output voltage waveform of an 11-level CMLI at fundamental frequency switching.

significant amount of THD reduction can be achieved as compared to SHE technique. A detailed discussion of optimization technique is presented in [9] and it can be referred for further detail. Figure 4 shows variation of total harmonic distortion (*THD*) produced in ac output voltage of STATCOM by the switching angles selected using the optimization technique as a function of modulation index (*m*). It is to be noted that, the modulation index (*m*) is defined as the ratio of magnitude of ac output voltage produced to the magnitude of maximum ac output voltage that can be produced (i.e. when all the switching angles are zero) and, in general, the total harmonic distortion (*THD*) in percentage is defined as:

$$THD(\%) = 100 \times \sqrt{\sum_{n=3,5,7,\ldots} V_n^2} / V_1;$$
$$Where\ V_n = 4V_{dc}\left(\cos(n\alpha_1) + \ldots + \cos(n\alpha_5)\right) / n\pi \quad (1)$$

As triplen harmonic components are absent in three-phase line to line voltages, therefore, in this paper *THD* is calculated using all non-triplen odd harmonic components up to 49th order.

2.4 Capacitor Charge Balancing

One major issue associated with CMLI is the problem of maintaining equal voltage across capacitors connected in different H-bridges. The main causes of this problem are: i) continuous power loss in switches and capacitors and ii) conduction duration of each H-bridge is different due to switching of semiconductor devices at different instants [3]. For example, H_1-bridge conducts from α_1 to π-α_1 in positive cycle while H_5-bridge conducts from α_5 to π-α_5 for the same cycle. As a result, charge unbalance on capacitors connected in respective H-bridges is created. To rectify this problem, a switching angle rotational scheme is implemented in which switching angles for H bridges are changed in cyclic order after every half cycle so that average conduction period of each H bridge remains same over five half cycles [3].

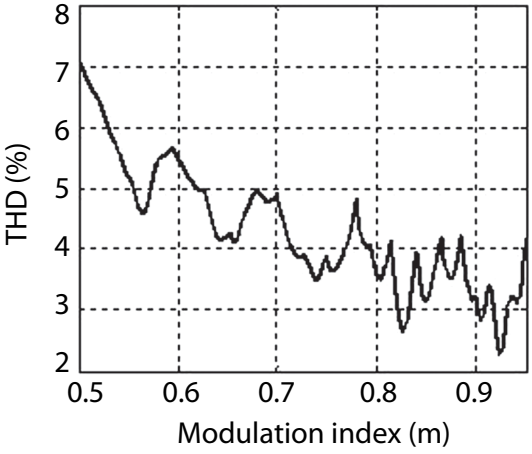

Figure 4: Variation of THD with modulation index for 11-level CMLI.

3. HARDWARE DEVELOPMENT FOR CMLI-BASED STATCOM

The complete configuration for hardware implementation of 3-phase, 11- level cascade multilevel inverter based STATCOM is shown in Figure 5. Although 3-phase configuration is shown in Figure 5, here only single-phase 11-level CMLI based STATCOM is implemented and described. Three-phase implementation can be done just using additional timers and interrupts in similar way as discussed below.

Three-phase inductive load (R_L, L_L) is connected to power system bus through witch *SW1*. An 11-level CMLI is connected to power system bus through a coupling inductor. The STATCOM is connected to or disconnected form power system by switch *SW2*. A zero crossing and quantizer circuit is used to sense zero crossing points and half cycle of load voltage. A voltage sensor and peak detector circuit is used to sense the peak of load voltage. This sensed load voltage is converted in digital form using ADC and is compared with reference voltage (V_{L_ref}) for generating error signal. Firing pulses generated by PC are fed to CMLI through a buffer, a delay and a pulse amplification and isolation circuits for protection and amplification of low voltage pulses generated by PC.

The ADD-ON card (VPC-IOT card) used for the implementation has the following features [10]:

(i) 48 programmable inputs/outputs using two Intel 8255 chips and these are 8255-I and 8255-II
(ii) Six channels of 16-bit down timer/counters using two Intel 8253 chips (8253-I and 8253-II)
(iii) Hardware clock generation for timers/counters

Port A, Port B and Port C of 8255-I are used to issue firing pulses to switching devices S_1-S_{20} through pulse amplifier and isolation circuit as per detail given in Table 1. PCU of 8255-II is used to read the quantized output of quantizer circuit and PCL of 8255-II is used to issue pulses to GATEs of different timers used. Actual configuration of times and interrupts is shown in Figure 6 for single-phase implementation of cascade multilevel STATCOM. For three-phase implementation two additional timers and interrupts are required.

Table 1: Details of firing pulses

Firing bit	PA_0	PA_1	PA_2	PA_3	PB_0	PB_1	PB_2	PB_3	PC_0	PC_1
Switch no.	S_1, S_3	S_2, S_4	S_5, S_7	S_6, S_8	S_9, S_{11}	S_{10}, S_{12}	S_{13}, S_{15}	S_{14}, S_{16}	S_{17}, S_{19}	S_{18}, S_{20}

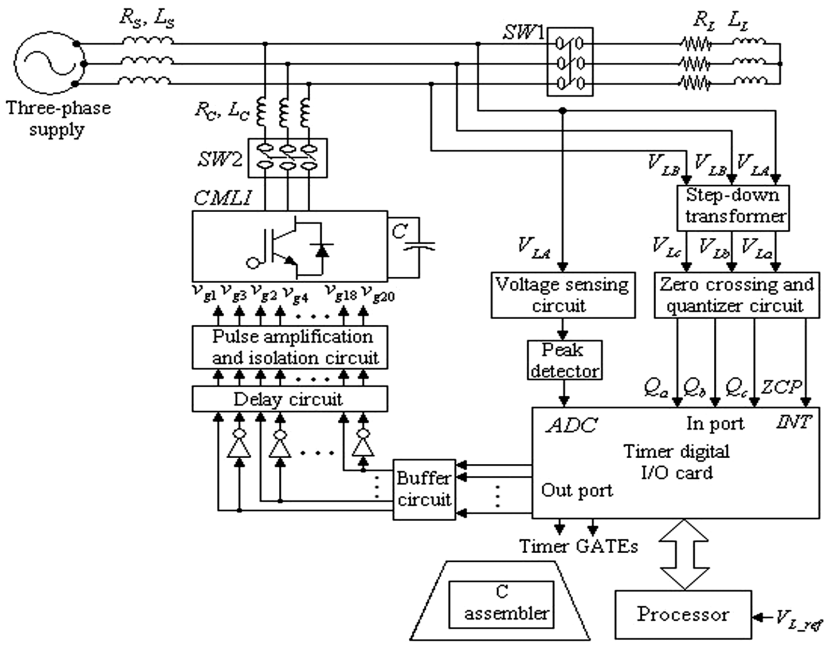

Figure 5: Hardware implementation configuration for 11-level cascade multilevel STATCOM.

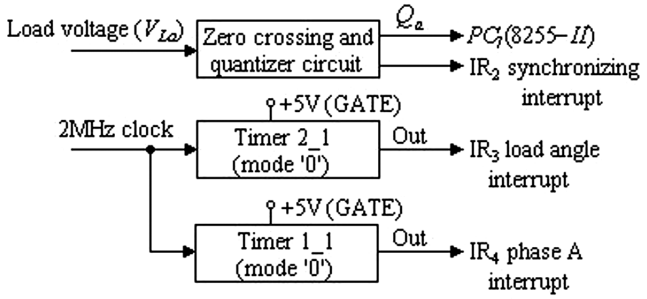

Figure 6: Timers and interrupts arrangement for hardware implementation.

4. SOFTWARE DEVELOPMENT FOR CMLI-BASED STATCOM

Control signals for the STATCOM are generated using system software developed using C language. It consists of main program, interrupt service subroutines (ISSs), ADC subroutine, error subroutine and PI processing subroutine. In main program, all initialization tasks, inputting constants, defining different variables etc. are included. The flow chart for main program is given in Figure 7. Flow charts for ADC subroutine and error processing are shown in Figures 8 and 9 respectively. Schematic diagrams for direct and indirect control schemes for software development are presented in Figure 10, while corresponding flow charts for PI processing are shown in Figures 11 and 12. Load angle thus obtained by PI processing of indirect control is loaded in Timer 2_1 (mode '0' operation) at zero crossing of load voltage (as indicated by IR_2 synchronizing interrupt). On terminal count, Timer 2_1 generates IR_3 interrupt, and on occurrence of IR_3

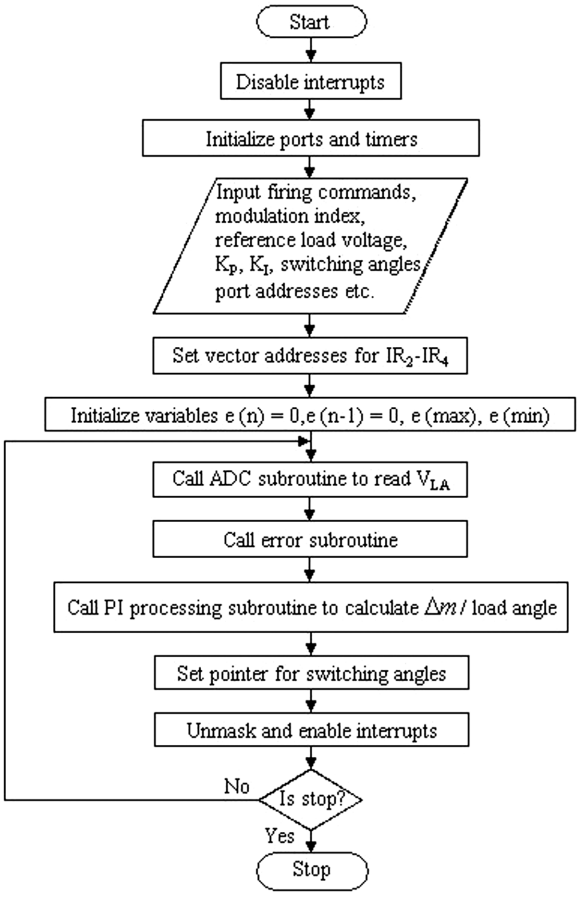

Figure 7: Flow chart for main program.

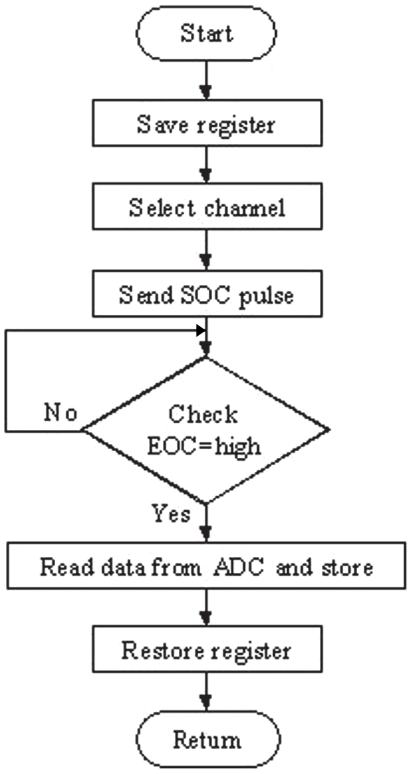

Figure 8: Flow chart for ADC subroutine.

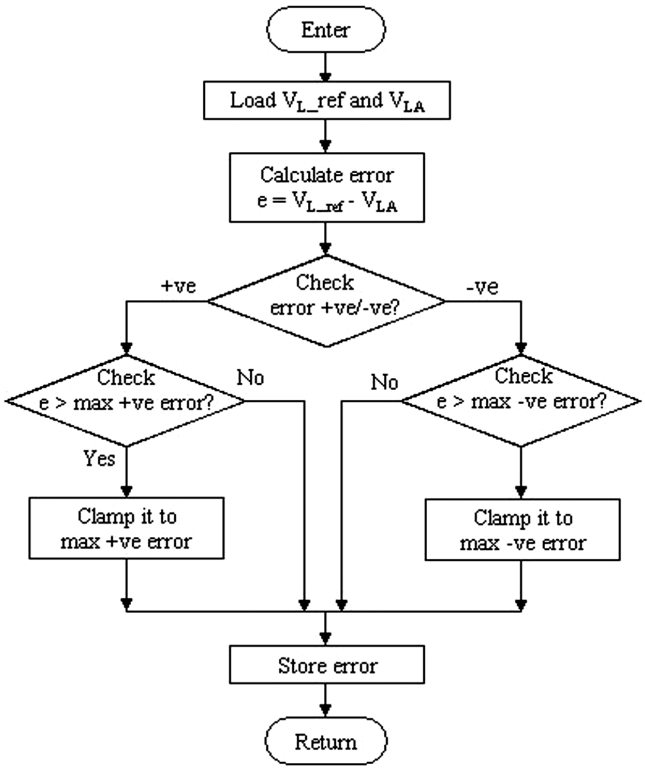

Figure 9: Flow chart for error subroutine.

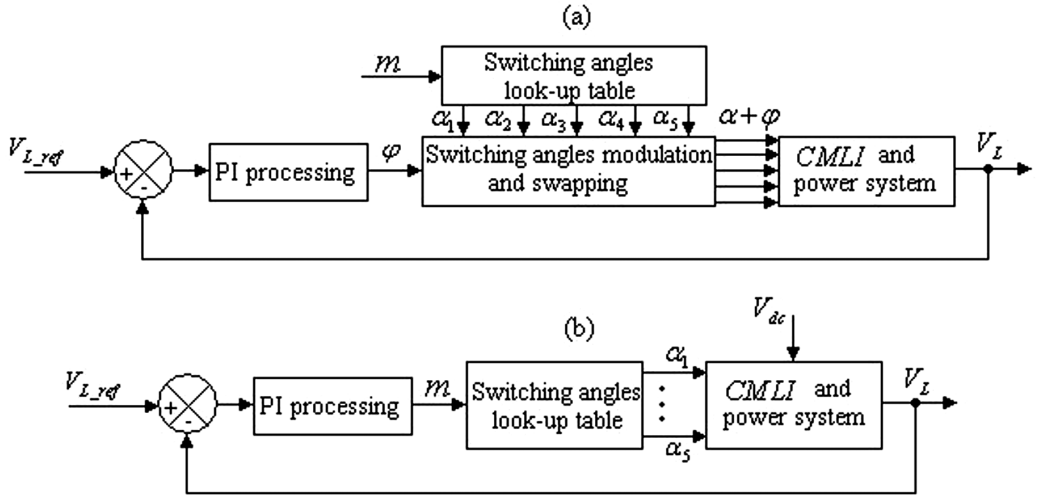

Figure 10: (a) Indirect control scheme and (b) Direct control scheme.

interrupt, first switching angle is loaded in Timer 1_1 (mode '0' operation) as discussed in flow charts given in Figures 13-15. In case of direct control, Timer 2_1 is not loaded, instead Timer 1_1 is loaded with first switching angle similar to indirect control scheme on occurrence of synchronizing interrupt and simultaneously all firing bits are reset for positive or negative cycle as the case may be. First firing pulse is issued on terminal count equivalent to α_1 when 'IR_4 phase A interrupt' occurs, subsequent firing pulses are issued on terminal count of α_2-α_1, α_3-α_2 … α_2-α_1, α_1 on repeated occurrences of 'IR_4 phase A interrupt'. On completion of positive half cycle synthesis, again at zero crossing, synchronizing interrupt occurs and firing pulses are issued for synthesis of negative half cycle (negative firing commands are issued). This way a complete cycle is synthesized.

5. EXPERIMENTAL RESULTS

To investigate the performance of 11-level cascade multilevel STATCOM, a prototype model is developed by taking 5 H-bridges per phase connected in cascade

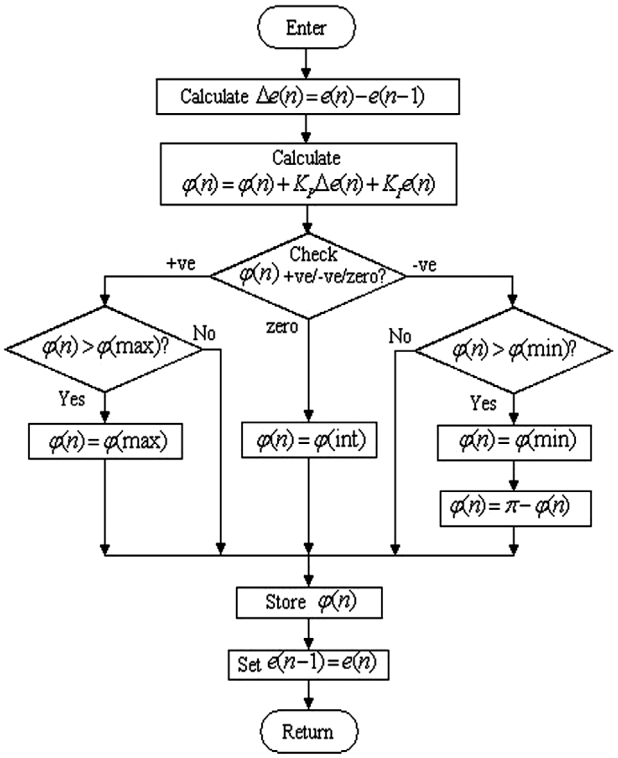

Figure 11: PI processing for indirect control.

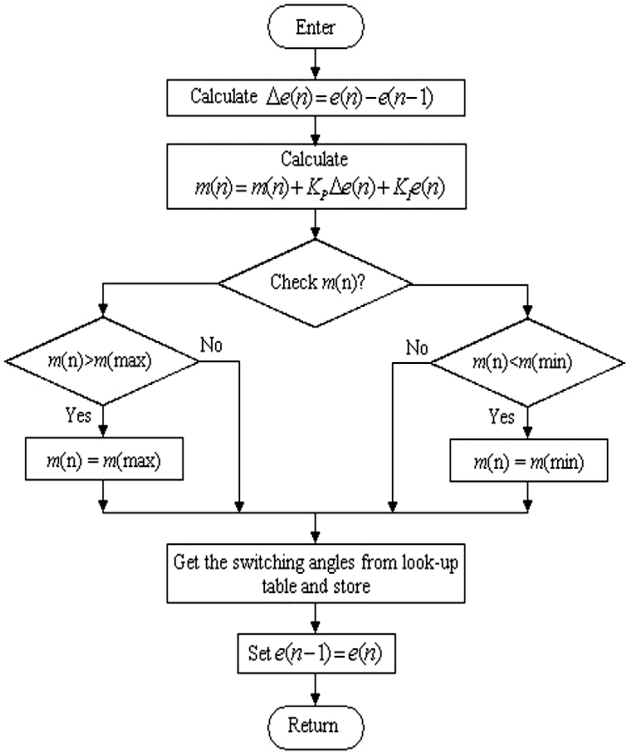

Figure 12: Direct control PI processing flow chart.

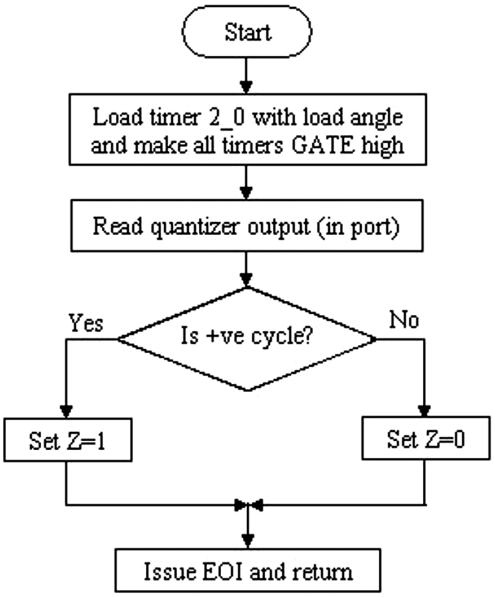

Figure 13: Flow chart for synchronizing interrupt.

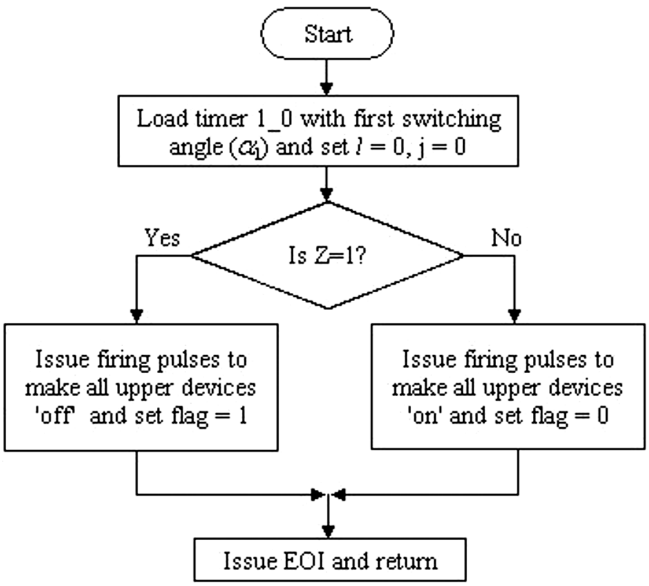

Figure 14: Flow chart for load angle interrupt.

and dc capacitors are used as dc source for each of H-bridges. Switching device selected is MOSFET IRF740 (400V, 6A). Values of power system parameters, coupling inductor and dc link capacitors are selected according to [1] and are given in Table 2. Firing pulses are issued to switching devices as per Table 1. It is to be noted that one port bit issues two firing pulses (original firing pulse and its complement) through delay circuit to the devices connected in same leg of an H-bridge i.e. the upper and lower devices.

5.1 Indirect Control Scheme

As discussed in Section II, in this scheme, the modulation

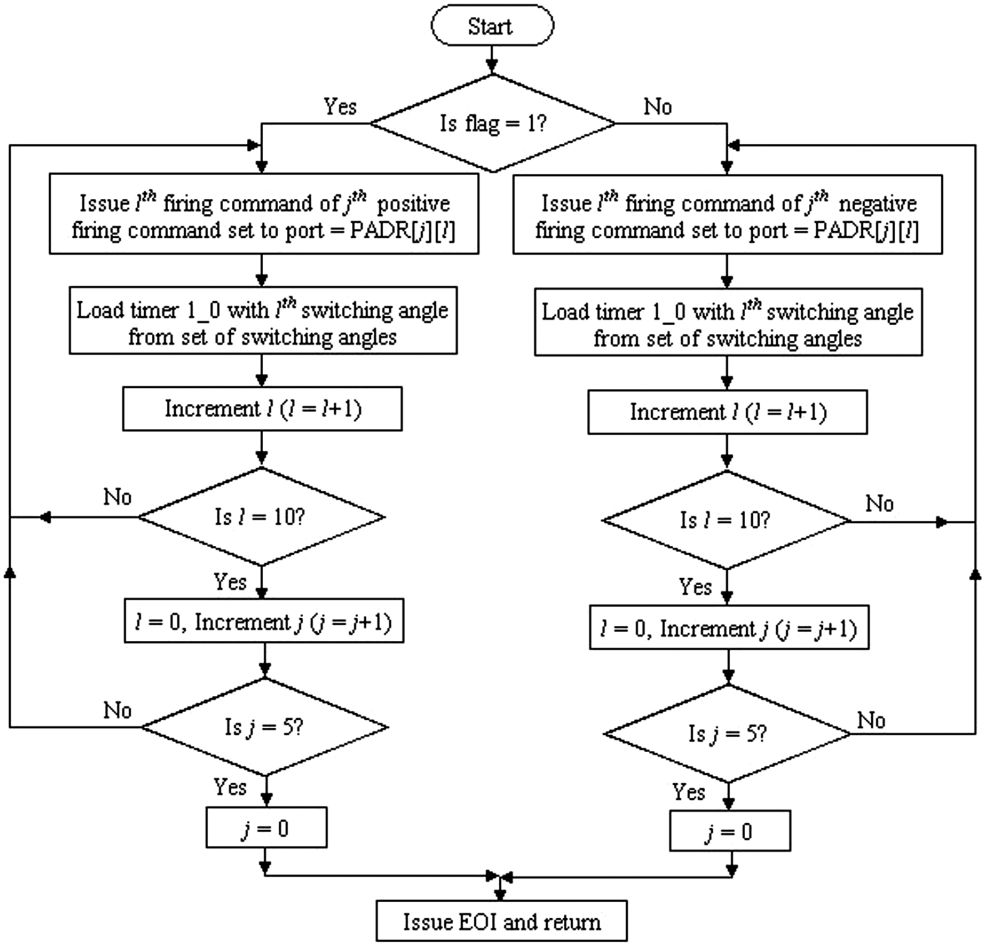

Figure 15: Flow chart for phase A interrupt.

Table 2: Parameters of STATCOM and power system

System voltage	100 V (peak) per phase
Inductive load	750 VA
Current rating	3.53 A
Series inductance, L_s	3.38 mH
Coupling inductance, L_c	16.85 mH
DC capacitor for each H-bridge	1000 μC
Modulation index (m)	0.9240 (indirect control)
	0.7000 (normalized value for direct control, V_{dc} = 32V)

index is kept constant while variation in output ac voltage of STATCOM is achieved by charging or discharging of capacitors by phase shifting of STATCOM voltage with respect to load voltage. Figure 16(a) demonstrates the synthesis of an 11-level voltage waveform while Figure 16(b) explains phase difference produced between the STATCOM voltage and load voltage for active power flow in order to charge capacitors at m = 0.9240. In Figure 17, load voltage, STATCOM current, STATCOM voltage and load current variations are shown before and after compensation. It can be seen from Figure 17 that initially when load is not connected, magnitude of load voltage remains constant while STATCOM is in floating mode. As soon as an inductive load is connected to power system, load voltage drops momentarily, and this drop in load voltage initiates control action producing phase difference (lag) between the STATCOM voltage and the load voltage, therefore STATCOM output voltage increases (due to more charging of capacitors), hence load voltage is restored at its nominal value due to flow of reactive power as discussed in Section II (principle of STATCOM operation).

5.2 Direct Control Scheme

Direct control scheme is implemented by varying modulation index in order to get variation in output voltage of STATCOM while keeping capacitor voltage constant. Figure 18 shows 11-level voltage waveform synthesized using single phase 11-level CMLI at two extreme operating values of modulation indices. Variations of load voltage, source current, load current and STATCOM current are shown in Figure 19 when STATCOM is connected to power system while load

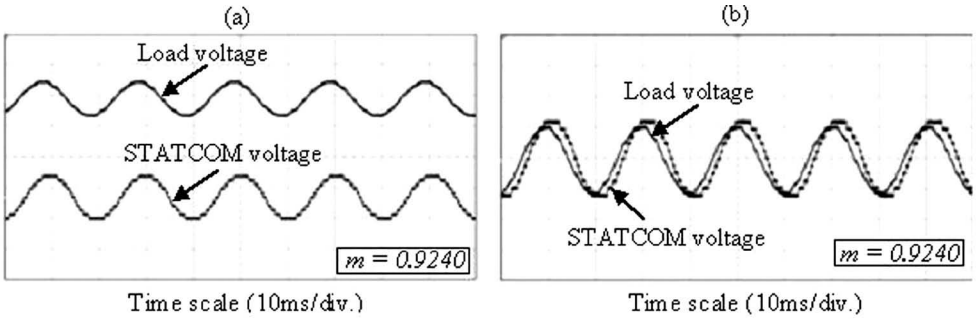

Figure 16: Load and STATCOM voltages (a) in phase (b) STATCOM voltage lags load voltage.

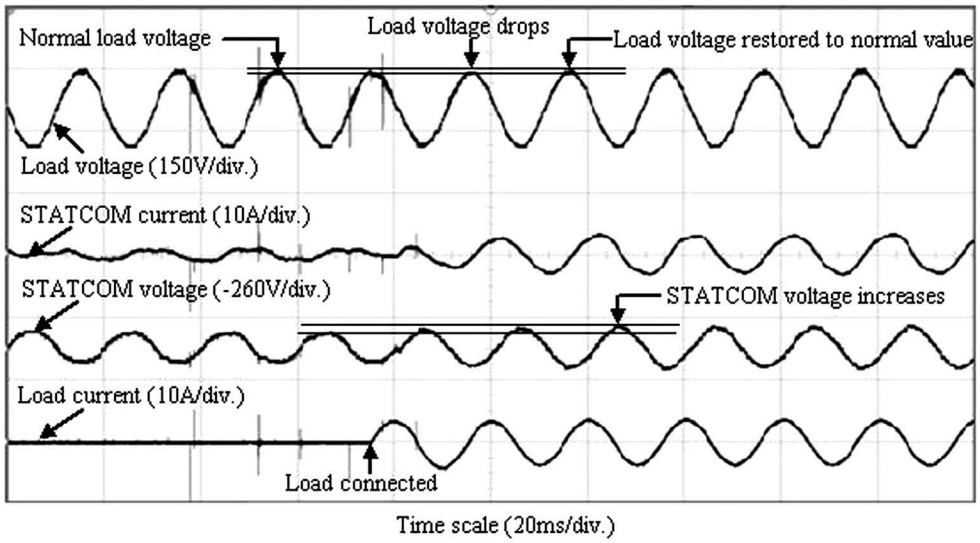

Figure 17: Variations of load voltage, STATCOM current, STATCOM voltage and load current when inductive load and STATCOM is connected at load bus (indirect control).

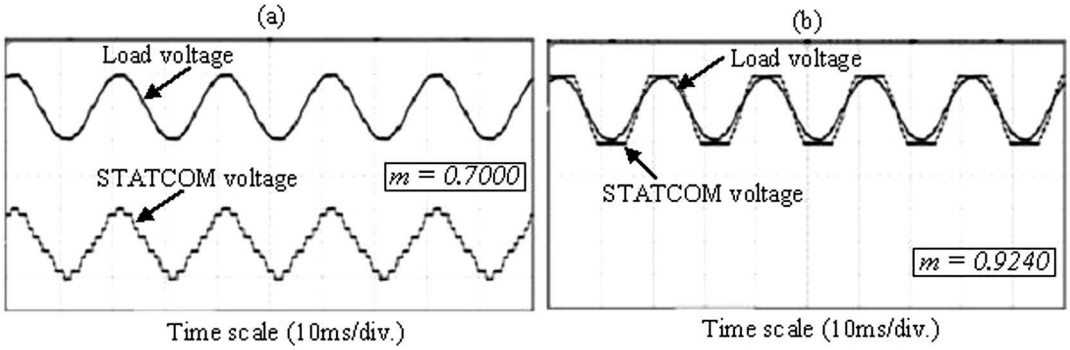

Figure 18: Generated 11-level STACOM phase voltage at different modulation indices.

was already connected. It can be seen from Figure 19 that due to presence of inductive load, load voltage is less than the reference value and this difference (error) is processed through PI controller which increases *m*, hence increasing STATCOM output voltage. This increased STATCOM output voltage injects reactive power to the power system hence normalizing load bus voltage to its nominal value. As compared to indirect control scheme, direct control scheme is faster due to the absence of capacitors dynamics. It may be noted that single phase 11-level voltage waveforms generated as shown in Figs. 16 and 18 contain triplen harmonic components because

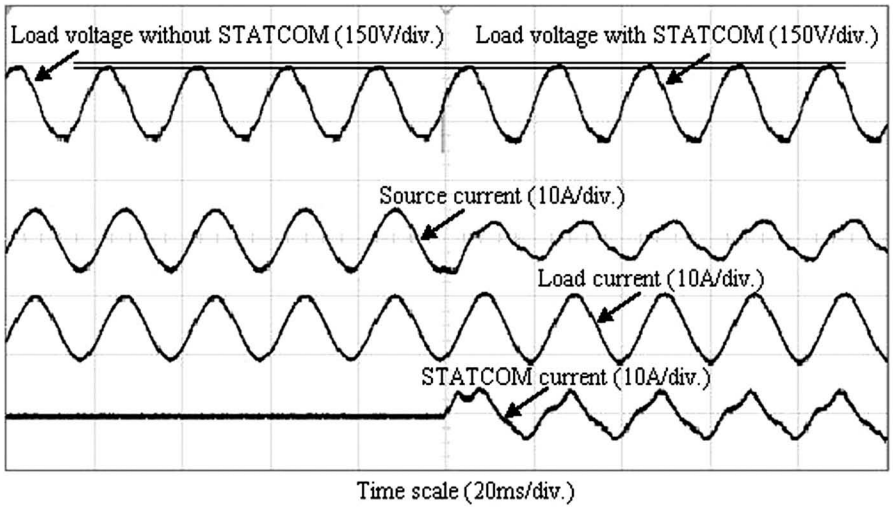

Figure 19: Variation of load voltage, source current, load current and STATCOM current with and without STATCOM connected to power system (direct control).

switching angles have been chosen to minimize non triplen odd harmonic components only as required for three-phase operation.

6. CONCLUSION

The personal computer-based voltage control scheme presented in this paper for cascade multilevel inverter-based STATCOM is a simple and effective method for load voltage regulation. Results presented here validate the basic principle of STATCOM for voltage regulation applications. Although, in this work, only single-phase 11-level CMLI based STATCOM has been employed the same procedure can be easily extended for a three-phase system as well as higher level CMLI-based STATCOM.

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