Design of Subthreshold Wide Band Down Conversion Mixer

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***Abstract*—In this paper, a subthreshold driven low power wide band Gilbert cell mixer in two different architectures is presented. The first is Common Source (CS) architecture with RC degeneration for bandwidth extension and capacitive cross coupling for gain boosting. Next is a conventional Common Gate architecture driven in weak inversion region for low power consumption. Both architectures are designed to work for Ultra Wide Band (UWB) applications (2GHz to 8GHz). From the simulation results, the CS topology provides 10dB (including 6dB loss in buffer) conversion gain over same bandwidth while consuming 1.38mW DC power from 1.8V supply. On the other hand, the CG topology provides 13.5dB (accounting 6dB loss in buffer)conversion gain over the same bandwidth while consuming 2.51mW DC power from 1.8V supply. The achieved input referred 1dB compression points are -11dBm for CS and -7dBm for CG topologies. Simulated performance on PVT variation and layout extraction are closely follow with the original design performances.**

I. Introduction

The emerging various wireless communication systems promote the necessity to design a single receiver capable of performing on multiple standards. This proves a way for exploring wideband receivers for a variety of application. Complementary metal oxide semiconductor (CMOS) technology would be the best choice for wireless applications, such as GSM, WLAN, or Ultra Wide-Band (UWB) systems, provided it can meet overall system specifications, generally attributed to its lower cost, lower power, and higher level of integration with base band circuits.

The primary building blocks in a wireless receivers are low noise amplifier, mixer and IF amplifier. One of the key components in the receiver chain (RX) is the down-conversion mixer. The mixer is a vital block to perform the frequency translation in wireless systems. The main challenge in the mixer design to optimize all the performances like, conversion gain, linearity and noise figure, bandwidth simultaneously. Compared to traditional narrow-band systems, design of UWB receiver building blocks are quite different and challenging. Additionally to UWB, with its operational frequencies ranging from 2G to 10GHz, covering frequencies down to 50MHz will result in a multi-standard design being able to operate within the most important wireless standards like wireless sensor network, Bluetooth, Wibree, Zigbee, Wi-Fi etc.

Several topologies of CMOS down conversion mixer deign have been proposed for wide-band operation [1]-[4]. One of the most famous topology is active mixer based on Gilbert cell topology. This active topology is favored over passive circuits due to its conversion gain (CG), which relaxes gain and noise requirements on the preceding low-noise amplifier (LNA) and subsequent base band stages, respectively. On the other hand, the Gilbert-cell mixer usually suffers from large DC power dissipation and the need for high supply voltages to drive multiple stacked devices (three stages: RF input, local oscillator (LO) switching, IF load). To achieve wide band gain, RC source degeneration technique is used in [5] which is implemented in bipolar technology. A low power design technique for a single band mixer is proposed in [6].

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In this paper, we propose a RC degeneration and capacitive cross coupling technique and a common gate topology which are biased in subthreshold region to achieve higher gain, bandwidth and lower DC power consumption. Rest of the paper is organized as follows. Section II briefs the CS Gilbert cell mixer design. Section III describes the proposed CS wide band mixer design and Section IV explains the details of CG mixer design. Simulated and Extracted results are discussed in Section V.

II. Gilbert Cell Mixer Design and Methodologies

The main challenge in active mixer design is optimizing conversion gain, linearity, and noise performance simultaneously. All three characteristics are related to the RF transconductance stage. The conversion gain and linearity in terms of input referred intercept point (IIP3) can be expressed as follows [7]:

$$Conv.Gain = \frac{2}{\pi} g_m R_L \tag{1}$$

$$IIP_3 = 4\sqrt{\frac{2I_{DC,RF}}{3K_{RF}}} \tag{2}$$

where $2/\pi$ is the factor for a square LO signal and R_L is the load resistor. $K_{RF} = 2\mu_n C_{ox} W/L$ is a process parameter, including the carrier mobility μ , the gate oxide capacitance C_{ox}, as well as the width W and the length L of a transistor. I_{DC} and $g_{m,RF}$ are the bias current and the transconductance of the RF input stage, respectively. These equations suggest that increasing the bias current improves the mixer performance, but the voltage drop across the load resistor is also increased, which, in turn, reduces the available voltage headroom at the output of the mixer for a fixed supply voltage, thereby deteriorating the switching action and the whole mixer performance. Reducing the value of the load resistor, to keep the biasing voltage at the drain of the switches constant, will decrease the conversion gain.

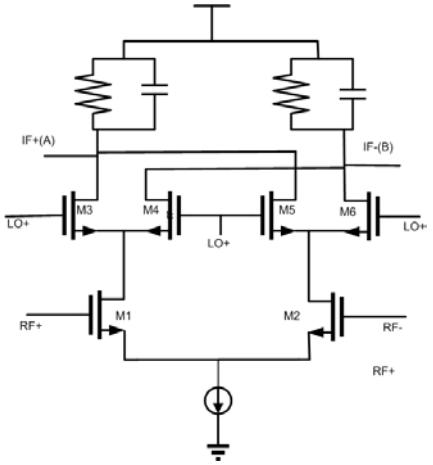

Fig. 1. Conventional Gilbert Cell Down Conversion Mixer.

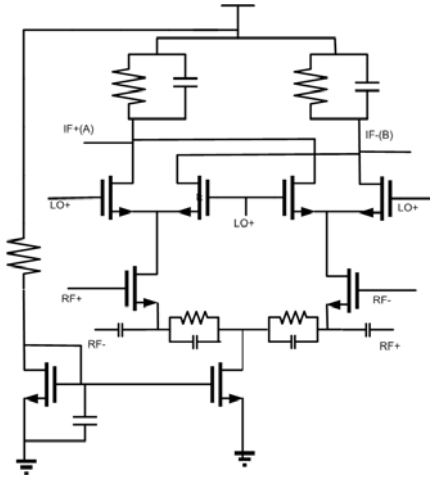

Fig. 2. Proposed Mixer with Bandwidth Extension Technique

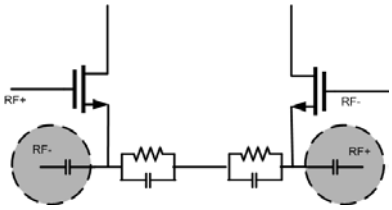

Fig. 3. Down Conversion Mixer with Cross Coupling

The CMOS active mixer is based on Gilbert cell core. The Gilbert cell configuration is selected for its double balanced implementation which offers high conversion gain and improved spur performance in a very compact size as shown in Fig. 1. The RF signal enters from the source coupled pair (M1-M2). The LO signal enters the upper cross coupled quad of devices (M3-M6). The circuit is biased from a tail current source. The transconductance stage converts the input voltage signal at the RF frequency into a current signal. The switching quad then ideally multiplies this current at the rate of the LO signal, thus enabling the wanted frequency conversion. The output current signal at the IF frequency from the switching quad is finally converted into a voltage signal by the load circuit. Neglecting any device parasitics, the voltage conversion gain of the Gilbert cell mixer is given as in (1).

III. Wide Band CS Mixer Design

The schematic of proposed wide band low power active mixer biased is shown in Fig.2. The transconductance MOS transistors are biased in subthreshold region to attain very low power consumption. The mixer core (LO pair transistor) consists of the four switching transistors and RF pair consists two transistor. RF pair is biased lower than the threshold voltage. The Gilbert cell employs emitter degeneration R and C for the transconductance stage. Resistive and capacitive degeneration in the transconductance stage allows a significant extension of the RF bandwidth [5]. This is, however, at the expense of reduced conversion gain because, effective transconductance will get reduced as given in equation (3).

$$g_{m,eff} = \frac{g_m}{1 + g_m(R||C)} \tag{3}$$

To overcome the gain degradation due to the degeneration, capacitive cross coupling is introduced in RF pair which is shown in Fig. 3. This will effectively increase the transconductance of the RF stage, so that the overall gain of down conversion mixer is increased. One issue, is that the cross-coupled capacitance is required to be much larger than the parasitic capacitance between the gate and the source for the transistor. Otherwise, it could degrade the noise factor and input matching.

IV. Design of Common Gate Mixer

The differential common source (CS) Gilbert mixer cell, illustrated in Fig. 1, has been the most popular structure due to its better performance and isolation characteristics. However, performances of Gilbert mixer are mainly dependent on its large voltage swing. This is because, multiple devices stacked on single DC path which makes the voltage headroom very minimum. Hence, getting larger output voltage swing and so better linearity from conventional CS Gilbert cell is a difficult task. On the other hand, the common gate (CG) structure shown in Fig. 4 has the capability to achieve better linearity than the CS structure. As the current drawing in the input stage dominates conversion gain and noise figure, the CG can be very attractive option where DC power consumption is not a concern.

Mixing is achieved by exploiting the non-linear exponential characteristics of subthreshold transistors by applying RF signal at the gate and LO signal at the source. Using the second-order term from the Taylor series expansion of the exponential in the subthreshold device equation, the conversion gain of this mixer is given in equation (4) [6]. The LO signal swing required in this architecture is considerably low which helps in significant power savings in the LO generation blocks too.

$$Conv.Gain = \left(\frac{W}{L}\right)_{MRF} I_{D0} \left(\frac{1}{n\left(\frac{kT}{q}\right)}\right)^2 v_{LO} \left(\frac{2}{2g_{ds3} + \frac{1}{R_L}}\right) \tag{4}$$

The optimum input matching can be achieved by selecting

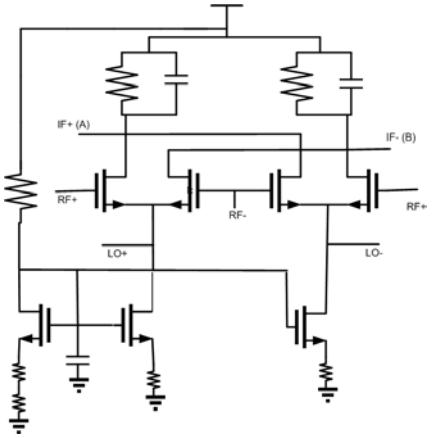

Fig. 4. Common Gate Mixer Circuit

TABLE I. VARIOUS PERFORMANCE PARAMETER OF COMMON SOURCE TOPOLOGY WITH RF INPUT MATCHING

Parameters	After Mixer	After SF Mixer	After Balun
Gain @2.45 GHz RF	9.5 dB	5 dB	4 dB

appropriate values of R,L,C in way done for CS.

V. SIMULATION AND EXTRACTION RESULTS

CS and CG Gilbert cell mixer architectures are simulated with input matching at RF input,source follower buffer and off chip balun at the output using in UMC 180nm technology. All simulation results shown below are after source follower and balun. Wideband down conversion CS and CG operates at 1.8V power supply and consumes 1.38mW and 2.51mW respectively. Figure 5 and 10 shows that these circuits achieved $3 \pm 1dB$ and $7.5 \pm 1dB$ conversion gain for CS and CG respectively. S_{11} response of CS and CG mixer are shown in Fig. 6 and 11 and is less than -10dB over the frequency range of 2GHz to 8GHz in both circuits. Figure 7 and 12 shows noise figure 18.5dB and 14dB at 50 MHz IF frequency. Figure 8 and 13 shows input referred 1dB compression were at -11dBm and -7.5dBm.

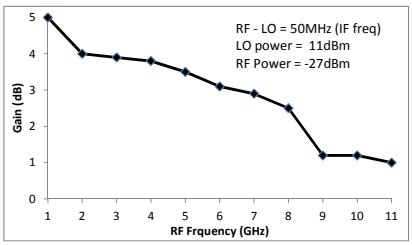

Fig. 5. Conversion Gain CS Mixer over vs RF Frequency

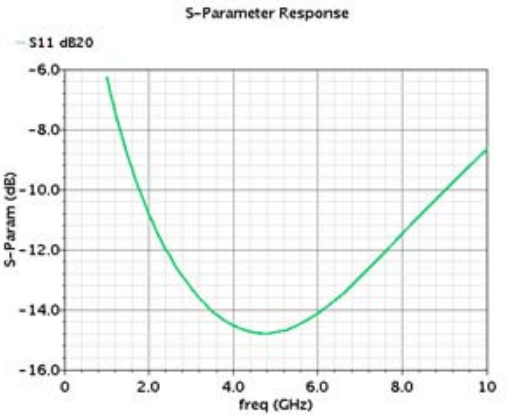

Fig. 6. S11 Plot at RF Input in CS Mixer

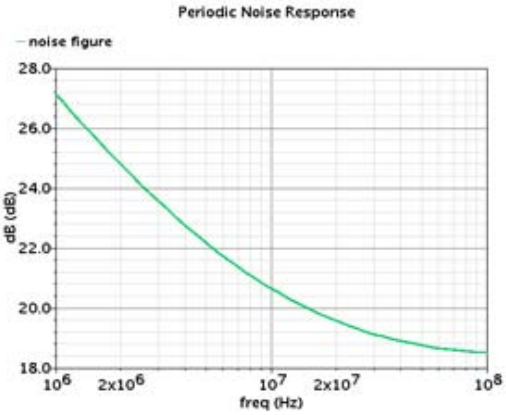

Fig. 7. Noise Figure Plot of CS Mixer over IF Frequency

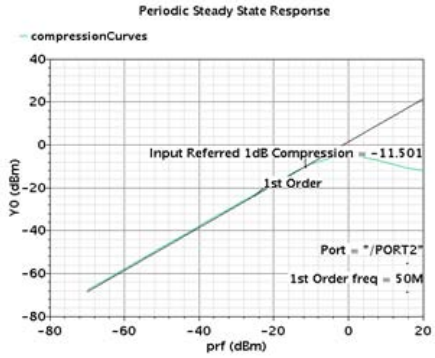

Fig. 8. Gain Compression Plot in CS Mixer

TABLE II. PERFORMANCE PARAMETERS AFTER EXTRACTED SIMULATION

Parameters @2.45 GHz RF	After Mixer
Gain	7 dB
Noise Figure	15 dB
CP_{1dB}	-16.8 dBm

VI. CONCLUSION

In this paper, a modified method for bandwidth extension and capacitive cross coupling in CS Gilbert cell mixer and a CG mixer in subthreshold region bias are proposed. The DC power consumption is greately reduced in both the architectures as well as higher bandwidth (2Ghz to 8GHZ) is achieved. Both the circuits are implemented in UMC 180nm RFCMOS

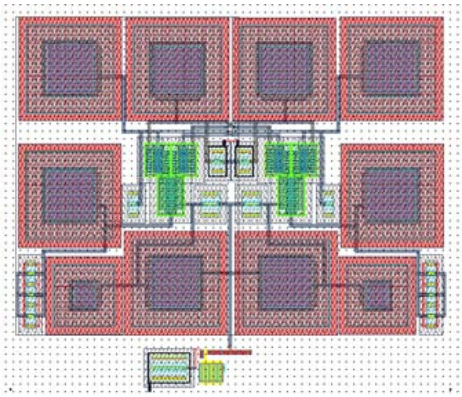

Fig. 9. Die Layout of Proposed CS Mixer Circuit

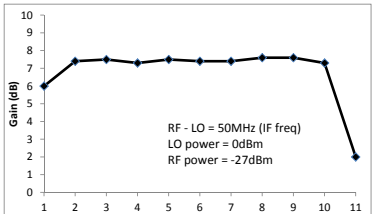

Fig. 10. Conversion Gain of CG Mixer over RF Frequency

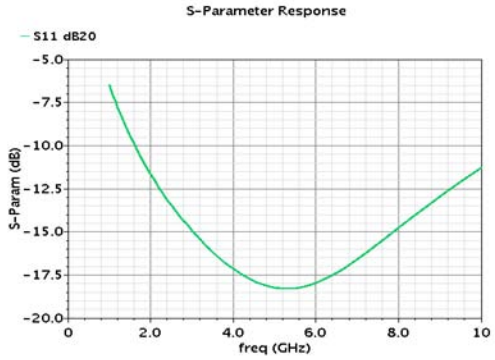

Fig. 11. S11 plot at RF input of CG mixer

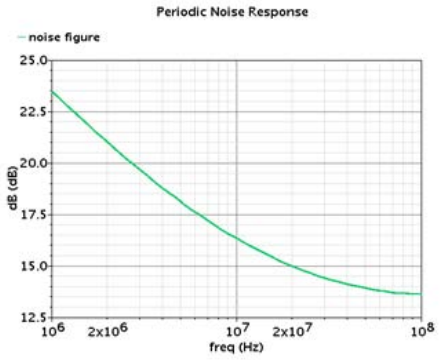

Fig. 12. Noise Figure Plot of CG Mixer

technology. CS mixer consumes 1.38mW and CG mixer consumes 2.51mW power from 1.8V supply respectively. Among

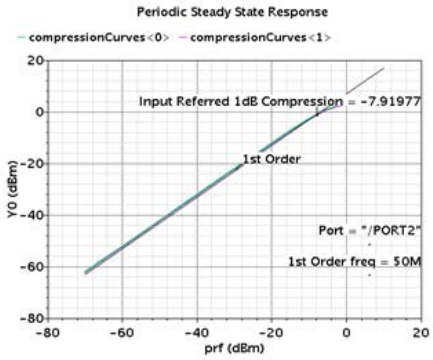

Fig. 13. Gain Compression Plot of CG Mixer

TABLE III. COMPARISON OF CS AND CG PERFORMANCES

Topology	Common Gate	Common Source
Conversion Gain	7.5 dB	4 dB
Noise Figure	14 dB	18.5dB
DC Power	2.51mW	1.38mW
Input Matching	<-12 dB	<-11 dB
CP_{1dB}	-7.9 dBm	-11.5 dBm

the two architectures, CG topology shows better performance at the cost of increased DC power consumption. The proposed circuits will be useful in low power applications like wireless sensor networks.

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