Superior Work Function Variability Performance of Horizontally Stacked Nanosheet FETs for Sub-7-nm Technology and Beyond

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Abstract—In this paper, work function variability (WFV) of stacked nanosheet FET (NSHFET) has been numerically investigated using 3-D quantum corrected Drift-Diffusion simulation framework for sub-7nm high performance logic applications. The WFV induced NSHFET performance is investigated using RGG (ratio of average grain size to gate area) plot for fair comparison against nanowire FET (NWFET) as the effective grain size ($G_{size,eff}$) is smaller than actual grain size (G_{size}). From RGG plot analyis, it is found that NSHFET shows better immunity towards WFV induced V_T variation by 15% compared to NWFET. The V_T variation due to WFV is decreased by 40.47% and 29.16% for 3-stacked NSHFET and NWFET respectively compared to single stack devices. NSHFET exhibits lesser WFV induced OFF-current (I_{OFF}) variation by 57.46% compared to NWFET. NSHFET shows better WFV induced threshold voltage mismatch index ($A_{VT}=0.7mV.\mu m$) compared to NWFET ($A_{VT}=1.2mV.\mu m$).

Index Terms—NSHFET, NWFET, RGG, WFV.

I. INTRODUCTION

For sub-7nm technology node, gate-all-around (GAA) Nanowire FETs (NWFET) are promising candidate compared to FinFET technology node due to their better gate electrostatic control and immunity to short channel effects [1], [2]. However, to improve the layout efficiency and drive current of NWFET, stacked nanowire FETs are used [3]. Moreover, stacked nanosheet FETs (NSHFET) has emerged as better candidate for future sub-7nm technology node due to its better electrostatic integrity, short channel immunity, more effective width per footprint and better power performance [4]–[6].

High-k/metal gate technology for NSHFET has improved gate capacitance and reduced gate leakage current. However, device performance gets degraded by the metal gate granularity (MGG) in metal gate, which leads to work function variability (WFV) [7]. WFV has been emerged as one of the major random device fluctuations among non planar devices such as FinFET, NWFET etc [8]–[11]. WFV is one among the major variability sources such as Line Edge Roughness (LER), Random Dopant Fluctuations (RDF) and Metal Gate Granularity (MGG) [12], [13]. In earlier literature, WFV on NWFETs have been numerically investigated [8], [9]. However, the WFV impact on stacked NSHFETs has not been
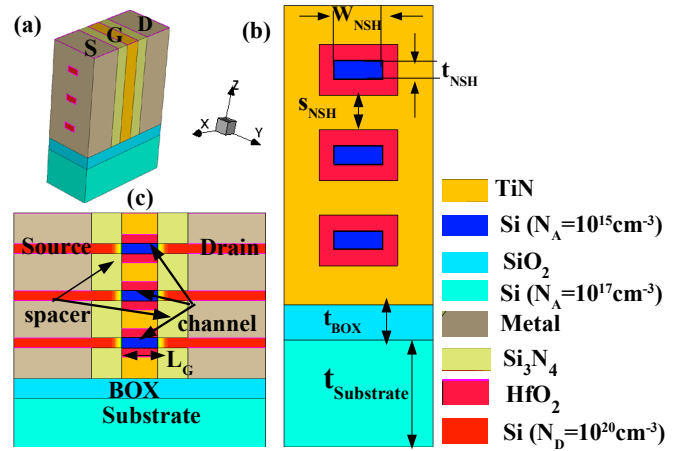

Fig. 1. Schematic diagram of 3-stacked NSHFET: (a) bird eye view; (b) cross-sectional view across the channel; (c) cross-sectional view along the channel.

investigated in detail. In this work, we are investigating the WFV of NSHFET & NWFET using RGG (ratio of average grain size to gate area) to take into account of gate area and grain size of metal gate surface [9], [14]. The impact of WFV on NSHFET & NWFETs of different stacks are also studied.

II. DEVICE STRUCTURE & SIMULATION METHODOLOGY

The device structure schematic of 3-stacked nanosheet transistor (NSHFET) is shown in Fig.1. The NSHFET structural simulation parameters are listed in TableI. TiN gate metal and HfO$_2$ gate dielectric of thickness (t_{ox}) 4.5nm are considered. For comparative study of WFV, NWFET of width (t_{NS}) of 5nm is used. Sentaurus TCAD tool is used for the analysis of our target device structure [15]. Quantum corrected 3-D drift-diffusion transport model is considered for our device simulation. Density Gradient model for quantum correction, Shockley Read Hall model for recombination and generation and Oldslotboom model for bandgap narrowing are considered. Calibrated mobility models such as High Field Saturation, Enormal, coulomb scattering and
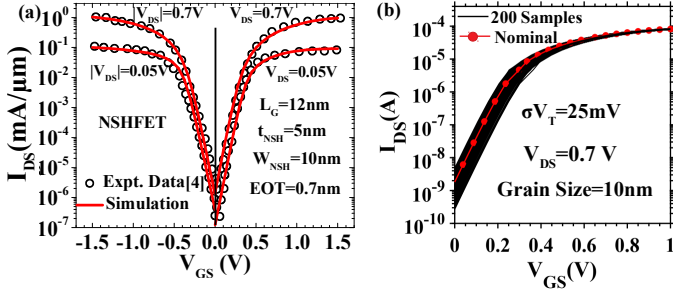
Fig. 2. (a) Calibration of simulation transfer characteristics of stacked NSH-FET with experimental data [4] (b) simulated input transfer characteristics due to WFV for 200 random device samples.

TABLE I
STRUCTURAL PARAMETERS USED FOR NSHFET.

Parameter Name	NSHFET
Gate Length (L_G)	12 nm
Nanosheet Width (W_{NSH})	10 nm
Nanosheet Thickness (t_{NSH})	5 nm
Nanowire Thickness (t_{NS})	5 nm
S_{NSH}	8 nm
EOT	0.7 nm
BOX thickness (t_{BOX})	20
Substrate thickness ($t_{substrate}$)	30
Channel doping (N_{CH})	1×10^{15} cm^{-3}
Source/Drain doping ($N_{S/D}$)	1×10^{20} cm^{-3}
Substrate doping (N_{Sub})	1×10^{17} cm^{-3}
Work Function	4.38eV

Inversion and Accumulation Layer (IAL) mobility are considered for our simulation. Our simulation parameter calibration efforts involve the reproduction of NSHFET experimental transfer characteristics [4] (Fig.2(a)). Both experimental (DIBL=32mV/V; SS=75mV/dec) and numerically simulated NSHFET (DIBL=36mV/V; SS=77mV/dec) show a close matching characteristics.

III. RESULTS AND DISCUSSION

To analyse the work function variability of the device, TiN metal gate of two different grains of orientation <100> and <111> with probability of occurrence 0.6 and 0.4 respectively with a workfunction difference of 0.2eV are considered [7]. Fig.2(b) shows the simulated transfer characteristics of 3-stacked NSHFET due to WFV for an average grain size of 10nm. For statistical analysis of WFV, we are considering 200 different device samples. The statistical threshold voltage variation of NSHFET for linear (V_{DS}=0.05V) and saturation regime (V_{DS}=0.7V) are shown in quantile plot (Fig.3(a)). The 3-stacked NSHFET shows WFV induced threshold voltage variation of 24 & 25 mV in linear and saturation region respectively. Work function variation due to randomized work function values for grain of 10nm size are shown in Fig.3(b). In NWFET, the effective grain size ($G_{size,eff}$) will be the projection of actual metal gate grain size (G_{size}) onto the channel region through gate dielectric material [9]. Therefore $G_{size,eff}$ will be smaller compared to G_{size} for smaller diameter NWFET. A comparative analysis of metal work function
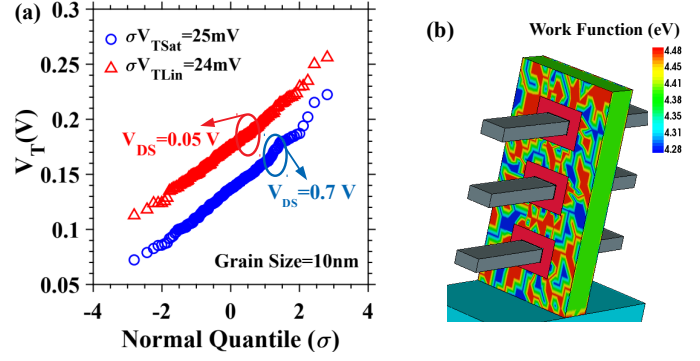

Fig. 3. (a) Quantile plot of threshold voltage variation for linear and saturation regime for an average grain size of 10nm (b) work function variation contour plot of 3-stacked NSHFET.
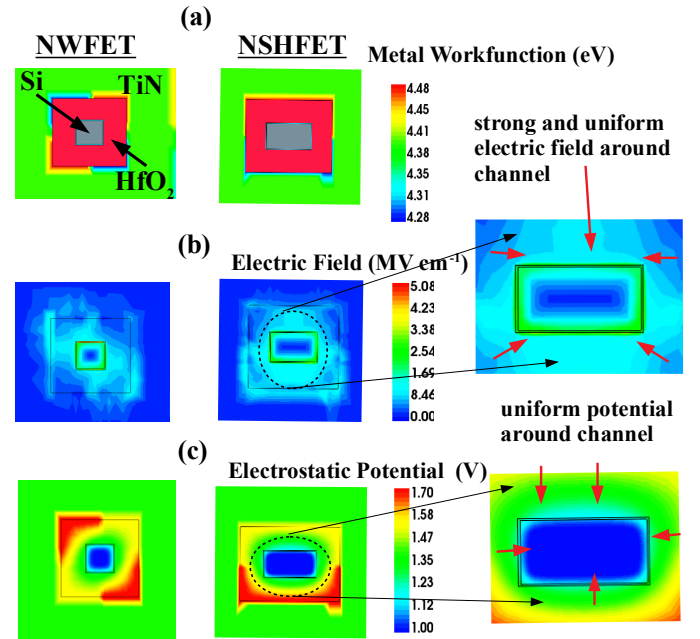

Fig. 4. Cross-sectional view of (a) metal work function (b) Electric field (c) Electrostatic potential variation for single stack NWFET (left) and NSHFET (right) respectively.

variation, electric field and electrostatic potential for single stack NWFET and NSHFET are done (Fig.4). Based on the work function distribution profile, electrostatic potential and electric field are distributed accordingly for NWFET and NSHFET. It is revealed that the electric potential distribution fluctuation due to WFV around the channel region is less compared to that around gate dielectric for both NWFET and NSHFET (Fig.4(c)). It is found that the WFV induced potential fluctuation around channel region is more uniform for NSHFET compared to NWFET. Also NSHFET shows strong and more uniform electric field distribution (due to WFV) than NWFET around channel resulting in more averaging effect. This conveys the fact that $G_{size,eff}$ is smaller than G_{size}.

WFV depends on both average grain size (G_{size}) and area of metal gate, which determines the number of grains cov-
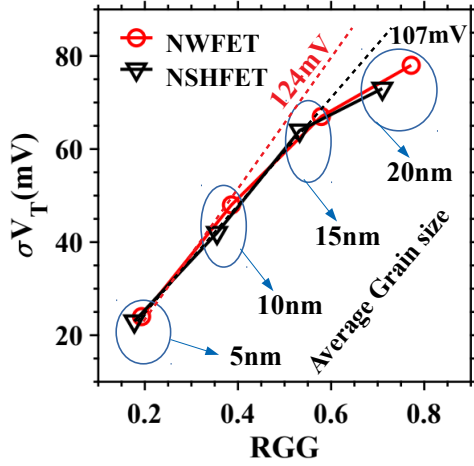
Fig. 5. σV_T vs RGG plot for NSHFET and NWFET for different grain sizes.

Fig. 6. Bar diagram of threshold voltage deviation comparison for NSHFET and NWFET for different number of stacks.

ering the metal gate area. In order to consider both these factors, RGG (ratio of average grain size to gate area) has been proposed [9]. To accurately analyse the work function variability of NWFET and NSHFET, we have considered RGG plot. The RGG for both NWFET and NSHFET are calculated as following [9] equations (1) and (2) respectively. Fig.5 shows

$$RGG|_{NWFET} = \frac{G_{size}}{\sqrt{L_G \times [4t_{NS} + 8t_{ox}]}} \quad (1)$$

$$RGG|_{NSHFET} = \frac{G_{size}}{\sqrt{L_G \times [2(t_{NSH} + W_{NSH}) + 8t_{ox}]}} \quad (2)$$

WFV induced threshold voltage deviation of single stack NWFET and NSHFET as a function of RGG. With RGG value, we can compare threshold voltage deviation due to MGG for different devices despite device dimension and grain size of gate metal. For a fixed RGG value, NSHFET shows less σV_T than NWFET (Fig.5). Thus it is revealed that NSHFET is more immune to WFV than NWFET. The smaller slope of RGG plot shows better immunity to WFV variation. The slope of RGG plot of NSHFET (107mV) is smaller than NWFET (126mV) due to averaging effect of WFV. Thus σV_T deviation (due to WFV) in NSHFET can be suppressed to 15.01% than NWFET.

Fig.6 shows comparison of σV_T deviation due to WFV for different stacked NSHFET and NWFET. As the number of stacks increases from 1 to 3, the MGG induced σV_T deviation decreases for both NWFET and NSHFET. This is because the MGG induced σV_T deviation is averaged out by multiple channels in 3-stacked NWFET and NSHFET. However, 3-stacked NSHFET shows more immunity to WFV than 3-stacked NWFET due to more averaging effect. As the number of stacks increases from 1 to 3, NSHFET and NWFET shows 40.47% and 29.16% less WFV induced σV_T deviation respectively. The ON-current (I_{ON}) and OFF-current (I_{OFF}) variation in 3-stacked NSHFET and NWFET due to WFV (average grain size=10nm) are shown in Fig.7 (a) & (b) respectively.
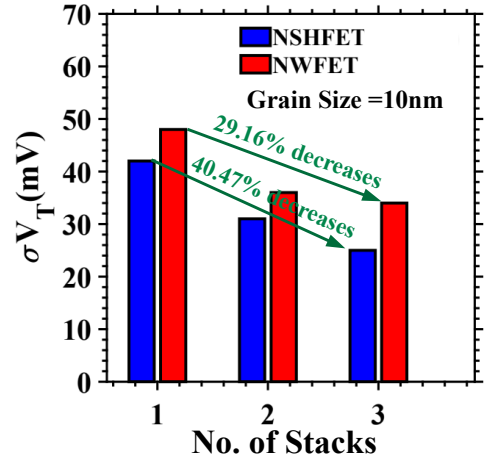
WFV induced NSHFET shows strong correlation (ρ=0.86) between ON and OFF-current in comparison to NWFET (ρ=0.2). The amount of variation in I_{ON} and I_{OFF} due to WFV can be calculated from relative variation (($\sigma/\mu)I_{ON/OFF}$). The WFV induced realtive ON-current variation in NSHFET and NWFET shows relatively similar variation. However, the relative OFF-current variation due to NSHFET [($\sigma/\mu)I_{OFF}$=0.77] is 57.46% less compared to NWFET [($\sigma/\mu)I_{OFF}$=1.34]. The WFV induced variations of stacked NSHFET and NWFET are suppressed by individual channel variations in the stack. NSHFET shows more suppression of leakage current variation compared to NWFET due to more averaging effect of WFV. Thus the WFV induced σV_T deviation can be more suppressed by increasing the number of stacks in NSHFET. In-order to compare the threshold voltage mismatch index (A_{VT}) of NSHFET and NWFET due to WFV, Pelgrom plot analysis has been carried out as shown in Fig.8 [16]. 3-stacked NSHFET shows better A_{VT} value (0.7mV.μm) compared to NWFET (1.2mV.μm). This indicates that threshold voltage mismatch between two randomly selected device samples, NSHFET will show less variation compared to NWFET.
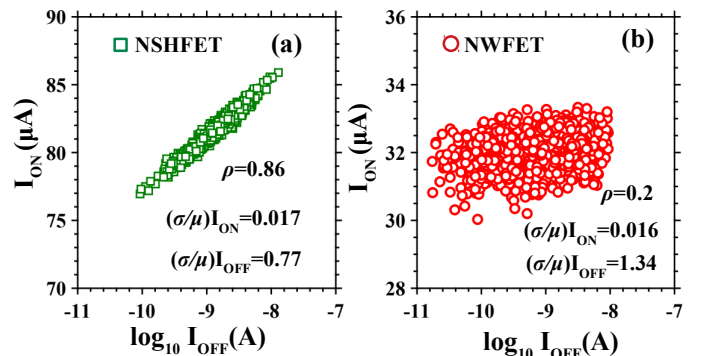

Fig. 7. Scatter plot of ON and OFF current of 3-stacked (a) NSHFET (b) NWFET due to WFV for average grain size of 10nm.
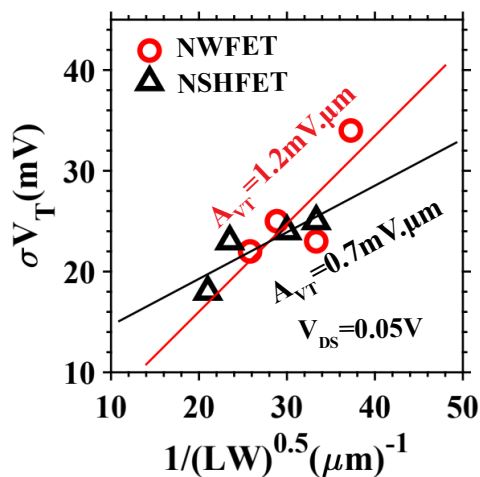
Fig. 8. Pelgrom analysis of 3-stacked NSHFET and NWFET due to WFV for an average grain size of 10nm.

Conclusions

In this work, we have investigated WFV induced V_T variation in NSHFET in comparison to NWFET for future sub-7nm technology. The WFV induced V_T variability analysis has been carried out using RGG metric. From RGG metric, NSHFET (slope=107mV) shows better immunity to WFV induced transistor performance than NWFET (126mV). It is revealed that σV_T due to WFV can be effectively suppressed by increasing the number of stacks in NSHFET compared to NWFET. 3-stacked NSHFET effectively suppresses the WFV induced OFF-current deviation in comparison to 3-stacked NWFET. NSHFET shows around 41.6% lesser A_{VT} value compared to NWFET. Thus we conclude that NSHFET is a better logic device candidate for future sub-7nm high performance logic applications considering immunity towards WFV.

Acknowledgment

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