EFFICIENT ARCHIETECTURE FOR EFFECTIVE UTILIZATION OF
HARVESTED POWER IN MICROSCALE ENERGY HARVESTING

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This Thesis entitled Efficient Architecture for effective utilization of Harvested Power in Microscale Energy Harvesting by Ghanashyam H S is approved for the degree of Master of Technology from IIT Hyderabad

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Abstract

Recent developments in combining sensors, microprocessors, and radio frequency (RF) communications holds the potential to revolutionize the way we monitor and maintain critical systems. In the future, literally billions of wireless sensors may become deeply embedded within machines, structures, and the environment. Sensed information will be automatically collected, compressed, and forwarded for condition based maintenance. Energy Harvesting comprises a promising solution to one of the key problems faced by battery-powered Wireless Sensor Networks, namely the limited nature of the energy supply (finite battery capacity). By harvesting energy from the surrounding environment, the sensors can have a continuous lifetime without any needs for battery recharge or replacement.

A typical energy scavenging system consists of a micro scale transducer, power converter, a control unit and battery for storage. The power converter is operated at a frequency to extract the maximum power from the transducer. The control unit has a Maximum Power Point Tracking (MPPT) VCO which is used to generate the clock for the power converter. The drawback with the system is, even when the transducer is not delivering power, the power converter is functioning hence consuming power from the battery. The control unit continuously consumes power to generate the clock for the power converter. The net power delivered by the scavenging system is positive only if the power extracted by the converter is higher than the power required for providing clock to the converter. We have proposed a sensor circuit so that the power converter can be switched off when the net power is negative. And switched back on when the net power becomes positive. Also a battery management unit which can monitor the battery for under and over voltages is designed. A new topology for charge pump is proposed, which is efficient at higher gains. Also reconfigurable charge pumps proposed which switch between gains by switching the topologies to serve over a wider range of input voltages.

Contents

1. Introduction

1.1   Introduction

Battery technology has undergone tremendous progress since it was first discovered. This progress has enabled the explosion of a wide range of new applications such as in mobile devices. However, new trends in technology added to some intrinsic limitations of batteries have motivated research into new energy generation solutions. There is a great interest in using free available external energy sources for powering small electronic systems, a process known as energy harvesting. We must distinguish between macro and micro energy-harvesting scales. Macroharvesting is related to energy recovery in the range from kilowatts to megawatts, which are fed to the grid. From the micro-scale point of view, a limited amount of energy, in the range from nano-watts to milli-watts, can be obtained from different types of external ambient sources and energy transducers

The advances in semiconductor technologies related to the reduction of the transistor's size allow the industry to obtain more interest in the development of new self- powered portable electronic devices that incorporate a great variety of circuitry and functions of new self-powered portable electronic devices that incorporate a great variety of circuitry and functions.

Energy harvesting, small-format batteries, and power management integrated circuits (ICs) are technologies that will enable commercialization of the next generation of ultra-low-power electronic devices and systems. Such devices are being deployed for wireless as well as wired systems such as mesh networks,

sensor and control systems, RF identification (RFID) devices, MEMS , and so forth [5].The reduced battery maintenance and replacement are expected to provide substantial growth market opportunities for power management technologies. Overall, the commercial viability and market opportunities, the dissemination and adoption of new value-added technologies based on energy harvesting, contribute to a global green growth exploiting new market and technological challenges.

1.2 Aim and Motivation

There is pressing need of design ultra-low power self-powering circuit for number of application such as remote wireless sensors nodes, biomedical implant etc. As these required small area, it is essential to generate power from a single-solar cell that will force the researcher to build up an ultra-low voltage power management circuit
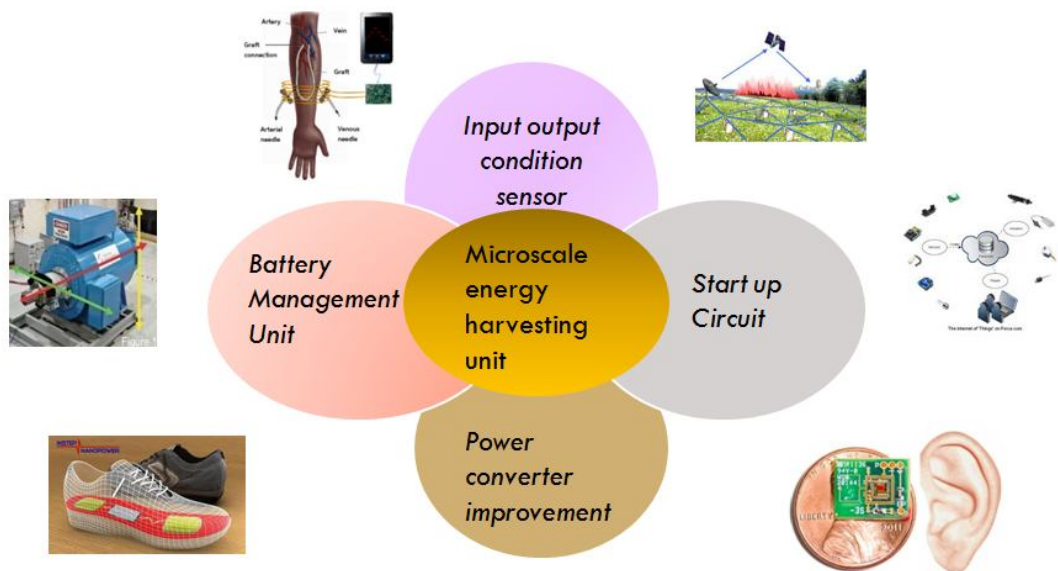

Figure 1.1 . Aim and Motivation.

A typical energy harvesting system consist of a transducer, DC-DC converter, control unit and battery storage (energy buffer). The transducer converts

environmental energy to electrical energy that can be stored in storage batteries. The storage batteries normally function on or above 1V. However, due to very low output voltage of transducer (0-0.4V), a DC-DC converter based power management unit is placed in between transducer and batteries to step up the its output voltage. For on chip energy harvesting application, charge pumps are preferred over inductor based DC-DC converter as inductors are bulky. A control unit is used to produce the clock for the operation of the charge pump. The control unit consumes power from the battery to produce these clocks. For the system to deliver net positive power to the battery, the power delivered by the charge pump should be higher than the power consumed by the control circuitry. Hence the design of microscale energy harvesting requires a system to monitor the net power delivered to the battery and accordingly disable or enable the system. The control unit is powered from the battery and also simultaneously the load could be consuming the battery. So a battery can discharge below its favorable under voltage limit. Also since the battery is continuously charge under favorable environmental condition. A battery management system is required which can monitor the battery for under and over voltages and take suitable measures to protect the battery and keep the system running. The power converter is the integral part of the energy harvesting system, an efficient power converter needs to be designed for the system.

1.3   Literature Survey

The major work on the power management module of micro-scale energy harvesting chipset are done in Maximum power point tracking (MPPT) for extracting the maximum power from energy harvesting sources , DC-DC converter for boosted voltage, battery element for the storage of the power. Estimates of the available energy per unit area, or volume, for each harvesting source, are reported in Table I [30]. These values depend heavily on the excitation conditions and technologies used. As an individual source, it has reported that a peak power of 400 μW can recover through vibration energy scavenging [31]. In [32], the utilization solar cell in indoor condition can provide

a power of 5 μW at 10 lux to 200 μW at 1450 lux. Recently researcher tried to scavenge the energy from all available sources like vibration, solar, RF , thermal etc.

TABLE I

Estimated Energy Harvesting from ambient sources

Energy Source	Performance
Ambient Light	Indoor 10uW/cm^2 (low illumination)
	Typical Office 100uw/cm^2
	Outdoor 10mW/cm^2
	Full bright sun 10mw/cm^2
Vibrational	4uW/cm^3 (human motion Hz range)
	800 uW/cm^3 (machines k-Hz range)
	These numbers depend heavily on size excitations, technologies, etc.
	Typically:
	Piezoelectric ~ 200uW/cm^3
	Electrostatic ~ 50-100uW/cm^3
	Electromagnetic < 1uW/cm^3
RF	GSM 4uW/cm^2
	WiFi .001mW/cm^2
	These numbers depend heavily on frequency
	of operation and distance between base station and receiver
Temperature Difference	Human 25uW/cm2-60uW/cm^2
	Industry 10mW/cm^2

The drawback with the existing system is, even when the transducer is not delivering power, the power converter is functioning hence consuming power from the battery. The MPPT unit continuously consumes power to generate the clock for the power converter. The net power delivered by the harvesting system is positive only if the power extracted by the converter is higher than the power required for providing clock to the converter. In ultra-low power wireless systems, the battery life is very critical and efficient battery management is needed to enhance the battery life. Overcharging and over discharging will reduce the battery life. The main function of the power management unit is to monitor the voltage across the energy buffers and to ensure the voltage is within the safe operating region determined by the under voltage and overvoltage thresholds [15]. So that the battery life is enhanced and the system performance is improved. In many energy harvesting systems, using single storage element will not be good enough to deliver maximum performance. On-chip implementation of power management units is required in micro-power energy harvesting and micro-sensor application. The power management unit usually include integrated switched-capacitor power converters or charge pumps. Along with the popular Dickson charge pump, Fibonacci charge which is a two phase charge pump with highest gain for the number of capacitor is used. In this thesis, we have proposed a new topology charge pump which can provide higher current compared to Fibonacci charge pup at comparable gain.

1.4   Contribution of Thesis

This work focuses on the design of efficient architecture for effective utilization of harvested power in microscale energy harvesting for ultra-low power systems. The main contributions of this research work are as follows:

- A novel sensor circuit to enable or disable the power converter based on the availability of power.

- A power management unit that controls the charging and discharging of the batteries. A novel startup circuit is designed to power up the system when the batteries are below under voltage.
- A new topology of charge pump, for high gains in low stages for very low voltage applications.
- Designed reconfigurable charge pump, to reconfigure between linear and the proposed charge pump.

2. Power Condition Sensor

2.1 Introduction

A typical energy harvesting system consists of a micro scale transducer, power converter and battery for storage. The power converter is operated at a frequency to extract the maximum power from the transducer. An MPPT tracking VCO is used to generate the clock for the power converter. The drawback with the system is, even when the transducer is not delivering power, the power converter is functioning hence consuming power from the battery. The MPPT unit continuously consumes power to generate the clock for the power converter. The net power delivered by the harvesting system is positive only if the power extracted by the converter is higher than the power required for providing clock to the converter. The proposed approach is to use a sensor so that the power converter can be switched off when the net power is negative. And switched back on when the net power becomes positive.

So as to effectively monitor the power condition of the system The output load current provided by each of the transducer converter block is sensed by the output load current sensor. When there is very low output current by one of the converters, the MPPT control block of that converter is switched off by the Control block, to save the battery power consumed by that MPPT block.

Once a converter block is switched off, the input conditions of that converter block is monitored by the input condition sensor and is fed to the Control block. When the input condition improves, the corresponding MPPT block is re-activated. By this scheme, when any one of the source is not giving enough output power, the MPPT block of that source converter is switched off. Thus saving the power the MPPT block consumes from the battery.(Fig. 2.1)
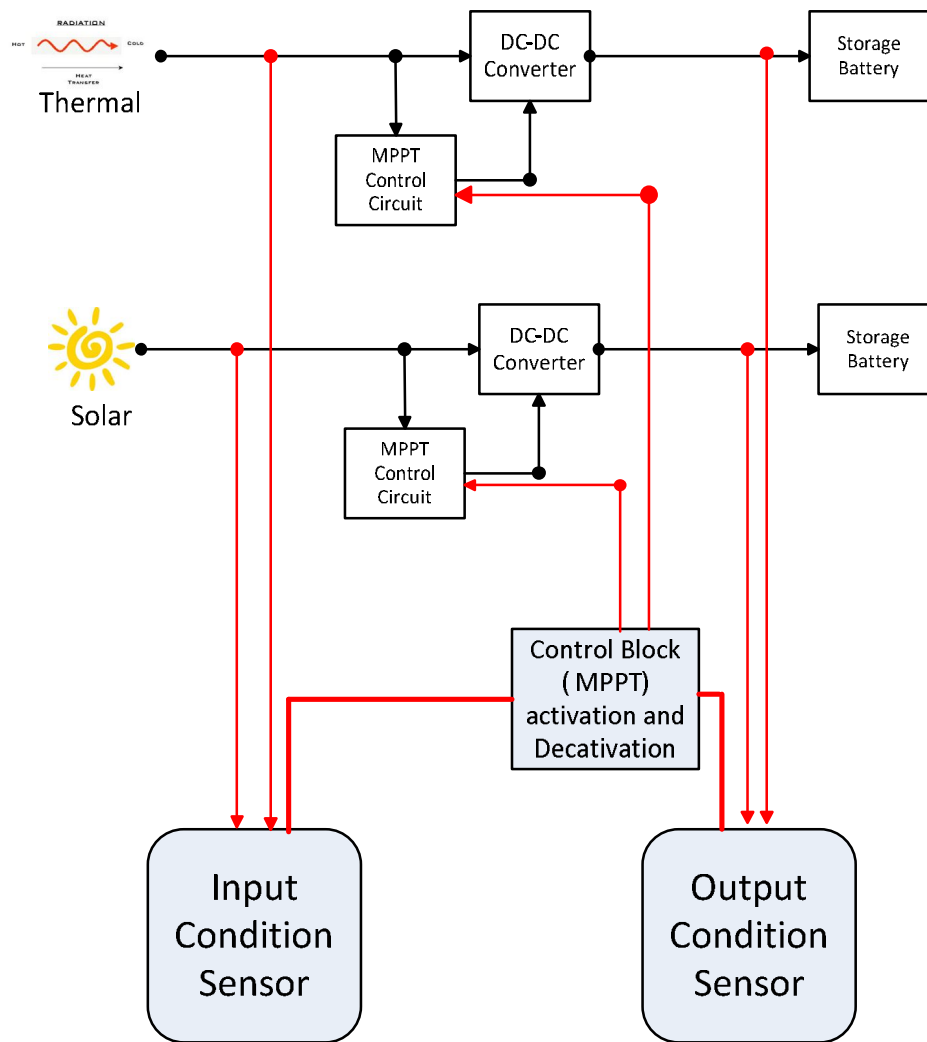
Figure 2.1 Control Circuit Activation and Deactivation

2.2 Power Condition Sensor System Description

To obtain an estimate of the net power, the MPPT block generating the clock is powered using a capacitor. Also, the output of the power converter is connected to the same capacitor. An increase in the voltage across the capacitor implies positive net power and a decrease implies a negative net power. The sensing circuit consists of two capacitors C1 and C2 and a comparator. The activation signal to the sensing circuit is provided by low frequency clock. When the sensing circuit gets activated the battery voltage is sampled across the capacitors. the MPPT block producing clock is

powered using the capacitor C1 and the output current is also fed to the capacitor C1. After a brief time, the voltage at capacitor C1 is compared with that of C2. A decrease in voltage across capacitor C1 compared to C2 indicates that the power consumed to generate the clock for the power converter is more than the power delivered to the battery. The power converter is switched off, to save power.

Figure 2.2 shows the block diagram. The control signals are generated using a very low frequency clock. When sig1 goes low the two capacitors are connected in parallel with the battery. During this time the capacitors C1 and C2 are charged to battery voltage. As sig1 goes high and sig2 low the power to the clock generator and buffers is provided by the capacitor C1, also the output power from charge pump is fed to capacitor C1. The Comparator_active signal enables the comparator to compare the voltage across the two capacitors. The system is disabled if the voltage across C1 is less than that across C2.
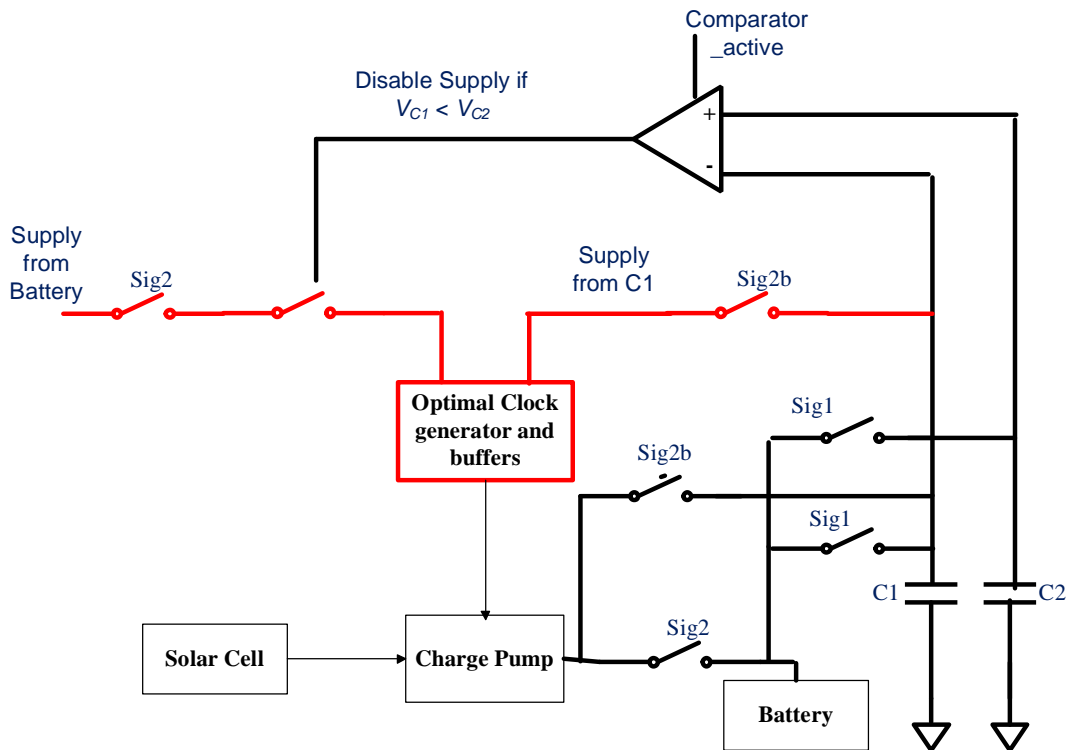

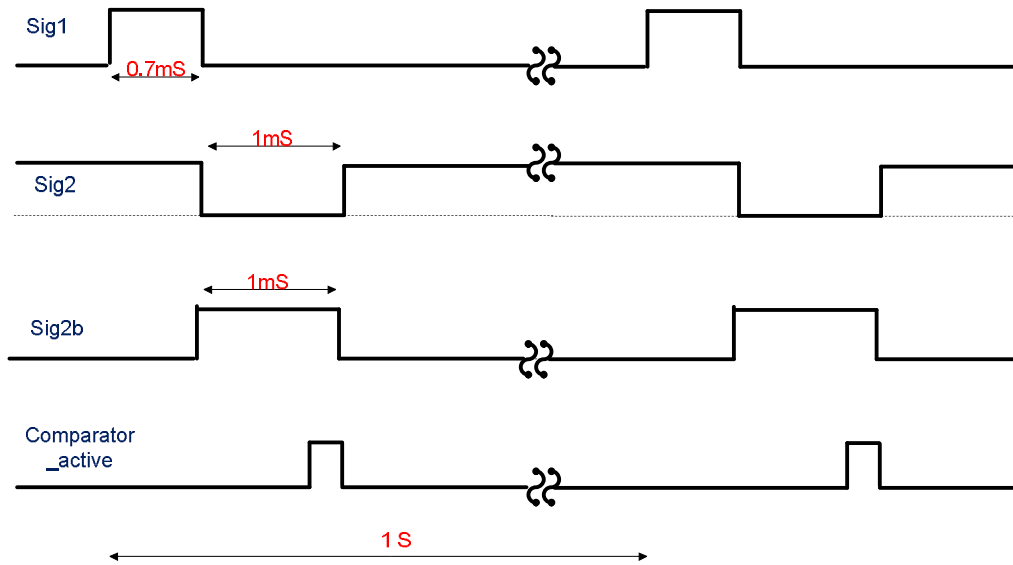Figure 2.2 Implementation of the Power condition sensor

Figure 2.3 Control signals for power condition sensor

Here two 500pF capacitors are used. A very low frequency clock is used to generate signal sig1. When sig1 goes low the 2 capacitors are connected in parallel with the battery. The signal sig1 is held low for 700us so that the two 500pF capacitors reach up to the battery voltage. After sig1 another signal sig2 is pulled low. When sig2 goes low the power supply to the power converter system is provided by one of the 500pF(C1) capacitor. And also the power delivered by the power converter is fed into this 500pF(C1) capacitor. After a period of 1ms sig2 is pulled high so that the power converter gets its power from the battery and also delivers the power to the battery. After the sig2 period comp_active pulse is generated to compare the voltages across the two capacitors.

2.3 Simulation Results and Discussion

The circuits are designed in 0.18μm CMOS technology. The plots of the sensors are shown in Figure 9. Plot (a) in Figure 9 shows the value of the Vsource (thermal input voltage here). Plot (b) shows signal sig1 which is usedto sample the battery voltage into capacitors C1 and C2. Plot (c) shows signal sig2, which runs the whole system

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with the capacitor C1. Plot (d) and (e) shows the voltage curves of capacitors C2 and C1. Plot (f) shows the switch_off signal which is the sampled value from the comparison between voltage levels of C1 and C2. Initially the system is switched off, the Vsource during the time T1 is still 100mV, during sig2 the system is run using capacitor C1. And as the Vsource is less, the voltage across C1 falls indicating that the system should remain switched off. In the time T2 Vsource has increased to 400mV. At this voltage when the system is run using capacitor C1 when sig2 is high, the voltage across C1 increases. This indicates that the source condition has improved and the system needs to be switched on. The switch_off signal is accordingly set to turn on the system.
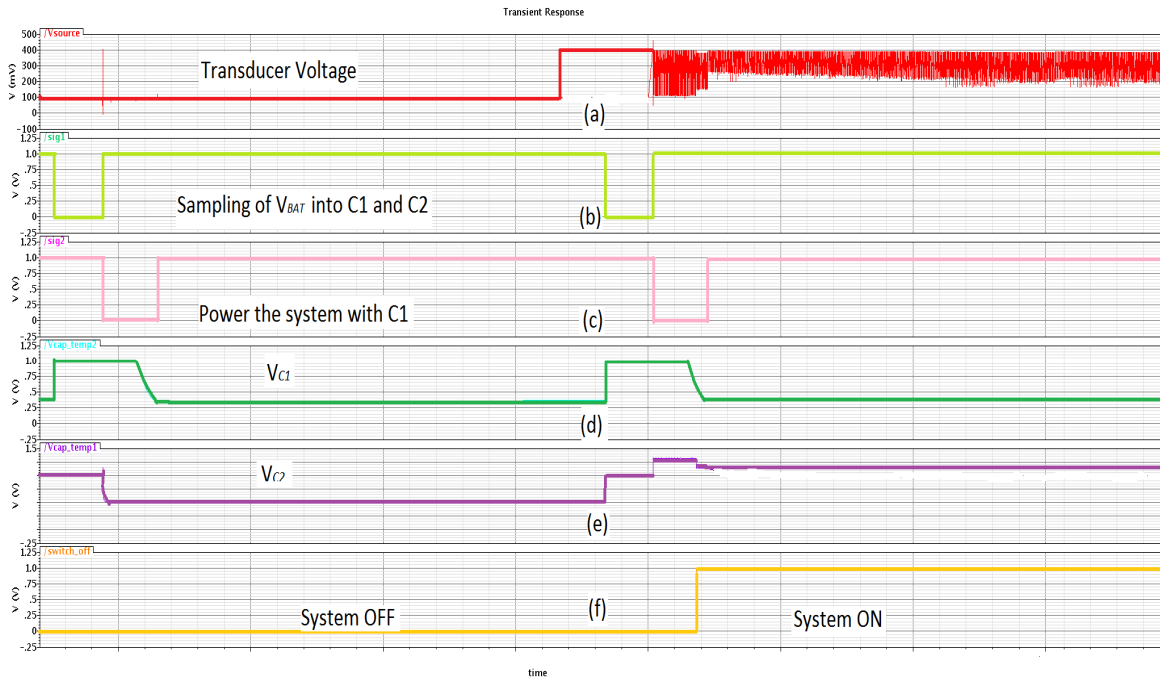

Figure 2.4 Simulation Waveform

2.4 Conclusion

A power condition sensor can suitably enable and disable the system based on the environmental condition. Power saving is achieved by deactivating the clock generator, if the environmental power source has deteriorated. The system can be

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used for any kind of power converter as the principle of net power delivered applies for all kinds of power converters.

3 Battery management unit and start up circuit

3.1 Introduction

In ultra-low power wireless systems, the battery life is very critical and efficient battery management is needed to enhance the battery life. Overcharging and over discharging will reduce the battery life. The main function of the battery management unit is to monitor the voltage across the energy buffers and to ensure the voltage is within the safe operating region determined by the undervoltage and overvoltage thresholds. So that the battery life is enhanced and the system performance is improved. A battery management unit is designed which monitors the battery for over voltage threshold and disables the energy harvesting system to prevent over charging. Also the battery management unit disconnects the load from the battery if the operating voltage is below lower threshold, and activates the start up circuit. The start up circuit is a standalone circuit which can harvest energy from the transducer without, any external clock source. Though the efficiency is less, the start up circuit can help recharge the battery without any power consumption from battery.

3.2 Start Up circuit

Since the voltage produced by single PV cell is sub threshold, a startup circuit is essential to power up the system when the battery is empty. The voltage developed across the solar cell is not high enough to drive any circuits effectively. The startup circuit will generate higher voltages for proper functioning of the power converter and power management unit. Most of the startup circuits that are used in low

voltage domain uses inductors [11] tunnel diodes [12], or mechanical switches[13, 14].

The proposed start-up circuit is purely based on CMOS. It has 3 stages of voltage doublers and a CMOS ring oscillator. The ring oscillator oscillates between the available solar voltage (V_{PH}) and ground (0V) thus provides a clock of V_{PH}(0.3 - 0.4V).This clock is used drive the first voltage doubler. Even though the efficiency of this doubler is poor (it works with sub threshold current), it can produce a voltage which is higher than threshold voltage of MOSFET. Using this voltage, another clock is created using CMOS inverters to drive the next voltage doubler. One more doubler stage is used to make decent voltage amplitude (1V) as shown in Fig. 3.1. The circuit diagram of individual voltage doublers is shown in Fig. 3.2. Clk and Clkb are derived from the oscillator using n inverter. The voltage generated by start-up circuit is used to charge a capacitor of 50µF up to a voltage of 1V. This charged capacitor is then used as power source for the MPPT unit and clock drivers to charge the battery.
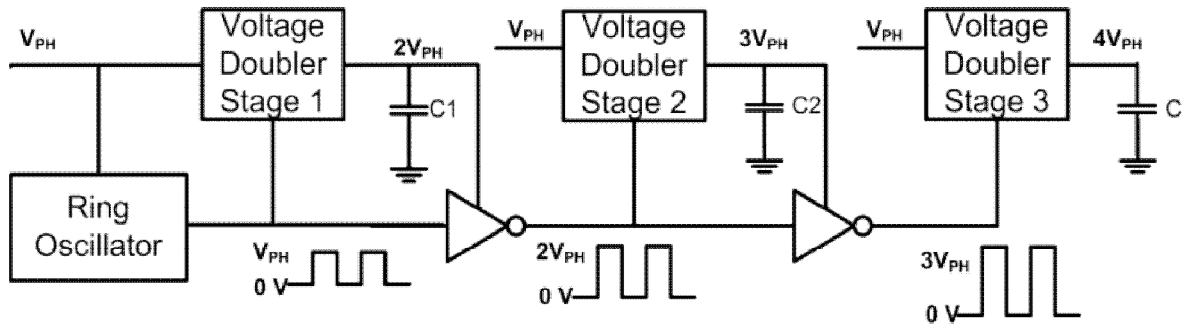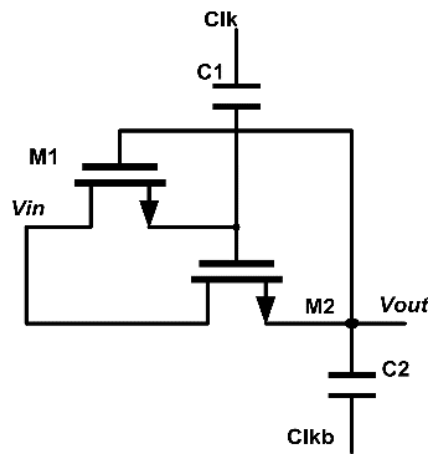

Figure 3.1 Start up Circuit

Figure 3.2 Voltage doubler

3.3 Battery management Unit

Fig.3.3 shows the energy harvesting unit with startup and the power management. In this system two energy buffers (one capacitor and one battery) are used as storage elements. When the batteries are empty, the startup circuit will charge the capacitor until the capacitor can deliver enough current to drive the power management unit and charge pump. Once the charge pump has started functioning normally, the startup circuit is disabled by the power management unit. The two buffers are charged alternatively until they are completely charged. If any of them is fully charged, further charging of that battery is prevented to avoid overcharging. If both the buffers are completely charged, the MPPT and charge pump are disabled. Similarly the power management unit disconnects the load from the battery if the operating voltage is below lower threshold.
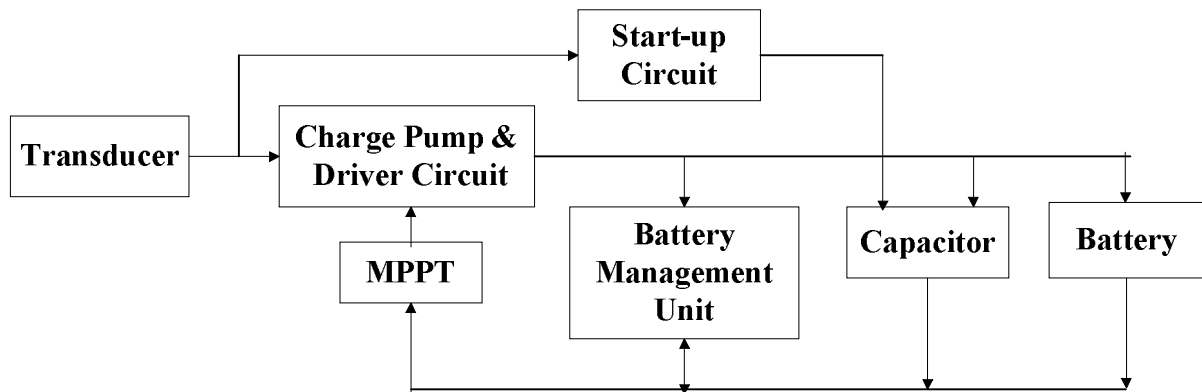

Figure 3.3 Energy harvesting unit with battery management and start up circuit

The internal block diagram of the power management unit is shown in Fig 3.4. It mainly consists of a Bandgap reference [16], comparator and Flip flops. The BGR is used to produce the reference voltage that is compared with the scaled version of the battery voltage to identify whether the voltage is in the safe operating region. If the voltage is above the upper threshold, charging of the battery is prevented and if it is below the lower threshold, further discharging is prevented (load is disconnected).

To perform all the above operation we need two reference voltages (upper threshold and lower threshold) and four comparisons (over voltage and under voltage comparisons for two buffers). In order save power and hardware cost single BGR and comparator is used to perform all these operations by proper design of control signals. Four Flip flops are used to store the comparison results.
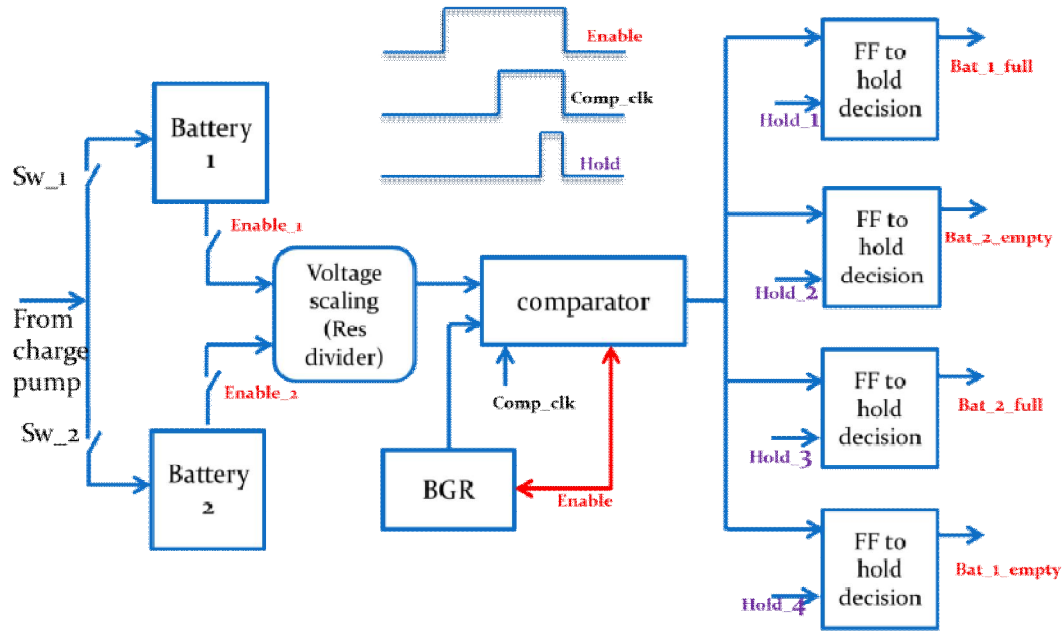

Figure 3.4 Block Diagram of Battery management Unit

In our system the nominal battery voltage is assumed to be 1V and the lower threshold and upper threshold are defined as 0.9V and 1.1V. One of the challenges in using BGR in this system is that the supply voltage to the BGR is also from the battery and it is not fixed. As the battery voltage is falling, it will affect the reference voltage. Hence the reference voltage produced by the BGR at 1.1V is different from that at 0.9V they are 784.7mV and 773mV respectively. These reference voltages are taken as upper voltage reference and lower voltage reference. The battery voltage that is to be compared is connected to the comparator through a voltage divider. The design of the voltage divider is done such a way that at battery voltage 1.1 V and 0.9V, the divider output matches exactly the over voltage reference and under voltage reference.
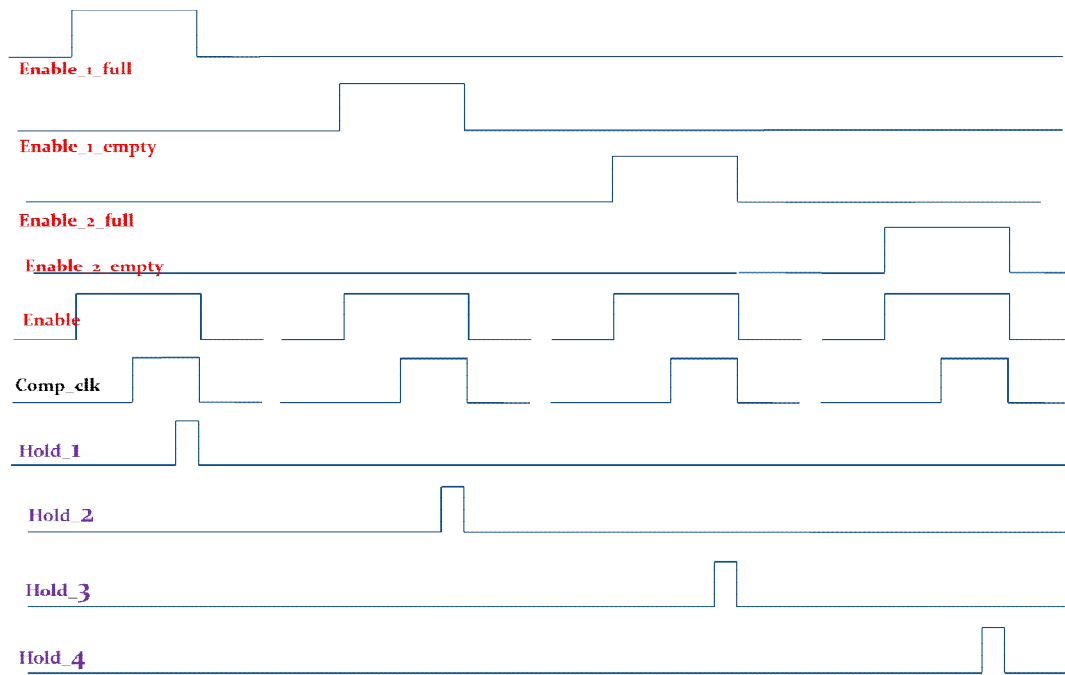
Figure 3.5 Control signal for battery management unit

The control signals used in the circuit are shown in Fig 9. The control signals play an important role in reducing power consumption. The devices are enabled according to the requirement and disabled after that to save power. There are four enable signals to carry out four comparisons. The enable signal enables the comparator and BGR. The BGR requires finite amount of time to produce the reference voltage. Thecomparison is done during the Comp_clk signal. Four signals Hold_1, Hold_2,Hold_3 andHold_4 are used hold the results of these four comparisons. The outputs of the Flip flops are used to make the decision to charge / discharge the batteries.

3.4 Start up circuit enabling

The battery is continuously monitored for over-voltage and under-voltage. The system is switched off when the battery voltage reaches 1.1V, to protect the battery

from over charging. Also, the system is switched off and load disconnected, when the battery voltage reaches 0.9V. Once the battery voltage reaches 0.9V, the power converter is disabled and the transducer connected across a start up circuit. The start up circuit has a 50uF capacitor at its output. The transducer is connected across this 50uF capacitor until the capacitor's voltage reaches to that of the battery. The power converter system is run using this 50uF capacitor until the battery voltage crosses the 0.9V. The block diagram is shown in Figure 3.5.
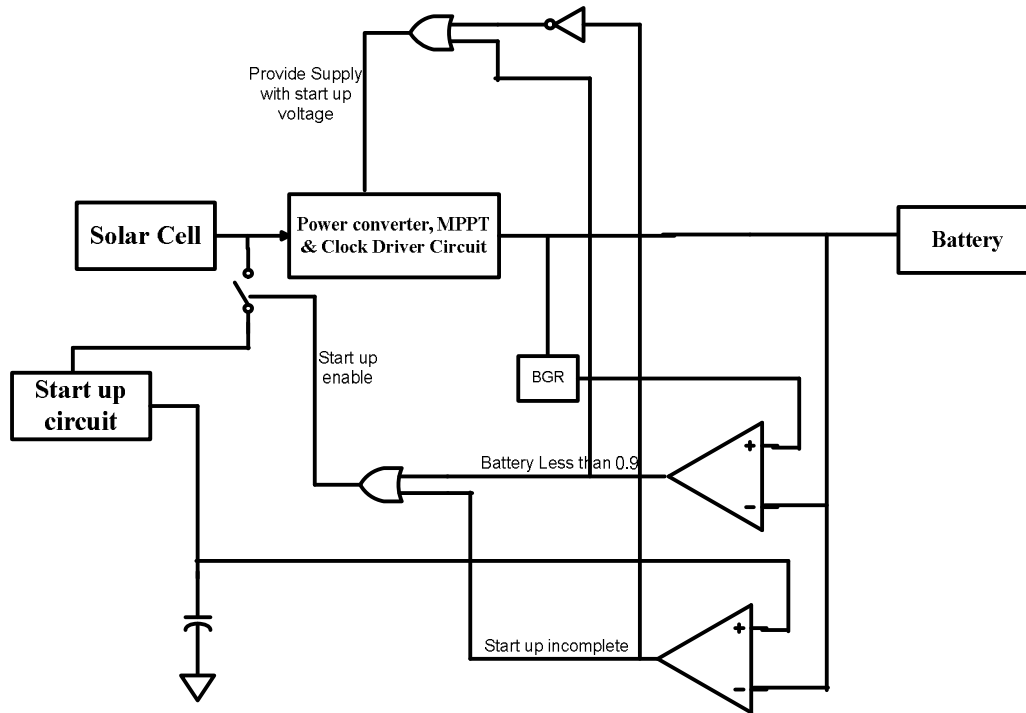
Figure 3.5 Start up circuit enable logic

3.5 Simulation Results and Discussion

The circuits are designed in 0.18μm CMOS technology. The control signals were generated using a low frequency clock. The startup circuit takes around 20 seconds to charge a 50μF capacitor to 1V at the transducer voltage of about 350mV.

3.6 Conclusion

Efficient power management systems for Microscale energy harvesting are discussed. The battery management ensures that the voltage is within the safe operating region determined by the undervoltage and overvoltage thresholds. The system was developed for multiple batteries. A startup circuit is designed for self-starting of the system. A control logic was developed for enabling the start up circuit

4 . A new topology of charge pump and its comparison with Fibonacci and linear charge pump

4.1 Introduction

On-chip implementation of power management units is required in micro-power energy harvesting and micro-sensor application. The power management unit usually include integrated switched-capacitor power converters or charge pumps. Along with the popular Dickson charge pump, Fibonacci charge which is a two phase charge pump with highest gain for the number of capacitor is used. The proposed $2^{N+1} - 1$ gain charge pump can give better current output with the same number of capacitors as Fibonacci at comparable voltage gain

Fibonacci charge pump and $2^{N+1} - 1$ charge pump are compared at equal number of capacitor and equal total area occupied for capacitors. The mathematical analysis of $2^{N+1} - 1$ charge pump is done at slow-switching condition, where the switching period is larger than the time constant due to capacitor and resistance due to switches and source.

4.2 $2^{N+1} - 1$ Charge Pump Circuit

The $2^{N+1} - 1$ charge pump topology is shown in Figure 4.1. The switches are driven by two non overlapping clock phases 1 and 2. Each stage has two capacitors which are charged to the voltage of the preceding stage in one phase. The upper capacitor

is further boosted by the lower capacitors voltage and the input voltage in the next phase.
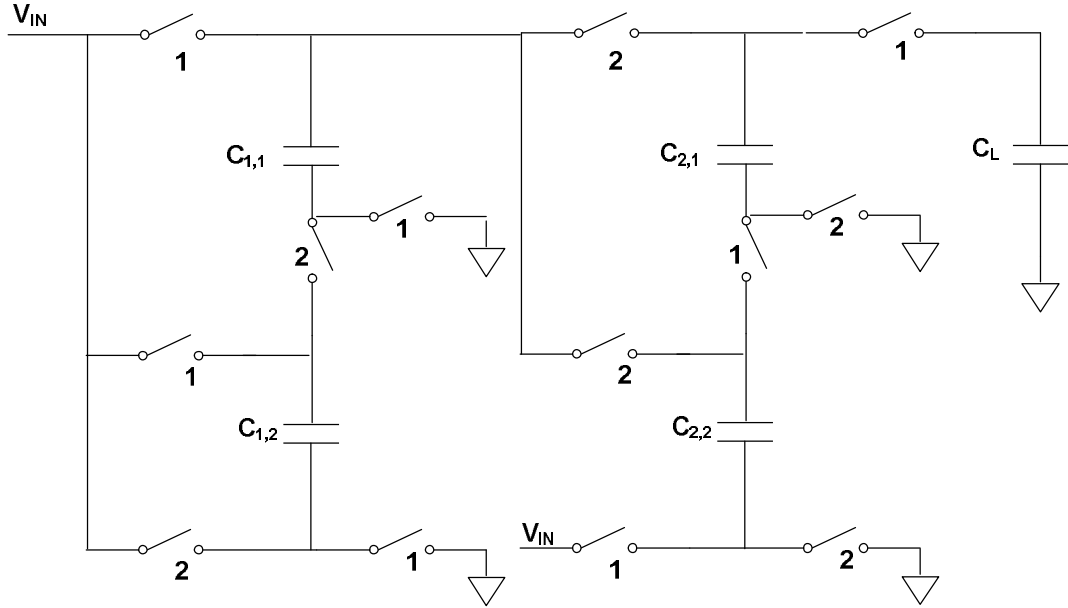
Figure 4.1 Schematic diagram of a 2-stage $2^{N+1} - 1$ charge pump

The charge pumps efficiency is affected by the output resistance, and hence has to be kept as low as possible. In the next section we optimize the capacitance at each stage to give minimum output resistance for the topology presented.

4.3   Optimization of $2^{N+1} - 1$ Output Resistance

In a two-phase circuit with switches and capacitors the output resistance [13] is given by

$$R_{OUT} = \frac{1}{f_s} \sum_{i=1}^{N} \frac{(a_{ci})^2}{c_i} \qquad (1)$$

where f_s is the switching frequency, N is the number of stages, C_i is the value of the capacitor i, and a_{ci} is its charge multiplier factor , which is given by the ratio of the charge q_i transferred by capacitor C_i in a semi-period, and the charge q_{OUT} delivered to the load. The charge multiplier factors are calculated by applying charge conservation to the circuit in phase 1 and 2, and by considering that, in steady-state, each capacitor receives and delivers the same charge in each of the two phases.

In $2^{N+1} - 1$ gain charge pump there are two capacitors at each stage and both their charge multiplier factor is given by $a_{ci1,2} = 2^{N-i}$ for $i = 1$ to N, therefore the output resistance is

$$R_{OUT} = \frac{1}{f_s} \sum_{i=1}^{N} \left[\frac{(2^{N-i})^2}{C_{i,1}} + \frac{(2^{N-i})^2}{C_{i,2}} \right] \tag{2}$$

Since the charge multiplier factor of the 2 capacitors in each stage is equal , we have $C_{i,1} = C_{i,2} = C_i$. Therefore the output resistance is

$$R_{OUT} = \frac{1}{2f_s} \sum_{i=1}^{N} \frac{(2^{N-i})^2}{C_i} \tag{3}$$

To minimize the output resistance of the $2^{N+1} - 1$ charge pump for a constant total capacitance C_T, we substitute $C_1 = C_T - C_2 - \ldots\ldots - C_N$ into (3) and we set the partials with respect to capacitors equal to zero,

$$\frac{\partial R_{OUT}}{\partial C_i} = \frac{1}{2f_s} \cdot \left(\frac{((2^{N-1})^2}{C_T - C_2 - \ldots\ldots - C_N} - \frac{(2^{N-i})^2}{C_i} \right) \tag{4}$$

For $i = 2$ to N, and leads to

$$C_{i,1} = C_{i,2} = C_T \frac{2^{(N-i-1)}}{(2^N - 1)} \tag{5}$$

Therefore for the optimal performance of an N-stage $2^{N+1} - 1$ charge pump the capacitance have to scaled in an exponential sequence with the largest pair of capacitances next to V_{DD} and the smallest pair next to load.

4.4 Analysis of $2^{N+1} - 1$ Chare Pump

Consider the Nth stage of the $2^{N+1} - 1$ charge pump. Applying the charge balance law (see Figure 4.2 and Figure 4.3) [2] gives

$$C_{N,1}V_{N-1} = C_{N,1}(V_{OUT} - V_{N,2} - V_{IN}) + I_{OUT}T \qquad (6)$$

$$C_{N,2}V_{N-1} = C_{N,2}V_{N,2} + I_{OUT}T \qquad (7)$$

Simplifying (6) and (7) we obtain

$$V_{OUT} = 2V_{N-1} + V_{IN} - \frac{I_{OUT}}{C_{N,1}} - \frac{I_{OUT}}{C_{N,2}} \qquad (8)$$
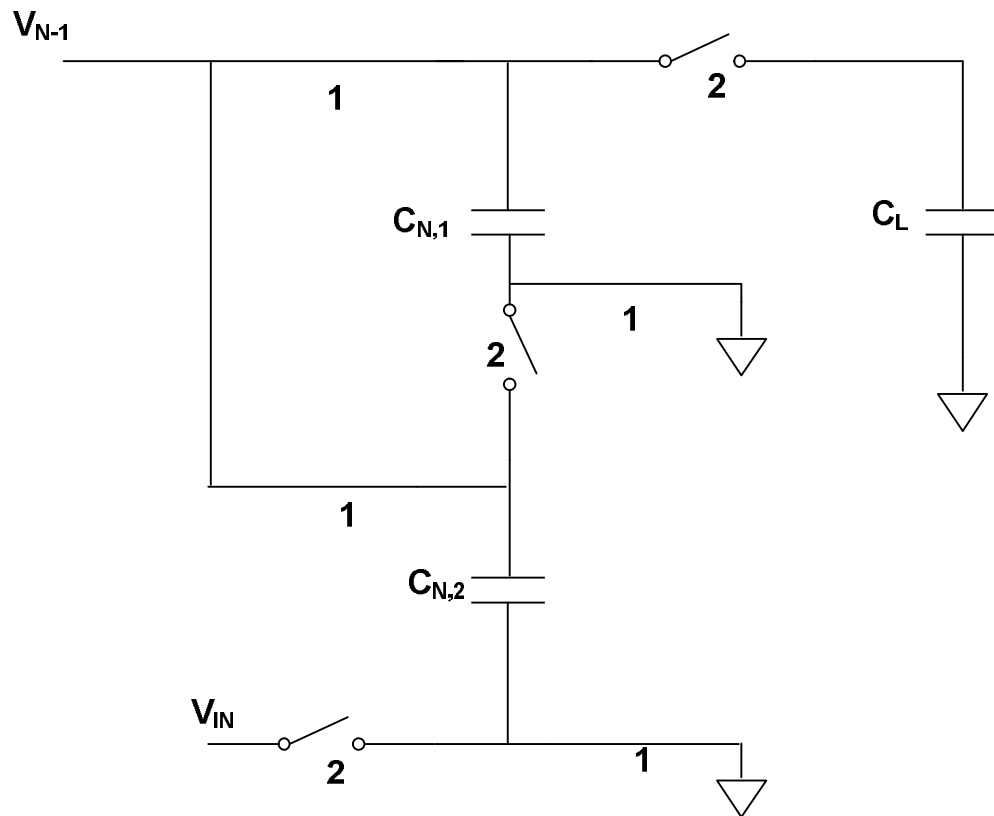
Figure 4.3 Clock Phase 1
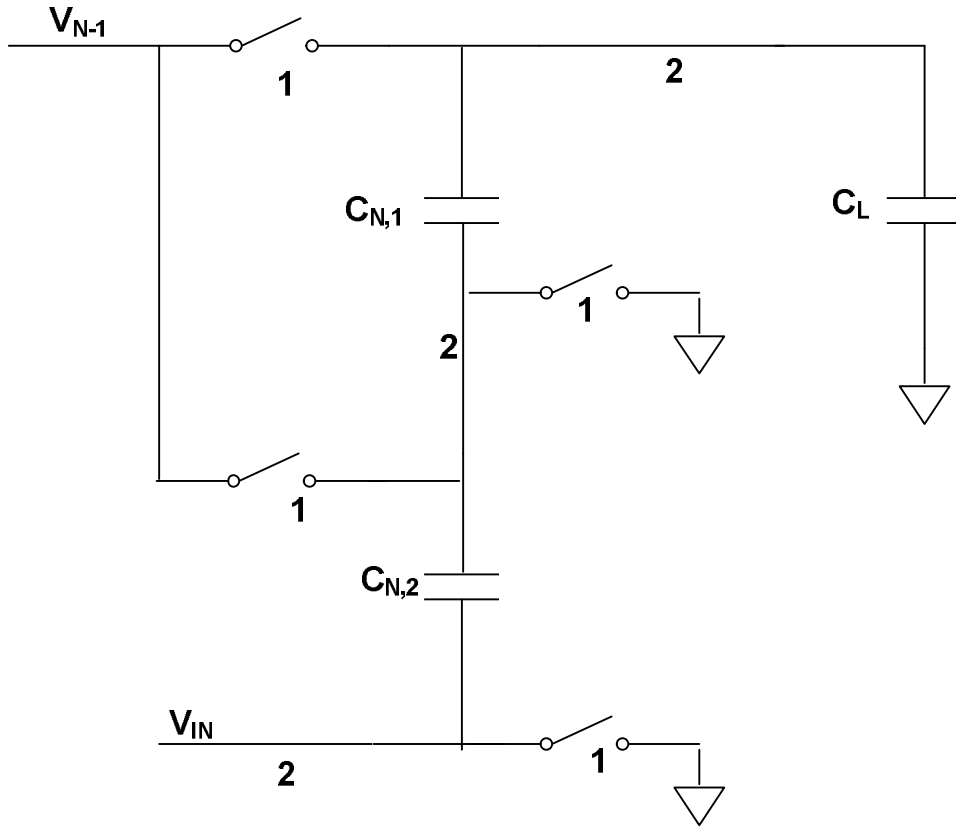
Figure 4.3 Clock Phase 3

Since the capacitor values in a single stage are equal (from (5)) we have

$$V_{OUT} = 2V_{N-1} + V_{IN} - \frac{2I_{OUT}}{C_N} \tag{9}$$

Similarly, considering the last 2 stages gives

$$V_{OUT} = 4V_{N-2} + 3V_{IN} - \frac{8I_{OUT}}{C_{N-1}} - \frac{2I_{OUT}}{C_N} \tag{10}$$

Inferring the result for N stages by observing the above trend, we have

$$I_{OUT} = \frac{[(2^{N+1} - 1)V_{IN} - V_{OUT}]f}{\sum_{i=1}^{N} \frac{2^{2i-1}}{C_{N-i+1}}} \tag{11}$$

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4.5 Comparison with Fibonacci charge pump

The I_{OUT} and C_i equations for the Fibonacci charge pump are [4]

$$I_{OUT} = \frac{[fib(N+2)V_{IN} - V_{OUT}]f}{\sum_{i=1}^{N}\frac{fib(i)^2}{C_{N-i+1}}} \tag{12}$$

$$C_i = C_T \frac{fib(N+1-i)}{\sum_{j=1}^{N}fib(j)} \tag{13}$$

The I_{OUT} and C_i equations for the Linear charge pump are

$$I_{OUT} = \frac{[(N+1)V_{IN} - V_{OUT}]f}{\sum_{i=1}^{N}\frac{1}{C_i}} \tag{14}$$

$$C_i = \frac{C_T}{N} \tag{15}$$

We take a two stage $2^{N+1} - 1$ CP and a four stage Fibonacci charge pump, whose voltage step-up ratios are comparable. With a fixed total capacitance C_T in both cases, we get

$$I_{OUT\_fib} = \frac{[8V_{IN} - V_{OUT}]fC_T}{49} \tag{16}$$

$$I_{OUT\_2^{N+1}-1} = \frac{[7V_{IN} - V_{OUT}]fC_T}{36} \tag{17}$$

$$I_{OUT\_lin} = \frac{[7V_{IN} - V_{OUT}]fC_T}{36} \tag{18}$$

From (16) and (17), we can say that a two stage $2^{N+1} - 1$ CP gives higher current than 4 stage Fibonacci CP but lesser current than a linear charge pump, with equal

total capacitance, when operated at the same frequency. Figure 4.4 plots (16) , (17) and (18). The total capacitance is taken to be 1500pF and the slow switching frequency of operation 12MHz.

4.6 Simulation Results and Discussion

The circuit are designed in 180nm technology. The ideal switches were replaced by suitable MOS switches with (W/L) = (200um/180nm). A total capacitance of 1500pF was used in each of the topology and was divided according to the optimum value at each stage as given by (5) and (13).The chare pump was connected to a capacitor of 50uF precharged to 1V, to mimic the application in energy harvesting where the charge pump is connected to a rechargeable battery. The input voltage was varied from 180mV to 360mV and the current flowing into the 50uF capacitor
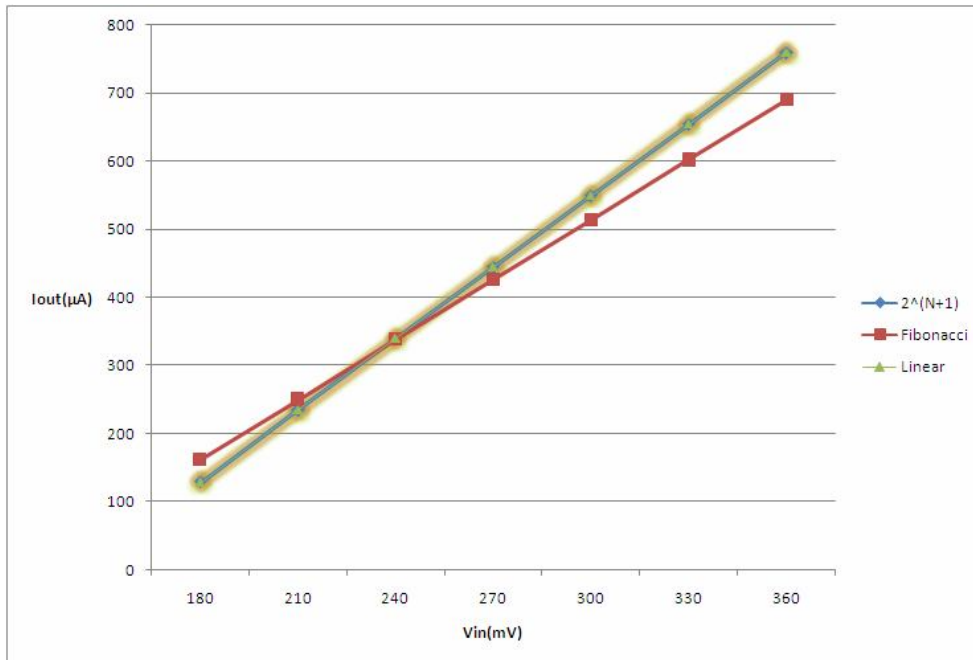

Figure 4.4 Plot for comparison of $2^{N+1} - 1$ with Fibonacci and linear charge pump

was recorded. The drivers providing the two phase clock were powered by the 50uF capacitance hence giving the net output current. The frequency of operation was varied over a wide range and the output current was noted for the frequency at which maximum current is obtaind.

Table II

V_{IN} (mV)	$I_{OUT\_2^{N+1}-1}$ (μA)	$I_{OUT_{fib}}$ (μA)	I_{out_linear} (μA)
180	31.3	57.7	16.2
210	113	132	129
240	174	192	245
270	228	234	361
300	281	259	470
330	334	272	574
360	385	280	668

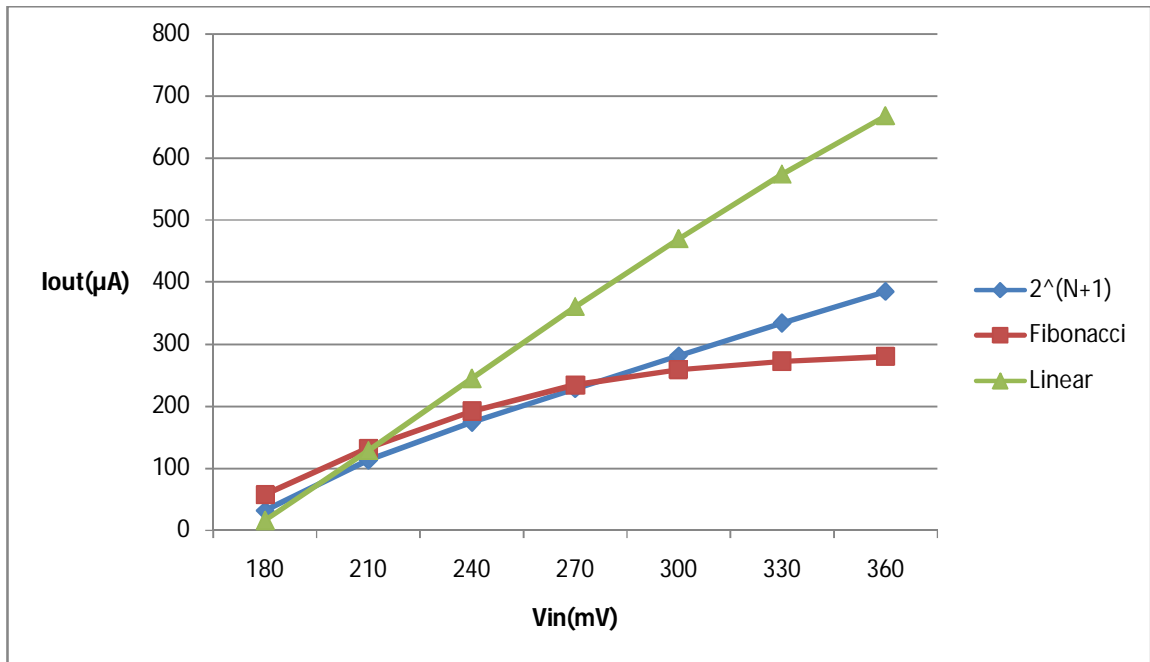Figure 4.5 Simulation plots for comparion of $2^{N+1}-1$ with Fibonacci and linear charge pump

4.7 Conclusion

The proposed $2^{N+1} - 1$ charge pump was compared with Fibonacci charge pump under slow switching condition. The mathematical proof and the simulation results prove that the 2 stage $2^{N+1} - 1$ gives higher output current than a four stage Fibonacci charge pump with equal total capacitance.

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5 Reconfigurable Charge pump

5.1 Introduction

On-chip implementation of power management units is required in micro-power energy harvesting and micro-sensor application. The power management unit, usually include integrated switched-capacitor power converters or charge pumps. The power management unit needs to be able to operate over a wide range o input voltages. Linear charge gives high current, but the gain per stage ratio is low. A Fibonacci charge pump gives high gains at lower stages. And also the proposed $2^{N+1} - 1$ gain charge pump, gives high gain at lesser stages. Reconfigurable charge pumps with, linear and Fibonacci , and linear and $2^{N+1} - 1$ have been designed to increase the input range of the power converter.

5.2 Reconfigurable charge pump with Linear and Fibonacci topology

The gain of an N stage linear charge pump is *N+1* amd that of an N stage Fibonacci charge pump is F_{N+2}, where F_N is the Nth Fibonacci number. So a four stage linear charge pump gives a gain of five, and a Fibonacci charge pump of same stages gives a gain of eight.

A reconfigurable charge pump has been designed between a four stage linear and four stage Fibonacci charge pump (shown in figure 5.1). When the control switches shown by ctrl and ctrlb are suitable operated the charge pump can be reconfigured between linear and Fibonacci charge pump. When ctrl is zero and ctrlb is one the charge pump operates in linear mode. The mode can be changed to Fibonacci by changing ctr to one and ctrlb to zero.
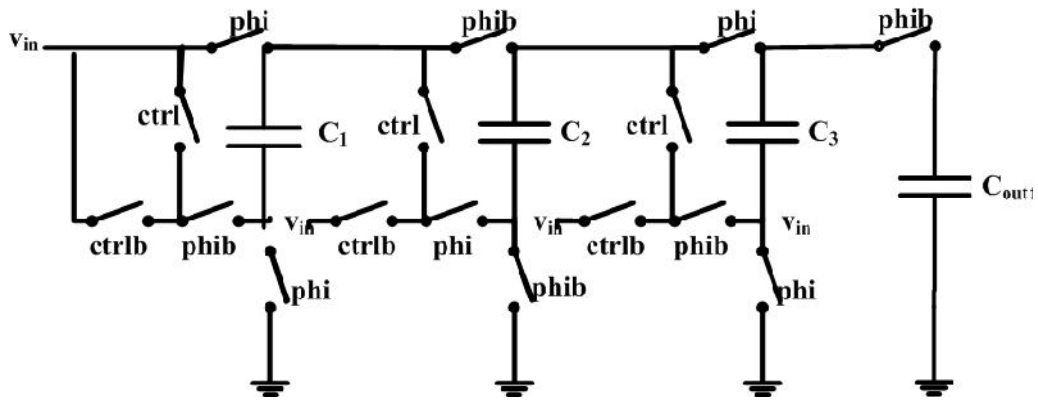
Figure 5.1 Linear and Fibonacci reconfigurable charge pump

5.3 Reconfigurable charge pump with Linear and $2^{N+1} - 1$ topology

The gain of an N stage linear charge pump is *N+1* amd that of an N stage $2^{N+1} - 1$ charge pump is $2^{N+1} - 1$. So a three stage linear charge pump gives a gain of four, and a $2^{N+1} - 1$ charge pump of two stages gives a gain of seven.

A reconfigurable charge pump has been designed between a three stage linear and two stage $2^{N+1} - 1$ charge pump (shown in figure 5.2). When the control switches shown by ctrl and ctrlb are suitable operated the charge pump can be reconfigured between linear and $2^{N+1} - 1$ charge pump. When ctrl is high and ctrlb low the circuit operates in linear mode. The two capacitors of the second stage of $2^{N+1} - 1$ are put in parallel to get a combined capacitance as in the first two stages of linear charge pump. When ctrl is low and ctrlb high the charge pump works in $2^{N+1} - 1$ mode, converting into a two stage $2^{N+1} - 1$ charge pump.
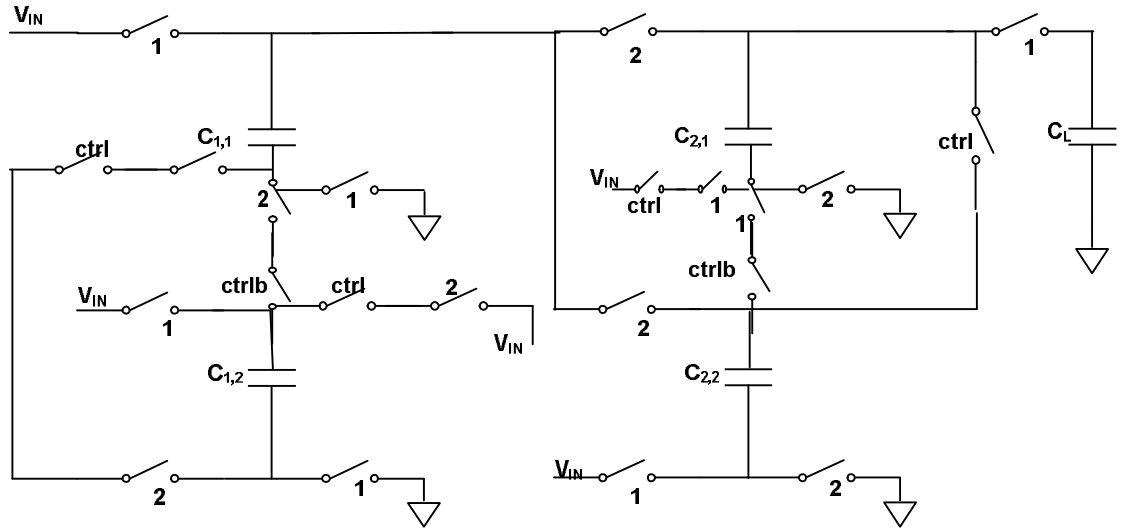
Figure 5.2 Linear and $2^{N+1} - 1$ reconfigurable charge pump

5.4 Simulation Results and Discussion

The circuit was simulated in 180nm technology. The dimensions of the switch were set at 200μm. The output of the charge pump was pumped into a large capacitor precharged to 1V. The clock buffers were also powered by this large capacitor to mimic the operation of energy harvesting circuit. The frequency of operation was varied and the frequency at which maximum current is obtained is used for tabulation.

For the reconfigurable charge pump between linear and Fibonacci charge pump, the input voltage was varied from 150mV to 390mV. Table III shows the simulation result for linear Fibonacci reconfigurable charge pump. At low voltages the reconfigurable charge pumps behavior is similar to that of the Fibonacci charge pump. At higher voltages it is run in linear mode. Figure 5.3 plots the behavior.

Table III

Vin(mV)	$I_{out\_reconfig}(\mu A)$	$I_{out\_fib}(\mu A)$	$I_{out\_linera}(\mu A)$
150	0	0	0
180	0	0	0
210	54.2	72	0
240	166	149	193
270	362	203	401
300	527	254	578
330	668	292	729
360	787	320	855
390	884	341	955
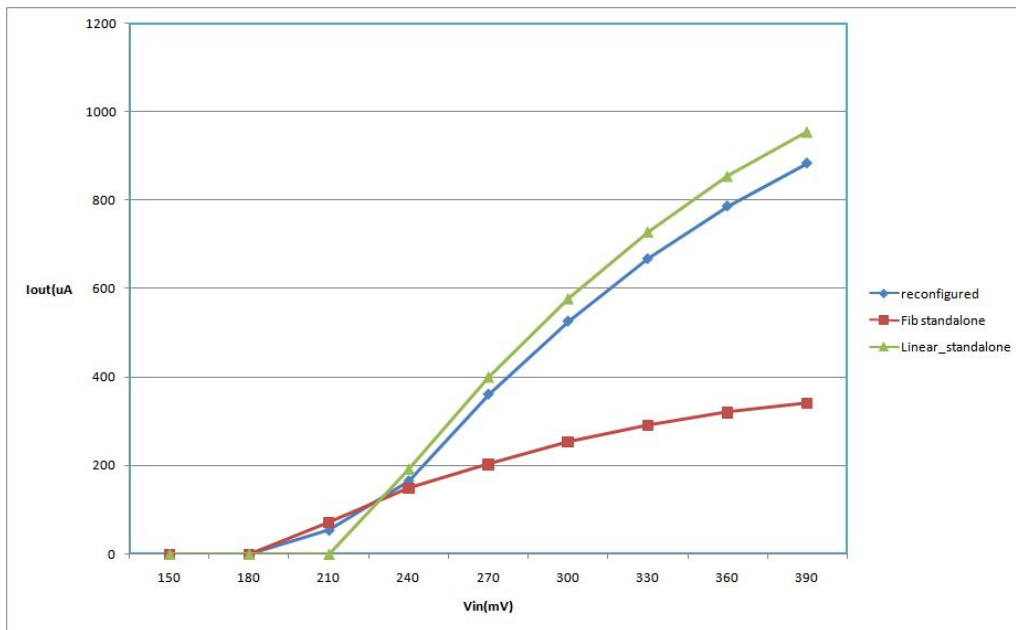
Figure 5.3. Simulation plots of Linear and Fibonacci reconfigurable charge pump

For the reconfigurable charge pump between linear and $2^{N+1} - 1$ charge pump, the input voltage was varied from 180mV to 580mV. Table IV shows the simulation result for linear Fibonacci reconfigurable charge pump. At low voltages the reconfigurable charge pumps behavior is similar to that of the Fibonacci charge pump. At higher voltages it is run in linear mode. Figure 5.4 plots the behavior.

Table IV

Vin(mV)	$I_{out\_2^{N+1}-1}$ (µA)	I_{out_linear}(µA)	$I_{out\_reconfig}$(µA)
180	0	0	0
230	197	0	132
280	385	82.7	311
330	538	402	449
380	652	702	574
430	740	918	768
480	785	1040	893
530	809	1110	953
580	823	1140	985
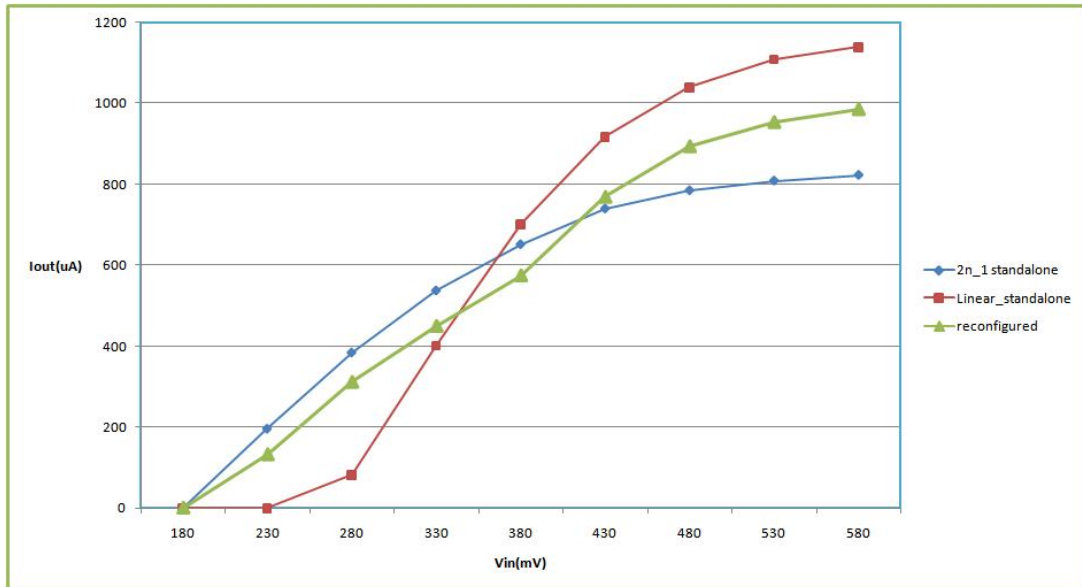
Figure 5.4. Simulation plots of Linear and $2^{N+1}-1$ reconfigurable charge pump

5.5 Conclusion

The reconfigurable charge pump between linear and Fibonacci and between linear and $2^{N+1}-1$ charge pump has been designed. The reconfigurability between two topologies increases the input voltage range of charge pump. The energy harvesters with these kind of charge pump will be able to harvest power from a wider range f voltages

6. Conclusion and Future work

6.1 Conclusion

We have presented a comprehensive view on the micro scale energy harvesting system, which can effectively function as energy source for ultra-low power systems. The system offers a perennial power source to low power wireless devices to work completely autonomous. The thesis has emphasized the development of the sensor circuit for suitable enabling of the system. The battery management unit ensures the voltage is within the safe operating region determined by the undervoltage and overvoltage thresholds of the battery. The start up circuit designed helps recharge the battery when the battery goes below under voltage. The new topology of charge pump gives higher gain for lower stages decreasing the switch loss when operating at very low voltages. The reconfigurable charge pump improves the voltage range of the power converter. The circuits have been designed and performance of the system is verified using 0.18 m CMOS process.

6.2 Future Work

- Tape out of the, complete energy harvesting system, with the sensor, battery management unit and start up circuit. Testing the system in real environment.
- Design of charge pump topology, which can give gains over various range.
- Integration of other energy sources like vibration and RF energy harvesting into the designed energy harvesting system.
- To design the energy harvesting chipset to support specific application. With an understanding of the energy requirement of the application.

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