SPUR REDUCTION IN PHASE LOCK LOOP USING CHARGE PUMP CURRENT MATCHING TECHNIQUE

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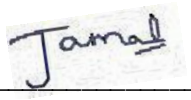
I declare that this written submission represents my ideas in my own words, and where others' ideas or words have been included, I have adequately cited and referenced the original sources. I also declare that I have adhered to all principles of academic honesty and integrity and have not misrepresented or fabricated or falsified any idea/data/fact/source in my submission. I understand that any violation of the above will be a cause for disciplinary action by the Institute and can also evoke penal action from the sources that have thus not been properly cited, or from whom proper permission has not been taken when needed.



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Approval Sheet

This thesis entitled SPUR REDUCTION IN PHASE LOCK LOOP USING CHARGE PUMP CURRENT MATCHING TECHNIQUE by Jamal MD is approved for the degree of Master of Technology from IIT Hyderabad.

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I would like to thank my parents and friends for their all-round support of my life, but especially of my education.

Abstract

A clock with high spectral purity is required in many applications. The spectral purity of the clock source is critical for the overall system performance. Phase locked-loops (PLLs) are commonly used to generate well-timed on-chip clocks in high performance. The most important application of the phase locked loops (PLL) is for clock generation and clock recovery in microprocessor, networking, communication systems, ADCs to accurately define sampling moments and frequency synthesizers. The concept of PLL technique was first described in 1932. Since the invention of PLL, design of PLL has remained challenging because of requirements such as fast operation, low power consumption, less noisy electronic equipment's. Phase Frequency Detector (PFD), Charge pump and Voltage Controlled Oscillator (VCO) are the non-ideality components of PLL.

But, non-ideality's in PLL introduces charge pump current mismatch, current sharing, switching delays and leakage which will produce the phase offset. Produced phase offset gives rise to phase noise, frequency inaccuracy, spur sidebands and increases settling time of the PLL. Spurs cause reciprocal mixing of the neighbor channels to the pass band of the IF filter or translate to deterministic jitter and degrade the signal-to-noise ratio. The clock source is often required to have low spurious tones, Typical systems require all sidebands be approximately -72dB below the carrier. Charge pump with matched currents will reduce the phase offset, reduction in the phase offset will reduce the spur in the PLL. Charge pump is designed with matching currents of the charge currents using the cascode current mirror and wilson current mirror. Amount of spur produced in the PLL by using cascode current mirror charge pump is -84.2 dBc and using wilson current mirror charge pump is -85.03 dBc respectively. The circuits have been designed and performance of the system is verified using 0.18μm CMOS process.

Contents

Chapter 1

Introduction

PLL is used for high accuracy clock in on chip. In most wireless communication systems require local oscillators for up-conversion and down-conversion of their transmitted and received signals and in analog-to-digital converters (ADC) to accurately define the sampling moments [1].

The concept of PLL technique was first described in 1932, in a paper by Henri de Bellescize, in the French journal L'Onde Électrique [2]

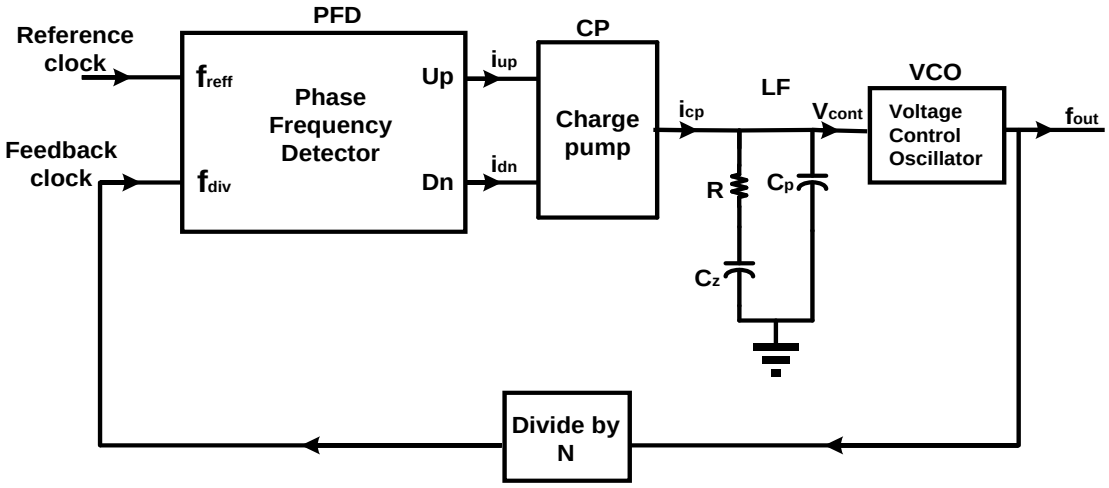

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Figure 2.1 - Block diagram of PLL

Charge pump PLL offers two important advantages over the XOR/LPF PLL approach. The capture range is only limited by the VCO output frequency range. The static phase error is zero if mismatches and leakage are negligible [3].

1.1 Working of PLL

A PLL is a closed-loop feedback system that sets fixed phase relationship between its output clock phase and the phase of a reference clock. A PLL is capable of tracking the phase changes that falls in this bandwidth of the PLL. A PLL also multiplies a low-frequency reference clock to produce a high-frequency clock F_{out} this is known as clock synthesis.

A PLL has a negative feedback control system circuit. The main objective of a PLL is to generate a signal in which the phase is the same as the phase of a reference signal. This is achieved after any iterations of comparison of the reference and feedback signals. In this lock mode the phase of the reference and feedback signal is zero. After this, the PLL continues to compare the two signals but since they are in lock mode, the PLL output is constant [4].

Phase Lock Loop (PLL) consists of Phase frequency Detector (PFD), Charge pump, Loop filter (LF), Voltage Controlled Oscillator and Divide by N circuit. PFD consists of two inputs signals one of the inputs is from the reference clock signal and another signal is feedback signal from the divide N circuit.

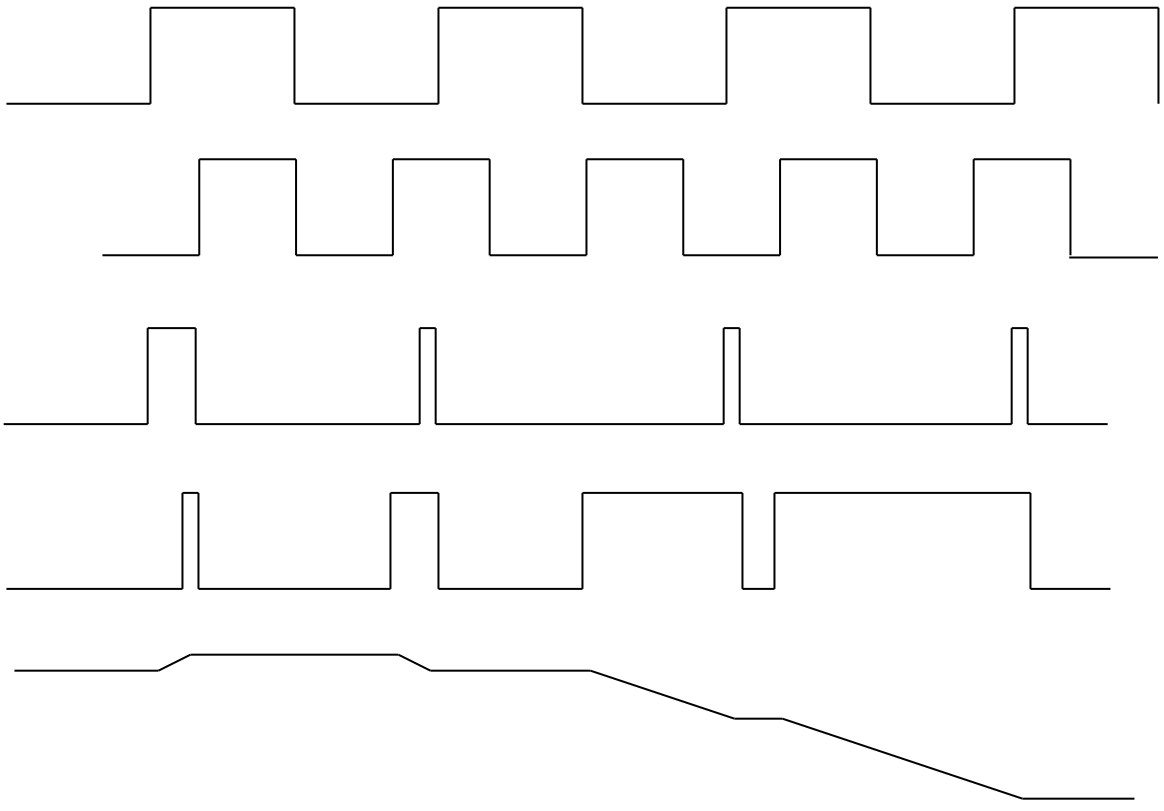


Figure 1.2 – Transient response of components of the PLL

1.1.1 Phase Frequency Detector

The "Phase frequency Detector" (PFD) is one of the main part in PLL circuits. It compares the phase and frequency difference between the reference clock and the feedback clock [5] . Depending upon the phase and frequency deviation, it generates two output signals "I_{up}" and "I_{dn}" respectively. Figure 1.2 shows the working of the PFD. Phase Detector can be implemented by simple XOR Gate.

1.1.2 Charge pump and Loop filter

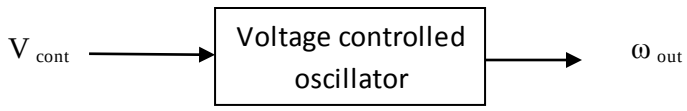
Charge pump is used to convert the phase or frequency difference information into a voltage using a loop filter which is used to tune the VCO. Charge pump circuit is used to combine both the outputs of the PFD and give a single output which is fed to the input of the filter. Charge pump circuit gives a constant current of value i_{cp} which should be insensitive to the supply voltage variation. The amplitude of the current always remains same but the polarity changes which depend on the value of the "UP" and "DOWN" signal. "V_{cont}" is the output voltage of the charge pump [16] shown in the figure 1.2 and loop filter is used to filter the wanted signal and voltage is used for the input to the VCO for the tuning to appropriate frequency.

1.1.3 Voltage Controlled Oscillator

Voltage controlled Oscillator is an electronic oscillator designed to be controlled in oscillation frequency by a voltage input. Most applications require that oscillators to be tunable i.e., their output frequency is a function of control input voltage. An ideal voltage-controlled oscillator is a circuit whose output frequency is a linear function of its control voltage [6].

$\omega_{out} = \omega_0 + K_{vco} V_{cont}$

Here, ω_0 represents the frequency of VCO at $V_{cont}=0$ and K_{vco} denotes the gain or sensitivity of the VCO expressed in rad/s/v or Hz/v and ω_{out} is VCO output frequency,



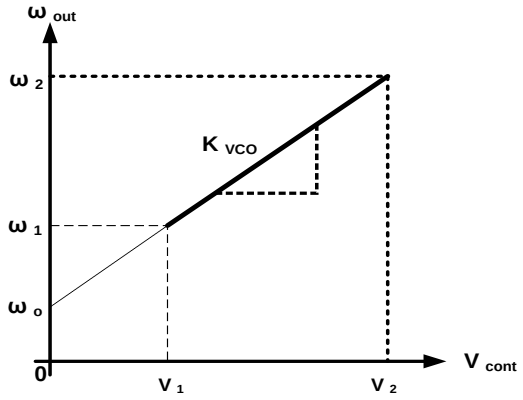


Figure 2.2.3.1 - Variation of frequency to control voltage of VCO

The achievable range, ω_2-ω_1 is called the "tuning range" [7].

$$\omega = \frac{d\phi}{dt}$$

Where ω-frequency, ϕ-phase and also $\phi = \omega\, dt + \phi_0$

Output voltage of VCO is

$V_{out}(t) = V_m \cos(\omega_{out}\, dt + \phi_0)$

Where $\omega_{out} = \omega_0 + K_{vco} V_{cont}$

Therefore $V_{cont} = V_m \cos(\omega_0 t + K_{vco} V_{cont}\, dt + \phi_0)$

The argument under cos is phase of Vout and excess phase term is

$\phi_{ex} = K_{vco} V_{cont}\, dt$ where $K_{vco} = \frac{f_{max} - f_{min}}{V_{max} - V_{min}}$ Hz/V

1.1.4 Frequency divider (N)

The frequency divider in the PLL circuit forms a closed loop. The output of the VCO is fed back to the input of PFD through the frequency divider circuit. It scales down the frequency of the VCO output signal.

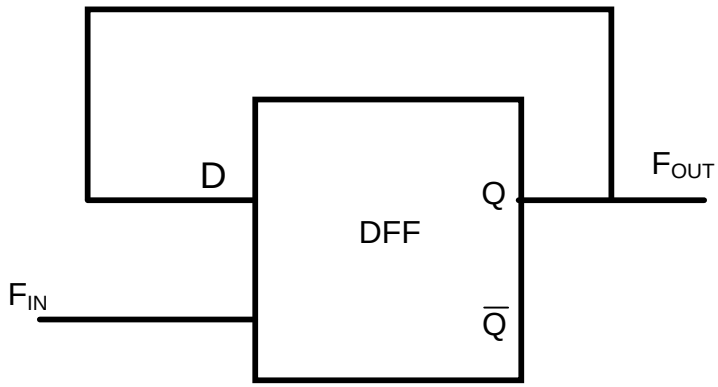


Figure 2.2.4.1 simple divide by 2 circuit using D-Flip Flop

Counter will acts as the frequency divider and a simple D-flip flop will acts as divider by 2 circuits and these frequency divider can be implemented by the programmable counter for accurate division of the frequency**.**

1.2 Aim and Motivation

PLL is used to generate clock with high spectral purity is required in many applications such as clock generation and clock recovery in wireless communications to up convert and down convert the wanted signals, microprocessor, networking, communication systems, and frequency synthesizers. The concept of PLL technique was first described in 1932. Since the invention of PLL, design of PLL has remained challenging because of non-idealities in the PLL such as Phase Frequency Detector (PFD), Charge pump and Voltage Controlled Oscillator (VCO). These non-idealities these components produce phase offset in PLL, which will leads to spurs at the spectrum of the VCO. Phase offset can be decreased by designing charge pump with matched currents. Spur is reduced by decrease in the phase offset.

1.3 Literature Survey

Spurs are part of the system we cannot eliminate but we can suppress these spurs. To reduce the spurs in the PLL there are many techniques are presented among them “Spur Reduction Techniques for Phase-Locked Loops Exploiting A Sub-Sampling Phase Detector” by Xiang Gao [8]. In this reduction spur by subsampling PFD, Spur Reduction in Wideband PLLs by Random Positioning of Charge Pump Current Pulses is the another technique to reduce the spur in the pll by nagendra krishnapura [9] in this a charge

pump random with position is proposed and reduce the spur in the PLL. Charge pump with perfect current matching characteristics in phase-locked loops by Jae-Shin Lee in this the amount of reference spur reduces is less than the -75dBm [10]. We are proposing the charge pump with the spur well of -80.12 for the charge pump using the cascode current mirror and spur well of -82.35 for the charge pump using the super wilson current mirror.

1.4 Contribution of the Thesis

This work focuses on the design and implementation of charge pump with current matching will reduction Spur in Phase Lock Loop (PLL). The main contributions of this research work are as follows:

A comprehensive analysis of the key performance parameters of charge pumps.

A comprehensive study about spurs, its causes and effects.

A novel charge pump design with matching current will reduce the spur in PLL.

1.5 Thesis Organization

• **Chapter 1:** Introduction describing the motivation behind the work, literature survey, objectives explores Block diagram and Working of the PLL and importance of PLL in the various applications and contributions of the present work.

• **Chapter 2:** Introduction to various spurs and its causes.

• **Chapter 3:** Phase Frequency Detector working and its importance in the PLL.

• **Chapter 4:** Performance of charge pump circuits

• **Chapter 5:** Design and performance of a novel current matched charge pump technique for reducing Spur in PLL.

• **Chapter 6:** presents the conclusion to the thesis as well as future directions of this work.

Chapter 2

Causes of Spur in PLL

2.1 Introduction

Spurs are the unwanted sidebands which occur at multiple comparison frequencies of VCO. Spurs are caused in the PLL by periodic disturbance of the Voltage Controlled Oscillator by the sampling at the reference frequency and due to phase offset present at the tuning line of the VCO.

Reference spurs and Non-Reference spurs are two types of Spurs. Reference spurs will appear at multiples of the comparison frequency and these are the most common spurs in the PLL. Non-Reference spurs are mainly caused in the dual PLL. These spurs are shown and explained in order to aid in troubleshooting [11].

2.2 Reference spurs

Reference spurs are caused due to mismatch and the leakages in the components of PLL and mainly caused due to the mismatches and leakages charge pump [11]. At low comparison frequency amount of spur is dominated by leakage currents and mismatches are dominated at the higher comparison frequency.

2.2.1 Spur due to leakage

Source of leakage in PLL is from charge pump, VCO, capacitors from loop filter and even from the board also. When the PLL is in the locked condition, the charge pump will put out short alternating pulses of current with long periods in between at which the charge pump is tri-stated. This will cause the phase offset, because of this offset there will be spur in the output spectrum of the voltage controlled oscillator.

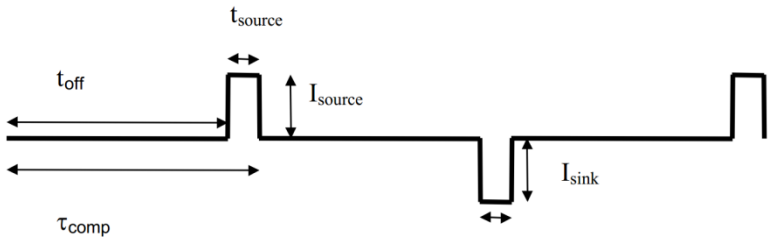


Figure 2.2.1 - Output of the charge pump when PLL is in locked condition

When PLL is in the locked condition then ideally charge pump current should equal to zero and offer infinite impedance. Leakage is more dominate at the lower reference frequencies because the period that the charge pump has to leak is longer, since the comparison frequency period, t_{comp} is longer. Leakage due charge pump is dependent on temperature and output frequency. Spur due to leakage increases as temperature increases and decreases as output frequency increases.

There are six short- channel leakages present in the deep micron MOSFET transistors [12], they are

i. Reverse-bias p– n junction leakage.
ii. Sub threshold leakage or the weak inversion cur-rent across the device.
iii. Gate leakage or the tunneling current through the gate oxide insulation.
iv. Gate current due to hot-carrier injection.
v. Gate-induced drain leakage (GIDL)
vi. Channel punch through current.

Phase offset due to the leakage current (I_{leak}) is

Phase offset $(\Phi_{\varepsilon_{leak}}) = 2\pi \frac{I_{leak}}{I_{cp}} \quad [rad]$

Spur $(P_r) = 20\log \frac{\sqrt{2}\frac{I_{cp}R}{2\pi} * \Phi_{\varepsilon_{leak}} * K_{vco}}{2f_{ref}} - 20\log \frac{f_{ref}}{f_{pl}} \quad [dBc]$ [13]

P_r is the amount of spur level in dBc, I_{cp} is the charge pump current f_{ref} is the reference frequency, R is the resistor in the loop filter, f_{pl} pole frequency and K_{vco} is the sensitivity gain of the VCO.

Leakage current of 1nA amount of spur [14].

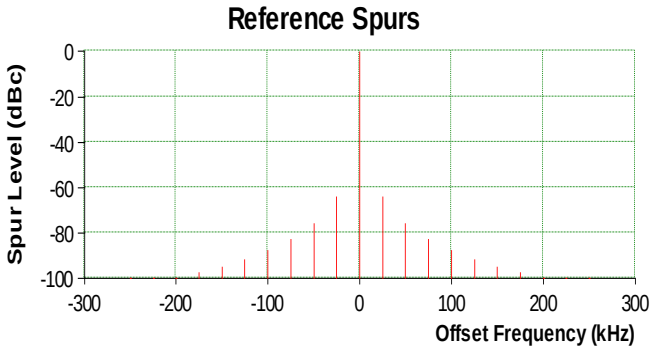


Figure 2.2.2 - Variations of spur for charge pump mismatch current

Leakage current of 25nA amount of spur

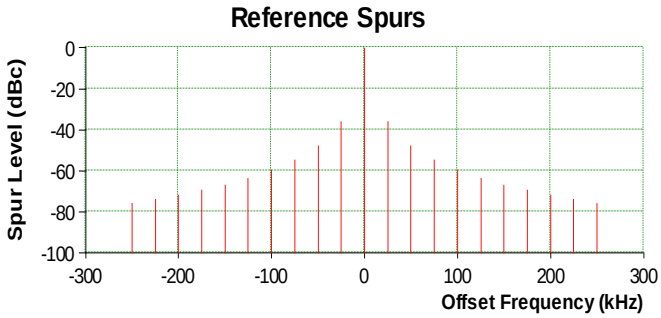


Figure 2.1.3 - Variations of spur for charge pump mismatch current

Leakage in the PLL can be reduced by good layout components of the loop filter, low leakage MOSFET, use capacitors with good leakage properties, use sealants if necessary to protect the board against humidity and keep board in clean and use VCO with low leakage.

2.2.2 Spur due to mismatch

Charge pump mismatch is another cause for the reference spur. When I_{source} and I_{sink} have the non-zero difference between them is known as the charge pump mismatch.

$$\text{mismatch } \% = 200\% \frac{I_{source} - I_{sink}}{I_{source} + I_{sink}}$$

From the figure 2.1, the net charge delivered when the charge pump is sourced current will be equal to the net charge delivered when the charge pump is sinking current. In the other words $\boldsymbol{I_{sink} * t_{sink} = I_{source} * t_{source}}$. The current is sourced by a PMOS device and sink by a NMOS device. The currents that are sourced and sink are not constant. The sourced current decreases as the tuning voltage is increased while the current sunk by the NMOS device sinks more current. The net effect of this is the mismatch varies as a function of the tuning voltage and increases with increasing tuning voltage. By this phase offset is introduced in the charge pump that leads to the spur in the output spectrum of VCO.
Phase offset due to mismatch current is[13]

$$\text{Phase offset } (\boldsymbol{\Phi_{\varepsilon_{mis}}}) = \boldsymbol{2\pi \frac{\Delta t_{on}}{t_{cp}} * \frac{\Delta i}{i}} \quad [\boldsymbol{rad}]$$

$$\text{Spur } (\boldsymbol{P_r}) = \boldsymbol{20\log} \frac{\overline{2}\frac{I_{cp}R}{1\pi} * \Phi_{\varepsilon_{mis}} * K_{vco}}{2f_{ref}} - \boldsymbol{20\log}\frac{f_{ref}}{f_{pl}} \quad [\boldsymbol{dBc}]$$

P_r is the amount of spur level in dBc, Δi is the mismatch current of the charge pump, Δt_{on} is the turn on time of the PFD, I_{cp} is the charge pump current f_{ref} is the reference frequency, R is the resistor in the loop filter, f_{pl} pole frequency and K_{vco} is the sensitivity gain of the VCO.

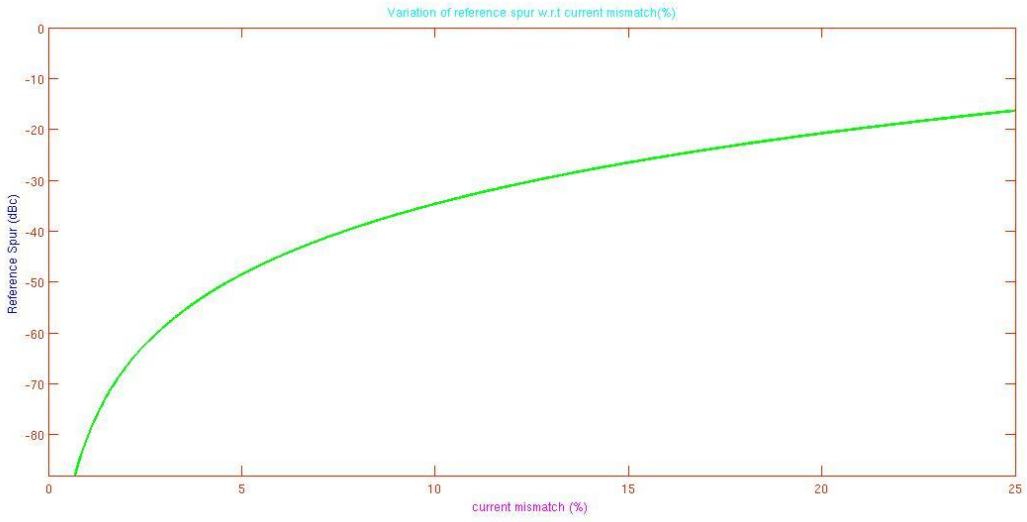


Figure 2.2.1 - Variations of spur for charge pump mismatch current\

2.3 Non-Reference Spurs

Crosstalk and Non-crosstalk related spurs are the two categories of the Non-References spurs. Crosstalk related spur is caused by some other signal or signals which effects on the output of the VCO. Non-Crosstalk related spur refer to spurs that are caused by some inherent behavior in the PLL. Common sources of crosstalk related spurs are the other side of a dual PLL, computer monitors, crystal oscillator and its harmonics and other frequencies on the board.

2.3.1 Auxiliary PLL Crosstalk Spur

This spur is seen at frequency spacing from the carrier equal to the difference of the frequencies of the main and auxiliary PLL of the dual PLLs on the board. Parasitic capacitances on the board can allow high frequency signals to travel from one trace on the broad to another. Since auxiliary PLL cause spur in the main PLL the spur related to this is called as Auxiliary PLL Crosstalk Spur.

2.3.2 External Crosstalk spurs

This spur is caused by long traces on the board and parasitic capacitances on the board and this can be act as antenna for noise. This could be things such as 31.25 KHz refresh rate on some computer monitors or higher frequencies. This type of spur is caused by some frequency source external to the PLL. This can be reduced good layout and remove or isolate the PLL from the signal source.

2.3.3 Fractional N Spurs

This spurs will be seen in the Fraction N PLL. Fraction N Spur are caused due to instantaneous phase error introduced by the fractional N averaging because, while averaging involves switching the N counter value between 2 different values. Fractional N parts have a lot of the part-specific spur causes. These spur occurs at the fractional modulus times the comparison frequency from the carrier and are very dependent on the fractional modulus and this spur is easy to identify.

2.3.4 Greatest common multiple Spurs

This spur occurs at the greatest common multiple of the two comparison frequencies comparison corresponding to the even that both charge pumps come on at the same time. This result in considering periods of the two comparison frequencies when both charge pumps come on, they produce noise, especially at the Vpp lines, which gives rise to spur. This spur occurs in a dual PLL at the greatest common multiple of the two comparison frequencies.

2.3.5 Prescaler Miscounting Spurs

This spur is caused by the prescaler miscounting. Miscounting prescaler is caused due to poor matching to the high frequency input, violation of the sensitivity specifications for the PLL and VCO harmonics. These spurs will occurs mostly at half the comparison frequency and it can also occur at one-third, two-thirds or the fractional multiple of the comparison frequency. This spur can be reduced by putting an inductor to match the imaginary part of the PLL input impedance at the operating frequency can usually fix impedance matching issues. Sensitivity and matching to the VCO harmonics are also cause a miscount in prescaler. Try to keep the VCO harmonics -20 dbm or lower in order to reduce the charge of the PLL miscounting the VCO harmonic.

Spurs are part of the system we cannot eliminate but we can suppress these spurs

SNR < minimum desired signal/maximum noise* LO spurs

LO spurs < minimum desired signal/maximum noise*SNR

Spurs will degrade the signal to noise ratio. PLL jitter at high damping factor causes periodic jitter from the phase detector spur. As the distribution deviates from Gaussian, the error due to dead zone increases.

Present PLL manufactured by national semiconductors produces spur level about -75dBm.

2.4 Effects of Spur on performance of PLL

w_{LO} is the center frequency of oscillator, w_s side bands (spur) of the oscillator and w_O desired signal to transmit in RF transmitter, w_{inf} is the interfere frequency. Figure 2.4.1 shows the frequency representation of the signals. When a signal is transmitted and in the receiving figure 2.4.2 shows at the IF frequency the received signal strength is degraded because of the spur at the sidebands of the oscillator. Spur decreased the signal to noise ration of the desired signal at the receiver [15].

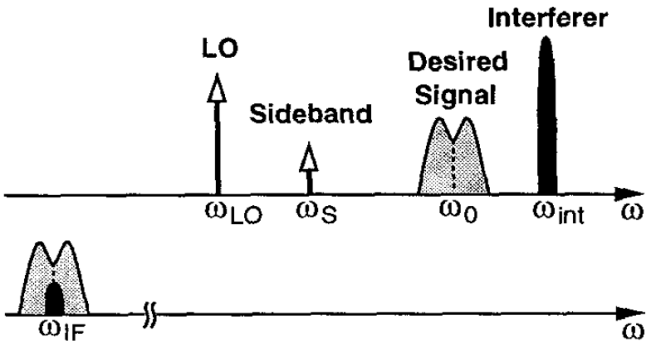


Figure 2.4.1 frequency representation of desired ,oscillator and sidebands

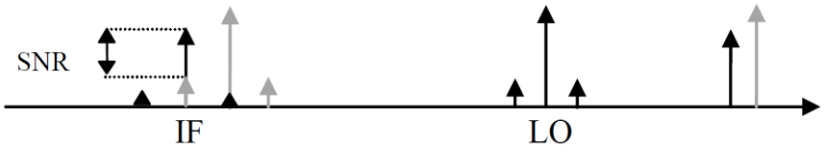


Figure 2.4.2 effect of sidebands on desired signal to reduce SNR ratio

2.5 Output spectrum of the PLL with Spur

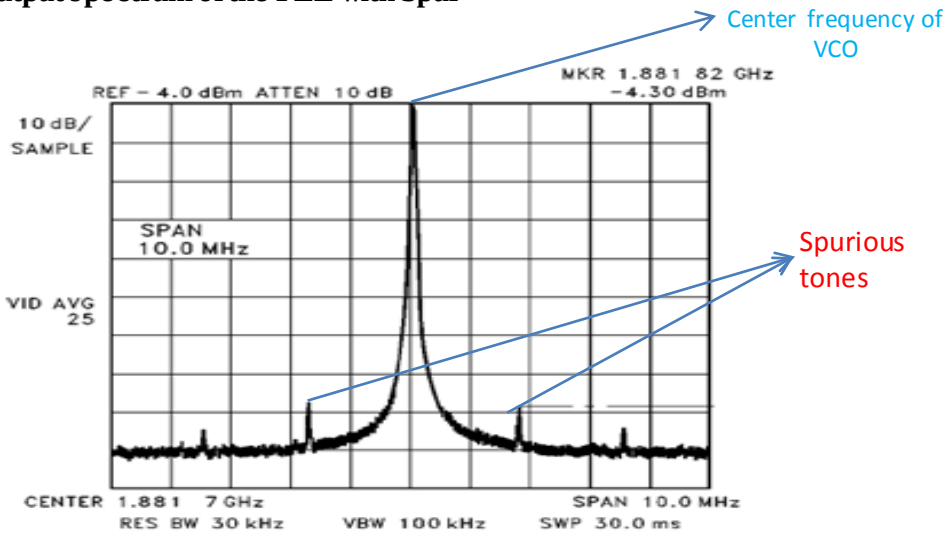


Figure 2.5.1 frequency spectrum of the oscillator along with sidebands

2.6 Calculation of spur from the output spectrum of the VCO

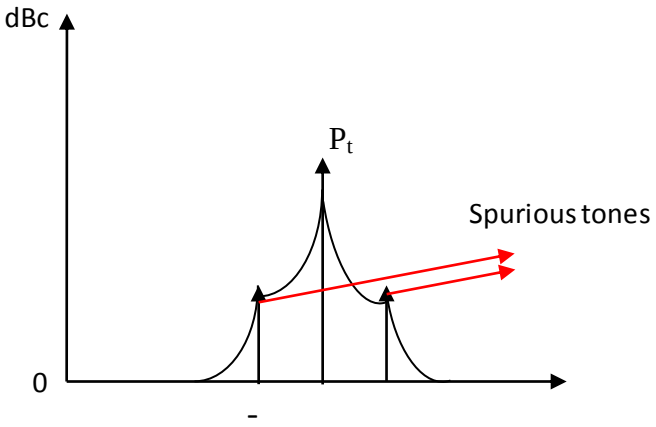


Figure 2.6.1 representation of spur in the spectrum of the VCO

Amount of spur can be calculated as

$$Spur \quad dBc \quad = 10 \log \frac{P_s}{P_t}$$

where P_s and P_t represents the power of the sidebands frequency and central frequency of the oscillator respectively at the output spectrum of the VCO.

Chapter 3

Phase Frequency Detector (PDF)

3.1 Introduction

The “Phase frequency Detector” (PFD) is one of the main part in PLL circuits. It compares the phase and frequency difference between the reference clock and the feedback clock. Depending upon the phase and frequency deviation, it generates two output signals “Iup” and “Idn”.

3.2 Phase detector

Phase Detector is used to detect the phase difference between the two signals of same frequency. XOR gate is used as the simple phase detector between the signals.

Let A and B are the two inputs to the XOR gate with some phase difference between them and the output is the phase difference between the A and B [17].

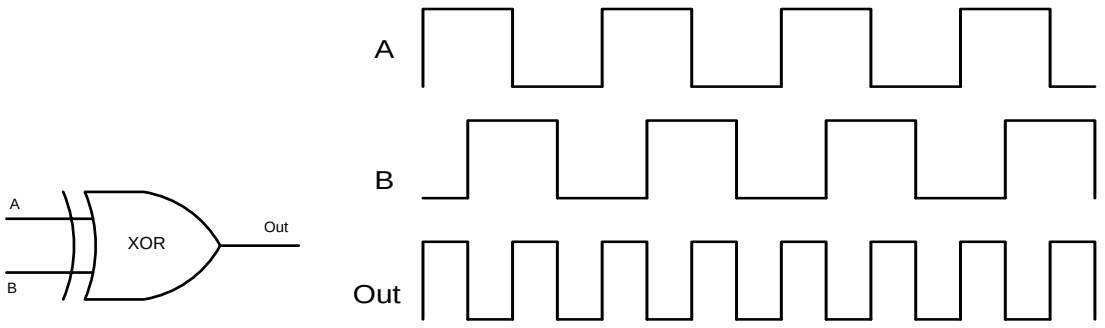


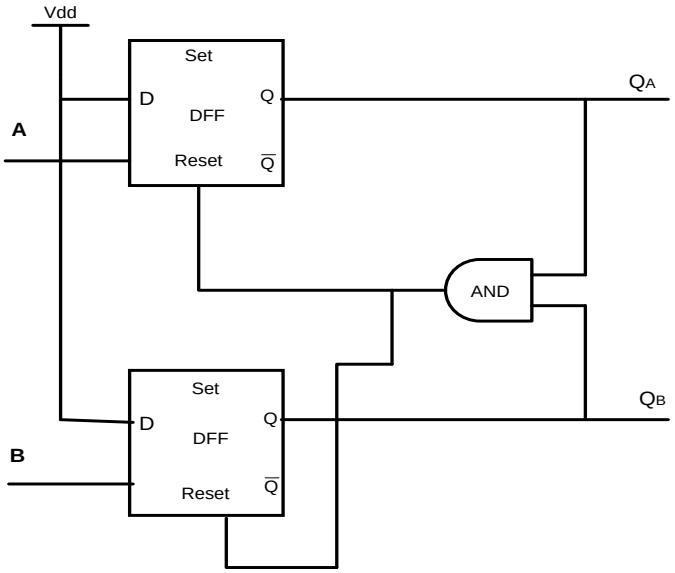
Figure 3.2.1 - Simple Phase detector and its waveform

If there is a phase difference between the two signals, it will generate “Iup” or “Idn” synchronized signals. When the reference clock rising edge leads the feedback input clock rising edge “Iup”

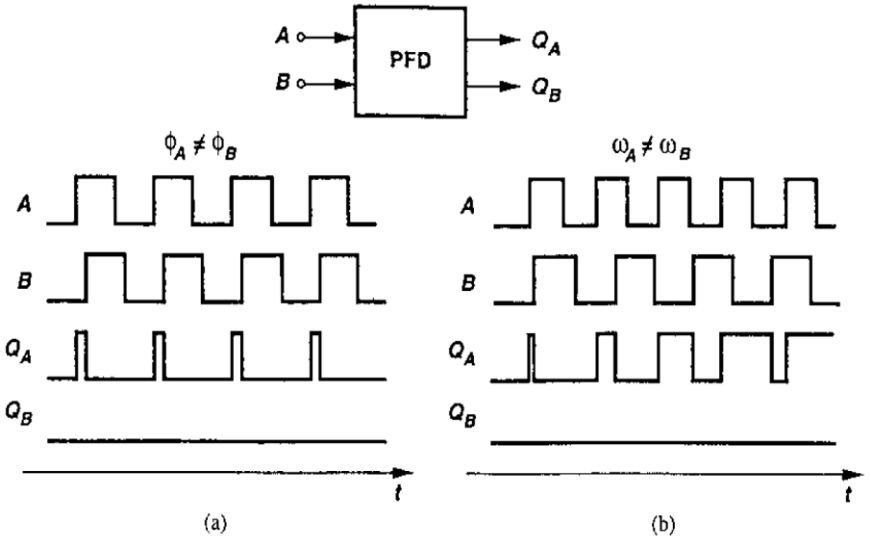
signal goes high while keeping “Idn” signal low. On the other hand if the feedback input clock rising edge leads the reference clock rising edge “Idn” signal goes high and “Iup” signal goes low.

Fast phase and frequency acquisition PFDs are generally preferred PFDs.

Figure 3.2.1 shows a traditional PFD circuit and figure 3.2.2 shows the working of the PDF for inputs signal with same frequency with phase difference and difference in frequencies of the signals. In the figure A and B represents “reference clock” and “feedback clock” respectively and QA and QB represents “Iup” and “Idn” respectively.



3.2.1 - Block Diagram of PDF



3.2.2 - Output Wave forms of the PFD

PFD consists of the two d-Flip flops with their D inputs tied to logical ONE and circuit is connected as shown in the above. Suppose two waveforms A and B arrive at input pins with equal frequency but unequal phases such that A leads B. As A goes high, output QA goes high. When leading edge of B comes, QA goes to zero while QB does not show any change and remains low. Exactly opposite thing happens when B leads A. Thus output QA continues to produce pulses whose width is proportional to |ΦA- ΦB| while QB remains at zero. Now as shown in below suppose A has higher frequency than B and also A leads B, then QA continues to produce the pulses with unequal width and QB remains quite and vice versa. Thus, the dc contents of QA and QB provide information about phase or frequency difference. If QA=QB=1 and A goes high, QA rises. If this event is followed by a rising transition on B, QB also goes high and the AND gate resets both flip-flops. In other words, QA and QB are simultaneously high for a short time but the difference between their average values still represents the input phase or frequency difference correctly.

3.2.1 Dead Zone

Dead zone is a main property in the PFD phase characteristics as it introduces jitter to the PLL system. The PFD doesn't detect the phase error when it is within the dead zone region, then PLL locks to a false frequency [18].

Dead-zone is due to small phase error. When the phase difference between PFD's input signals, the output signals of the PFD will not be proportional to this error. The reason of this problem is the delay time of the internal components of the flip-flop and the reset time that need s the AND gate to reset both flip flops.

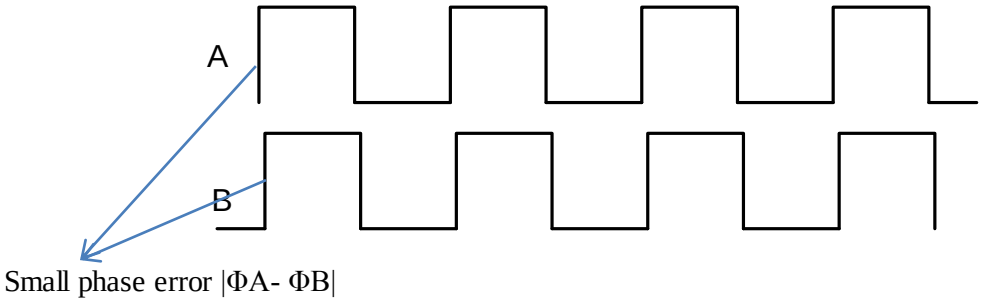


Figure 3.2.1.1 - Dead zone

Figure 3.2.1 illustrates the dead zone problem. When the two clocks are very close to each other (small phase error), due to the delay time the reset delay, the output signals UP and DOWN will not be able to charge and no output will signal leading to losing this small difference.

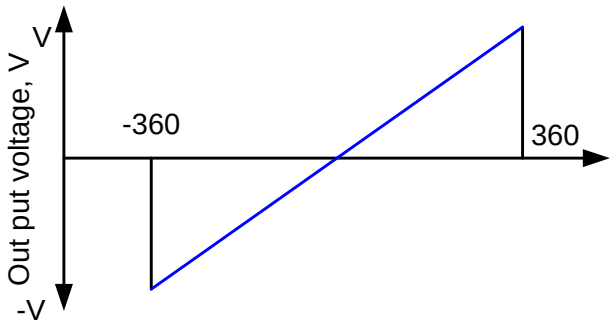


Figure 3.2.1.2 - Phase error vs. Output voltage with no Dead zone

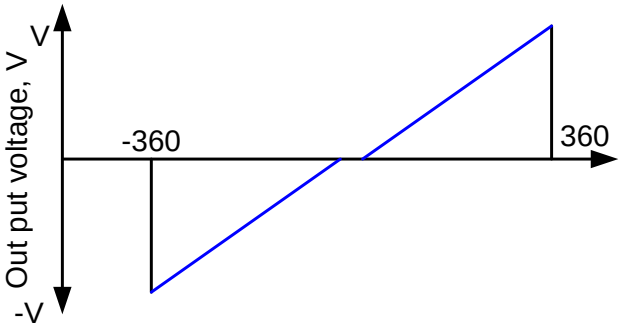


Figure 3.2.1.3 - Phase error vs. Output voltage with Dead zone

Figure 3.2.2.1 illustrates the output voltage vs. the phase error measured by the PFD. Figure.4a illustrates the relation in no dead zone PFDs, while figure 3.2.1.3 illustrates the relation in the presence of a dead zone. We can see that in a dead zone PFDs the relation become nonlinear around zero. This is due to inability to detect the phase error in this region. Plenty of solution has been done for this problem some of them reduce the delay time in the internal components of the PFDs, other solution eliminate the reset path by implementing new reset techniques that will not create a delay and produce a high speed PFDs.

Chapter 4

Charge Pump (CP)

4.1 Introduction

Charge pump is a three position electronic switch which is controlled by the three states of PFD.

Charge pump contains two inputs which are the digital output of the PFD, according to the inputs it will provide single output voltage using the loop filter, which is the given as tuning voltage of the VCO.

4.2 Simple Charge pump

Charge pump consists of two switches S1 and S2 which are connected to by QA and QB pulses respectively these pulses are the outputs of the PFD. Charge pump is connected capacitive load which is act as the loop filter. The amount of the current produced for the QA and QB pulses when they are high is Iup and Idn respectively and Iup and Idn have equal magnitude but have opposite sign [17]-[20].

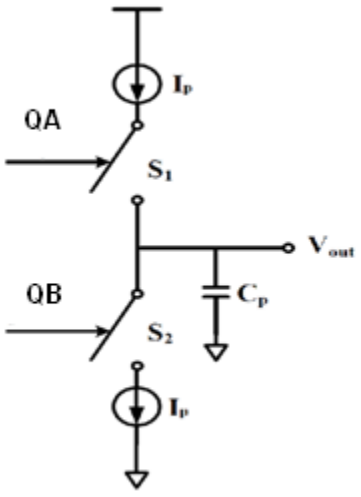


Figure 4.2.1 - Simple charge pump

If QA=QB=0, then S1 and S2 are off and Vout (or Vcont) remains constant. If QA is high and QB is low, then Iup (UP current) charges Cp. Conversely if QA is low and QB is high, then Idn (DOWN current) discharges Cp. Hence, if suppose, A leads B, then QA continues to produce pulses and Vcont rises steadily. Iup and Idn are also called as I source and I sink respectively because of its nature.

QA	QB	Current	Input VCO voltage
0	0	N	Constant
0	1	Idn	Decreases
1	0	Iup	Increases
1	1	R	constant

Figure 4.2.2 - Tabulation of the charge pump currents and VCO input voltage

4.3 Types of charge pump

Single ended and differential ended Charge pump are the two types of the charge pump. Single ended charge pump are which will have only two input and these inputs are connected individually, differential ended charge have differential inputs so there will be totally 4 inputs for the charge pump.

Advantages of Differential Charge Pumps:

1. The switching mismatch between NMOS and PMOS does not affect the overall performance substantially. The matching requirement between NMOS and PMOS transistors are relaxed to the matching between NMOS or between PMOS transistors respectively.
2. The differential CP uses switches using NMOS and the inverter delays for UPb and DNb signals do not generate any offset due to its fully symmetric operation.
3. This configuration doubles the range of output voltage compliance compared to single ended charge pump.
4. Differential stage is less sensitive to the leakage current since leakage current behaves as common mode offset with the dual output stages.

Limitations of Differential Charge Pumps:

Though differential CP has many advantages listed above, they suffer from critical drawbacks. They require two loop filters and common mode feedback circuitry. Since more number of transistors is required, with two or more current sources, they occupy large silicon area. This also leads to higher power consumption.

Limitations of Single Ended Charge Pumps:

1. Switch mismatch, clock feed through, charge sharing problems are still not eliminated fully.
2. Limited output voltage compliance range. For source CP shown above if we want higher output voltage we have to increase the charging and discharging current values.
3. Switch mismatch also results in timing mismatch as well as dead zone.
4. Parasitic capacitances are dominant in single ended CP. Using of OP-Amp may solve above mentioned problems; but designing of OP-Amp it itself tedious process and also increases unnecessary hardware.

Even though single ended charge pump has these disadvantages, they are more popular than differential design, because they do don't require two loop filter and offer tri state operation with lower power consumption. Also the problems listed above are not those much difficult to handle. With proper modification into the architecture, these problems can be eliminated or minimized easily. Also, single ended charge pumps require fewer components than differential charge pumps; hence they occupy less area in a chip. In the next session we will discuss the different architectures of single ended charge pumps with their simulation and comparison.

4.4 Switching of charge pump

Charge pump can design by different kinds of switching, they are Drain switching, Gate switching and Source switching charge pump [21]. Depending on the switching charge pump will have the different properties Switching time, power consumption, delays, cost of implementation and cost of complexity.

4.4.1 Drain switching charge pump

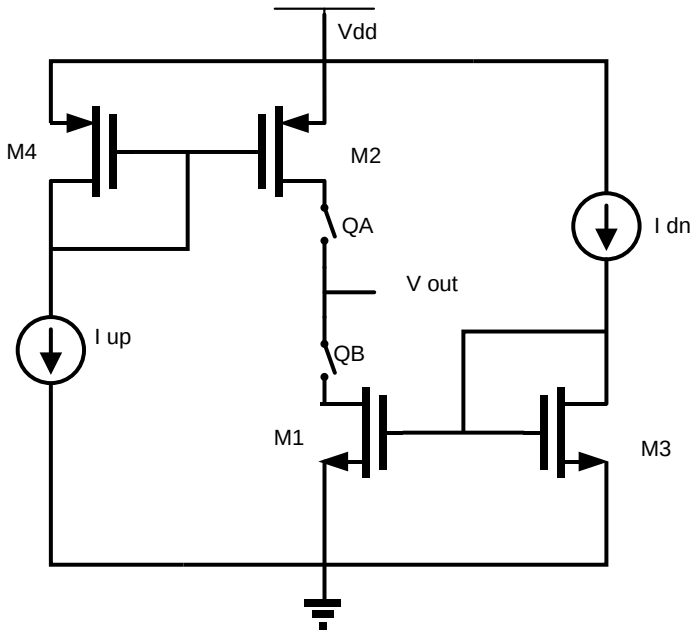


Figure 4.4.1.1 - Drain switching charge pump

Above figure is the drain switched charge pump. In which M1 and M3 MOS will acts as a current mirror and M2 and M4 are also current mirrors. Output should take across the capacitive load. When QA and QB are low the net current is zero and V out is constant. When QA is high switch is close and I up is current is pulled from the M2 MOS and V out is increased. Similarly when QB is high a current is I dn current is pulled from the capacitor and the voltage is decreased.

After the switch is turned on, the voltage at the drain of M1 increases from OV to the loop filter voltage held by PLL. In the meantime, M1 has to be in the linear region till the voltage at the drain of M1 is higher than the minimum saturation voltage. During this time, high peak current is generated even though the charge coupling is not considered. It is caused by the voltage difference of two series turn-on resistors from the current mirror, M1, and the switch. On the PMOS side, the same situation will occur and the matching of this peak current is difficult since the amount of the peak current varies with the output voltage.

4.4.2 Gate switching charge pump

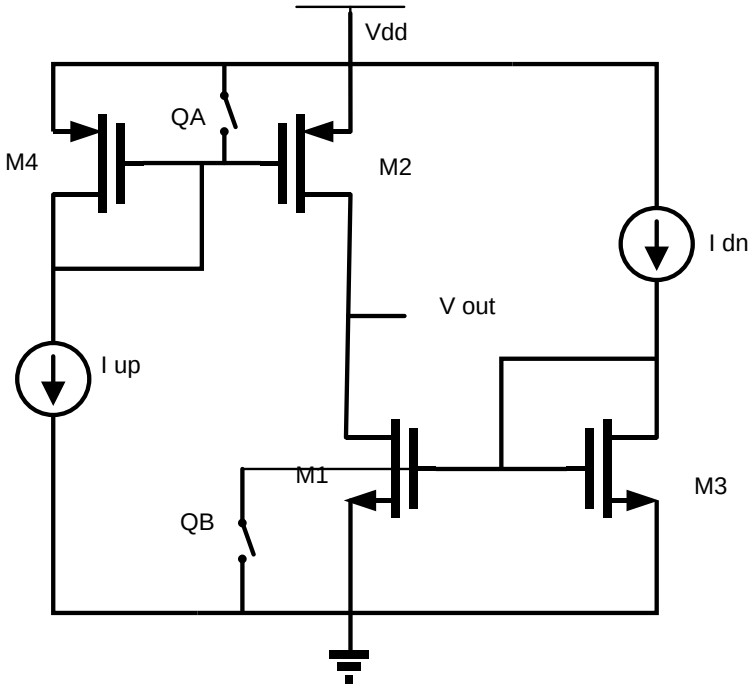


Figure 4.4.1.2 - Gate switching charge pump

Above figure is the gate switched charge pump. In which M1 and M3 MOS will acts as a current mirror and M2 and M4 are also current mirrors. Output should take across the capacitive load. When QA and QB are low the net current is zero and V out is constant. When QA is high switch is close and I up is current is pulled from the M2 MOS and V out is increased. Similarly when QB is high a current is I dn current is pulled from the capacitor and the voltage is decreased.

To achieve fast switching time, the bias current of M3 and M4 may not be scaled down since the gm3,4 affects the switching time constant in this configuration. The gate capacitance of MI and M2 is substantial when the output current of the charge pump is high and the long channel device is used for better matching. To save the constant bias current, the gated bias current can be employed cooperating with the PLL at the cost of complexity.

4.4.3 Source switching charge pump

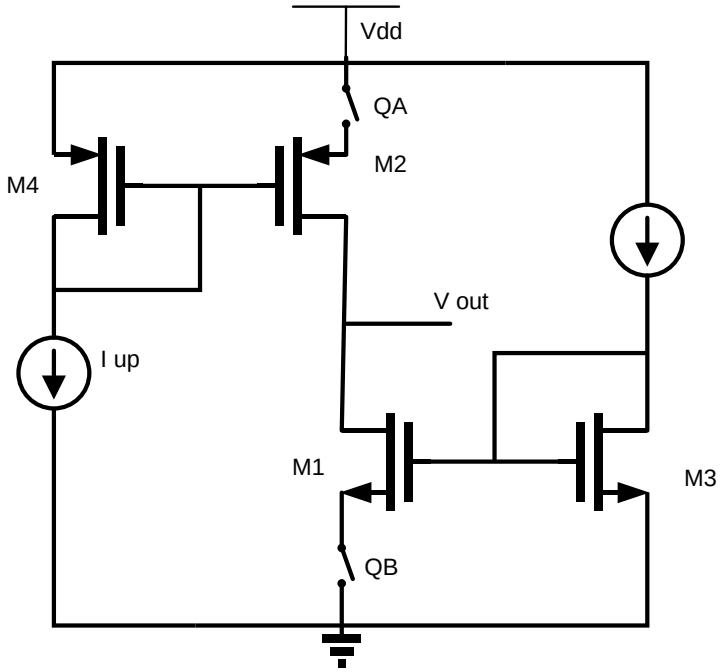


Figure 4.4.1.3 - Source switching charge pump

Above figure is the drain switched charge pump. In which M1 and M3 MOS will acts as a current mirror and M2 and M4 are also current mirrors. Output should take across the capacitive load. When QA and QB are low the net current is zero and V out is constant. When QA is high switch is close and I up is current is pulled from the M2 MOS and V out is increased. Similarly when QB is high a current is I dn current is pulled from the capacitor and the voltage is decreased.

M1 and M2 are in the saturation all the time. Different from the gate switching, the gm3,4 does not affect the switching time. As a result, the low bias current can be used with high output current. This architecture gives faster switching time than the gate switching since the switch is connected to single transistor with lower parasitic capacitance.

Chapter 5

Implementation of charge pump with to reduce Spur by matched currents

5.1 Charge pump using Cascoding current mirror:

Charge pump consists of the four inputs Up, Up_b, Dn_b and Dn which are the outputs of the PFD. Cascode current mirror is used in the charge ump because it will reduce the effect of channel length modulation. In put voltage of the mirror circuit will be equal and this will drive Iup and Idn almost equally. i.e... We can achieve matched currents of the charge pump.

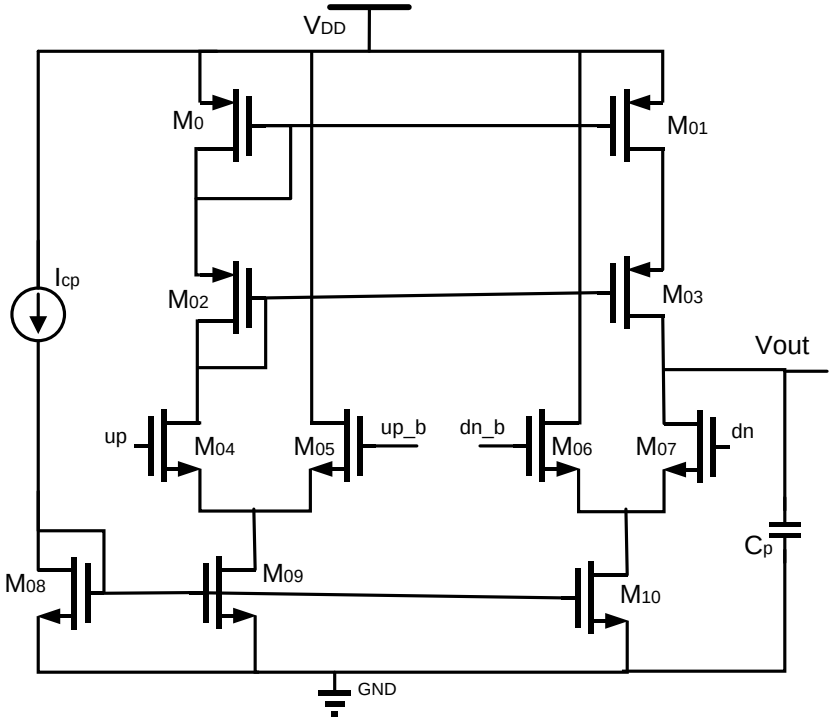


Figure 5.1.1 – Charge pump using Cascoding current mirror

If Up is +ve and Dn is –ve Icp current is steered from the Up transistor and the same current is mirrored to the capacitor due cascode current mirror. When Up is -ve and Dn is +ve Idn current is steered from the Dn transistor and the same current is mirrored from the capacitor. When Up is -ve and Dn is –ve then

transistor drive from the Dn_b and Up_b the both are connected to ground. So, the average current in the charge pump is zero and at this state we can say that the PLL is in the locked state.

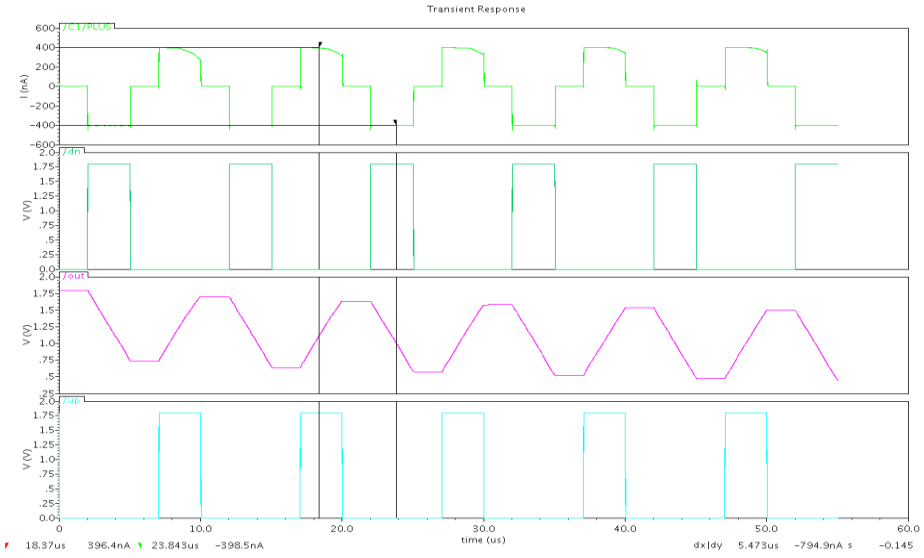


Figure 5.1.2 – Transient response of charge pump

In the above blue color waveforms are the inputs of the charge pump up and dn as shown in the figure Charge pump using Cascoding current mirror. When up and dn are low or high then voltage is constant i.e. pink color wave form represents the voltage which is input to the VCO and charge pump current is equal to zero. When dn is high and up is low then voltage is decreased and the Idn current is produced i.e current in the charge pump is represented in green color waveform. Similarly when up is high and dn is low then voltage is increased and charge pump current is increased.

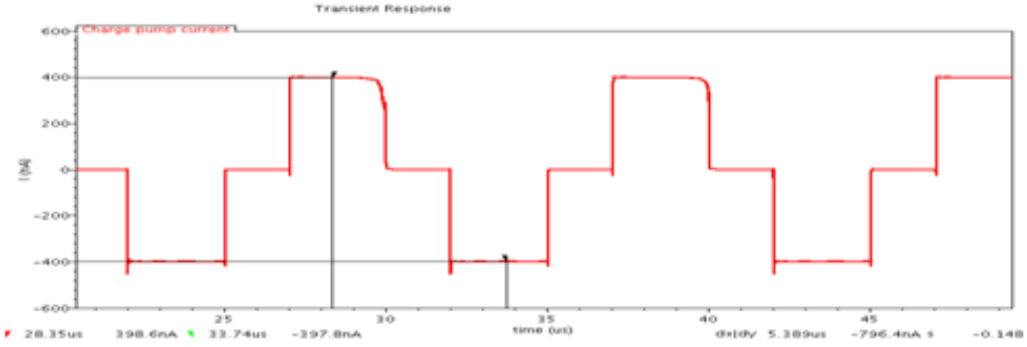


Figure 5.1.3 – Charge pump current across the capacitor

From the above figure the Iup and Idn currents are 398.6nA and -397.81nA, from those current matching of 99.01% is achieved and spur is about -80.12dBc.

5.2 Charge pump using Super Wilson current mirror:

Charge pump consists of the four input Up, Up_b, Dn_b and Dn which are the outputs of the PFD. Super wilson current mirror is used in the charge ump because it will reduce the effect of channel length modulation. In put voltage of the mirror circuit will be equal and this will drive Iup and Idn almost equally. i.e... We can achieve matched currents of the charge pump.

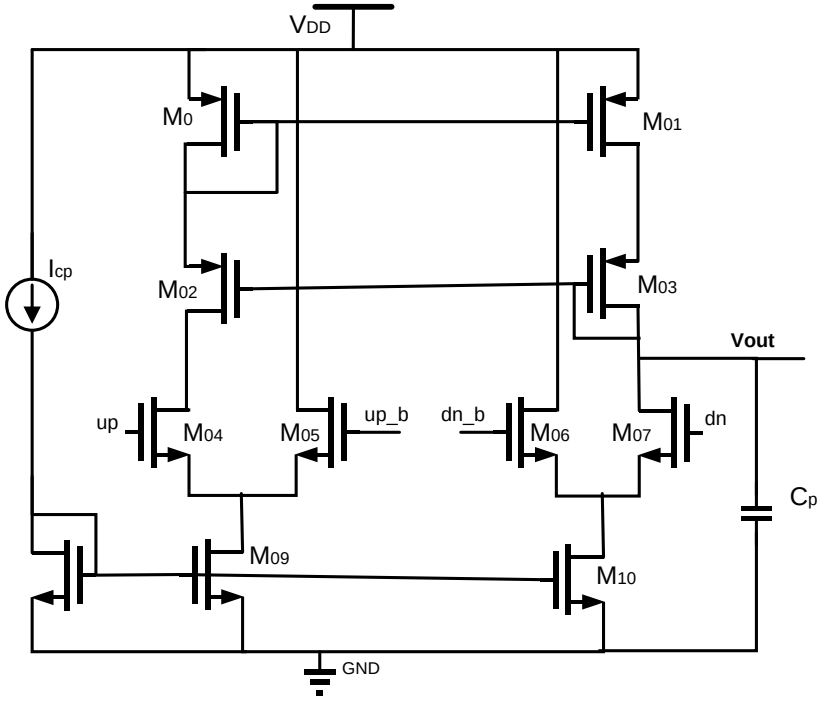


Figure 5.2.1 – Charge pump using Super wilson current mirror

If Up is +ve and Dn is –ve Icp current is steered from the Up transistor and the same current is mirrored to the capacitor due super wilson current mirror. When Up is -ve and Dn is +ve Idn current is steered from the Dn transistor and the same current is mirrored from the capacitor. When Up is -ve and Dn is –ve then transistor drive from the Dn_b and Up_b the both are connected to ground. So, the average current in the charge pump is zero and at this state we can say that the PLL is in the locked state

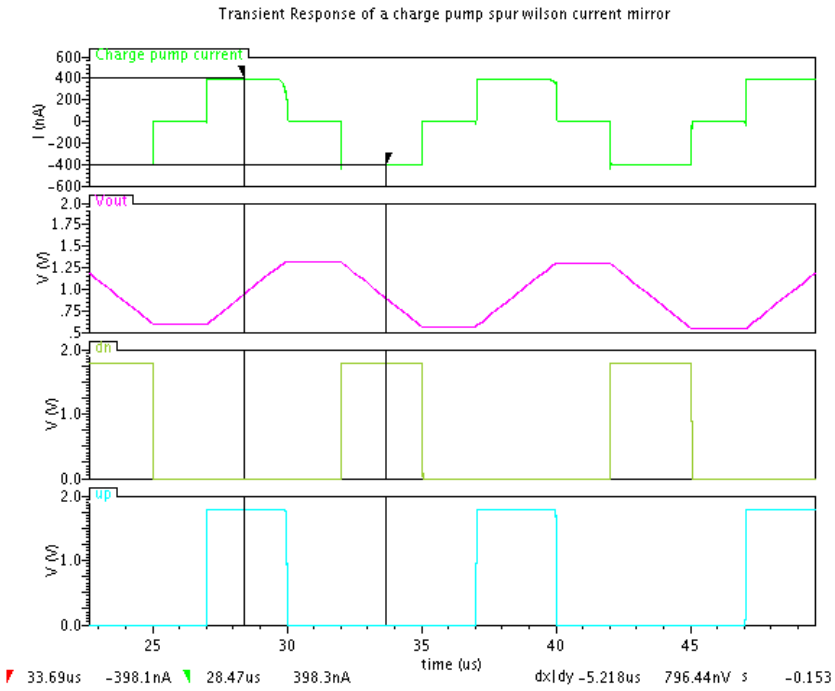


Figure 5.2.2 – Transient response of charge pump

In the above blue color waveforms are the inputs of the charge pump up and dn as shown in the figure Charge pump using super wilson current mirror. When up and dn are low or high then voltage is constant i.e. pink color wave form represents the voltage which is input to the VCO and charge pump current is equal to zero. When dn is high and up is low then voltage is decreased and the Idn current is produced i.e current in the charge pump is represented in green color waveform. Similarly when up is high and dn is low then voltage is increased and charge pump current is increased.

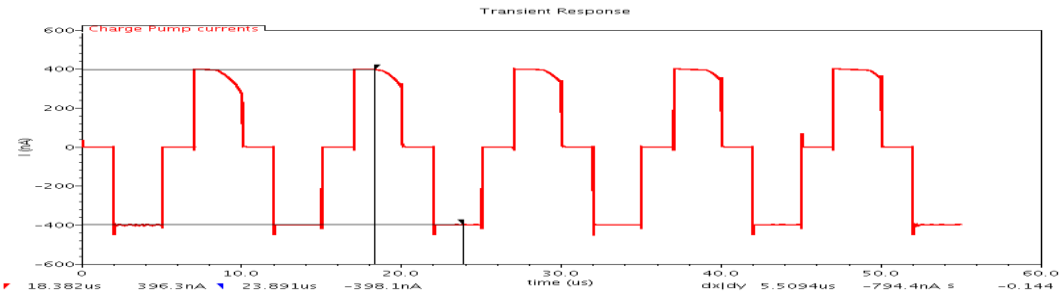


Figure 5.2.3 – Transient response across capacitor

From the above figure the Iup and Idn currents are 396.6nA and -398.1nA, from those current matching of 99.24% is achieved and spur is about -82.35dBc.

Chapter 6

Conclusion and Future Work

6.1 Conclusion

Charge pump with matched currents is designed using cascode current mirror and super Wilson current mirrors. Spur reduction in the PLL is achieved by the matching currents of the charge pump. The circuits have been designed and performance of the system is verified using 0.18µm CMOS process.

Mismatch of charge pump currents in cascode current mirror is 99.91 and which will produce the spur of about 78.2dBc.

Mismatch of charge pump currents in super wilson current mirror is 99.89 and which will produce the spur of about 75.2dBc.

6.2 Future Work

This work can be further carried out as a future scope in order to develop a complete PLL for producing the high spectral purity clock with reduced spur.

Designing the layout of charge pump circuit and fabricating the Charge pump with reduced spur.

Fabrication of the complete PLL with reduced spur.

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