

# **ANALYSIS OF ACTIVE TRANSFORMERS AND THEIR IMPACT ON VOLTAGE CONTROLLED OSCILLATORS**

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In Partial Fulfillment of the Requirements for  
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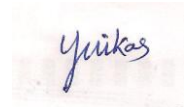
भारतीय प्रौद्योगिकी संस्थान हैदराबाद  
Indian Institute of Technology Hyderabad

Department of Electrical Engineering

June, 2012

## Declaration

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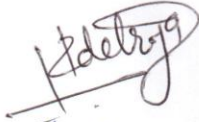
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## Approval Sheet

This thesis entitled ANALYSIS OF ACTIVE TRANSFORMERS AND THEIR IMPACT ON VOLTAGE CONTROLLED OSCILLATORS by VIKAS Y is approved for the degree of Master of Technology from IIT Hyderabad.



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## **Abstract**

The field of wireless communication has undergone a revolution in the past decade or so and RF communication blocks being integral to this revolution their advancement has not gone unnoticed either. Perhaps the only issue that still plagues RF designs apart from a dedicated technology requirement for fabrication purposes is the use of passive components in most on-chip circuit realizations. While a MOS may still mimic an actual capacitance quite successfully in a given voltage regime the same sadly cannot be said about the inductor. On-chip passive inductors continue to be the trusted guard in high performing RF front end circuits but occupy as much as 90% if not more of the circuit area. Active inductors and transformers provide us with a suitable on-chip remedy that under certain performance requirements can suitably replace the passive inductors occupying next to nothing area when compared with their passive counterparts. Active inductors and transformers being in their nascent phase many topological variations and circuit modifications affecting the same have been implemented in the past decade or so. We attempt one such modification in the work presented.

In the recent years, the demand for wireless communication has been increased dramatically. Typical RF transceivers have a built-in frequency synthesizer (oscillator) to generate a signal with the required frequency used for up and down conversion. More preferably the voltage controlled oscillators are good topologies.

Voltage controlled oscillators are the essential part in the RF receivers. Tuning range, phase noise, output power are main performance parameters for VCO. In this work, the passive transformer VCO has been simulated and transient ,phase noise analysis was discussed. In chapter 3, the new topologies of active transformers are proposed and are implemented in UMC 180nm CMOS technology and simulated using Cadence SpectreRF simulation. In chapter 4, the VCOs using the proposed active transformers are implemented in UMC 180nm CMOS technology and simulated using Cadence SpectreRF simulation.

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# Chapter 1

## Introduction

The broad range of modern wireless applications demand the wireless communication systems with more bandwidth, flexibility and configurability. More research work is going on these days on RF CMOS as it can be integrated with base-band circuits and other digital modules which are already made in CMOS, in System on Chip (SOC).we know that oscillators play a key in RF transceivers at the mixer stage. More preferably, voltage controlled oscillators are the best choice because we can tune the frequency as a function of voltage for our requirement. Also modern RF systems require a stable local oscillation signal at a particular carrier frequency ranging from hundreds of MHz to a few GHz. Designing an oscillator that fulfills the system specification of spectral purity and frequency tuning range under a stringent power consumption limit can be a challenging task especially when using CMOS process targeting a monolithic implementation of the entire RF system.

Voltage controlled oscillators are very much used as frequency synthesizer in RF transceivers to generate a signal with the required frequency used for up and down conversion. Wireless standards specify the minimum level of the received signal, the maximum level of noise, the channel bandwidth, and the spacing between adjacent channels. Therefore the maximum amount of acceptable phase noise on the oscillator can be calculated using the required signal to noise ratio after down conversion. Oscillators are usually in the form of voltage controlled oscillators and are the key component of a Phase Locked Loop (PLL) system. As a result, the amount of generated phase noise, within the bandwidth of the PLL, can be reduced by the loop characteristics. The tunability of VCOs can be achieved using tunable circuits like varactors and the tank circuits use active and passive inductors and transformers. Transformers give good quality factor, thereby we can improve phase noise performance. Active transformers are much more useful because we can increase the bandwidth by varying the coupling coefficient which is function MOS transistor parameters.



## 1.1 Motivation and Aim

The motivation for the work came from the tank circuits that are using in the voltage controlled oscillators. There are two types of tank circuits that are using in voltage controlled oscillators. one is passive inductor that are made in planar technology with spiral structure and another one is passive transformers that are made planar technology also. The spiral structures of passive inductor and transformer are shown in Figure 1.1.

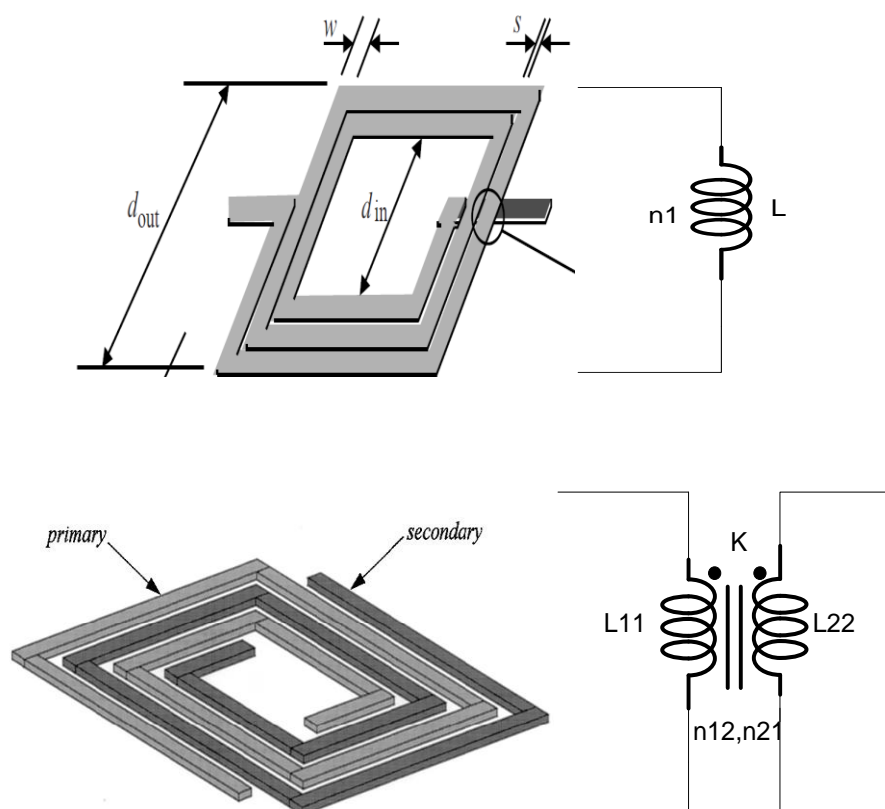


Figure 1.1 Diagrams of spiral inductor and spiral transformer

In wireless communications, the transceiver circuits require local oscillators. In that local oscillator these tank circuits are used. For some wireless systems, we require more bandwidth, for that we have to increase the inductance value. Many researches have done to embed these passive tank circuits in single chip, but it is a difficult task to embed these tank circuits because they require large area for to get the large inductance. If we to increase the inductance of inductor, either we have to increase the number of turns of inductor or use of stacked configurations. But latter increases the spiral-substrate capacitance. But passive transformers are used to increase the inductance without significantly increase the silicon consumption. For inductor, the number of turns is directly

proportional to inductance value but for transformer it is directly proportional to ratio of inductances of secondary windings and primary windings.

For inductor,  $n1 \propto \sqrt{L}$

For transformer,  $n12 \propto \sqrt{(L11/L22)}$

$n21 \propto \sqrt{(L22/L11)}$

If we take  $L = 8\text{nH}$ ,  $L11 = 8\text{nH}$ ,  $L22 = 2\text{nH}$ , then  $n1 > n12$

For the same inductance of 8nH inductor occupies more turns than the transformer. Therefore, it requires more area than the transformer because area is directly proportional to number of turns.

Transformer also increases the total inductance value of  $L_t = L11 + L22 + 2M$ , M is mutual inductance between primary and secondary.

In VCO circuits, the passive inductors and transformers are connected in various ways. Generally inductors are connected at drain of cross-coupled pair and transformers are also connected at drain and also from drain to source. The various connections of tank circuits are shown in Figure 1.2

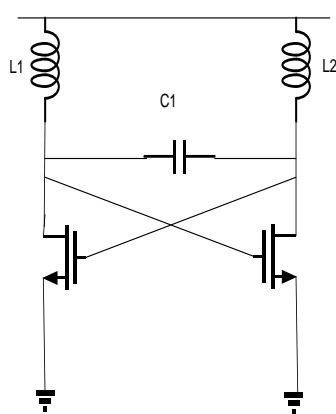


Figure 1.2(a) Inductor

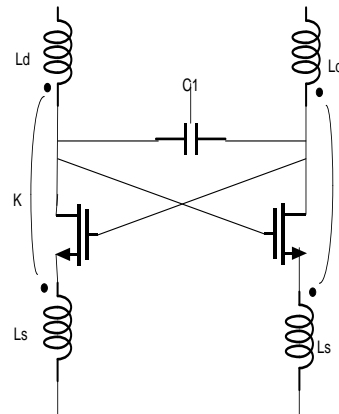


Figure 1.2(b) Transformer

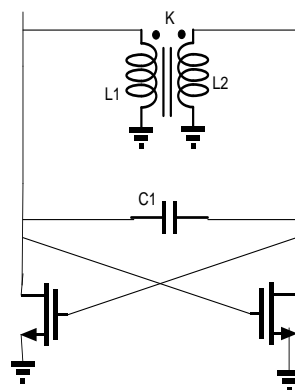


Figure 1.2(c) Transformer

From the above circuits, Figure 1.2(a) uses passive inductor at drain, Figure 1.2(b) uses transformer at drain and source. This circuit is useful in getting high quality factor and low phase noise for low voltage supply. Figure 1.2(c) uses transformer connected at ground.

These passive inductors and transformers have many disadvantages namely low inductance value, low quality factor, low self-resonant frequency, large silicon area and are not compatible with digital CMOS circuits. Alternatively, these passive inductors and transformers are implemented using active devices namely MOS transistors. These are connected in such a way they will offer inductive characteristics in certain frequency range. These active transformers offer lots advantages than the passive counterparts namely high and tunable inductance value, high quality factor, high self-resonant frequency, low silicon area and are very much compatible with digital CMOS technologies because they are constructed using MOS devices. The inductance value are varied directly by varying the width to length ratios of MOS devices.

In the voltage controlled oscillators using the passive transformers , the tuning can be done by varying the tuning voltage of varactors or by varying the coupling coefficient of the passive transformer . Once the value of inductance is fixed , it is difficult to change the inductance value at the expense of silicon consumption. Transformers are used to increase the inductance value without significantly increasing the silicon consumption. Active transformers consume negligible silicon consumption because they are implemented in CMOS technology. By this active transformers we can directly change the value of inductance through the MOS transistor dimensions. Also, this CMOS active inductors and transformers are easily realized using standard digital CMOS processes.

The aim of this work includes study and implementation of various configurations of active transformers and comparison of their performances. Implementation of VCOs using the proposed active transformers and comparison of their performances.

## 1.2 Literature Survey

So many research works have done on transformer coupled CMOS VCOs in the recent years. As we going into the low power VCO the work done by chao-chieh Li, To-Po wang gives good phase noise performance. The operation of the transformer coupled VCO and phase noise reduction is clearly explained in this paper. The effect of coupling coefficient on the frequency is also measured. Chieh-An Lin and Jing-Lin Kuo also presented a paper on the low power VCOs and they used varactors as tuning elements. They reach K-band with transformer feedback mechanism. Thaoura CHTIOUI and Dalenda BEN ISSA have done a simple circuit on the VCO, for this they got good noise performance and injection locked frequency. The design of transformer coupled CMOS VCO was explained in [2] and introduction on active transformers was explained in [3]. The design of varactors was explained in [4] through the equation. The usage of the active transformers was explained in [5] in which they have tang active transformers. The variations of the bandwidth was explained in [6] and also the effect of coupling coefficient on bandwidth was also explained. Broad-side coupled transformer was explained in [2] and also the effect of quality factor was also explained. Frequency dividing mechanism was described in [6] and also the injection locked mechanism was explained in this paper. CMOS quadrature VCO was explained in [1] and also good quality factor enhancement was achieved in this paper. The design of CMOS LC oscillators was explained in [4] and also oscillator topologies were explained.

## 1.3 Contribution of Thesis

This work focuses on analysis of active transformers and its impact on voltage controlled oscillators. The contributions of the work as follows.

- Performance calculation of passive transformer VCO.
- Implementation and simulation of Active transformer configurations.
- Implementation and simulation of Active Transformer VCO configurations.
- Comparison of performances of VCO configurations.

## 1.4 Voltage Controlled Oscillator

Voltage controlled oscillator is being used by the industry in many of wireless applications. one of such application is RF super heterodyne receiver. It is used in the receiver with the mixer. Here the voltage controlled oscillator is used as local oscillator for the mixing of signals. Another application of VCO is signal generator and also in various wireless applications. Recently, VCOs are manufacturing in the CMOS process and they gaining more attention in wireless applications.

A simple Phase Locked Loop(PLL) using the voltage controlled oscillator is depicted in the figure 1.1.It has also a phase detector and the low pass filter.The VCO represented here takes the output of low pass filter as voltage and according to that voltage it will change the frequency of the signal.

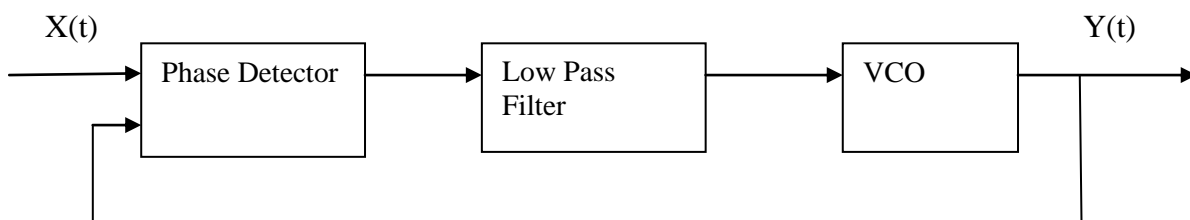


Figure 1.3 Basic Block diagram of PLL

The phase detector serves as an error amplifier in the feedback loop, thereby minimizing the phase difference between  $X(t)$  and  $Y(t)$ . The loop is considered locked if phase difference is constant with time, a result of which is that the input and output frequencies are equal. In the locked condition, all the signals in the loop have reached a steady state and the PLL operates as follows. The phase detector produces an output whose dc value is proportional to phase difference. The low-pass filter suppresses high frequency components in the phase detector output, allowing the dc value to control the VCO frequency and with a phase difference. Thus, the low pass filter generates the proper control voltage to VCO. The VCO generates the signal whose frequency is linearly proportional to the voltage applied from the low pass filter. The output again fed back to the input until the locking of phase occurs. Again the phase detector detects the error in the phase and give the signal to the low pass filter. The low pass filter suppresses the low frequencies and give the required signal to VCO.

## **1.5 Requirement of Active transformer in VCOs :**

Many standard applications require that the frequency as a function of some voltage. we can easily vary the frequency as a function of voltage. In the PLL circuits the VCO oscillators are much more useful because the voltage of the VCO decides the output phase of the signal. In the wireless remote technology, the VCO is much more useful and in the CMOS process for low power devices. Micro-Processors and Micro-controllers require low power and small area PLL circuits, the CMOS technology used by these circuits helps a lot to get the low power with good accuracy and smaller area. The wireless receivers which are used in mobiles and other remote sensing devices also require low power VCOs. The CMOS technology used for the manufacturing of these VCOs helps a lot to get low power circuits for the wireless transceivers. The VCO circuits with active transformers give a high quality factor and achievable resonant frequency. By this active transformer , we can tune the frequency easily by varying the width and length ratios of the active transformer transistors. Normally the CMOS circuits for wireless applications require low power and small occupied area circuits for VCOs, the active transformers offers a good performance for this purpose. They occupy smaller area and offer high quality factor for the low power VCO circuits.

# Chapter 2

## VCO Using Passive Transformer

### 2.1 Introduction:

Even though CMOS technology has been used in digital circuits and low-frequency analog circuits for many years, it is only within the early nineties that research has shown that CMOS is capable of being used in RF circuits . With the backend of transceivers already being implemented in CMOS, it is attractive to use CMOS in the RF front end in order to integrate the receiver on a single chip. This chapter introduces basic concepts and design considerations associated with CMOS VCOs. Most applications require that their oscillators be tunable i.e., the output frequency is a function of control voltage .An ideal voltage controlled oscillator is a oscillator whose output frequency is a linear function of control voltage. A voltage controlled capacitor is one method of making the LC oscillators to vary its frequency in response to its control voltage.

### 2.2 Target structure :

. A oscillator using the passive transformer circuit uses the cross-coupled connection acts as a voltage controlled oscillator with varactor as the tuning element. The diagram is shown in the figure 1.2.

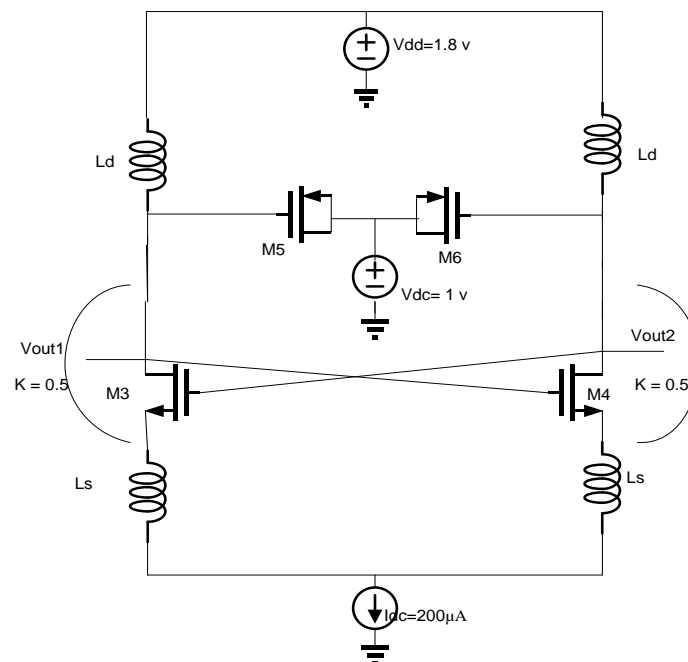


Figure 2.1 Passive Transformer VCO

The schematic of the transformer feedback low power CMOS VCO is shown in the figure 2.1. It consists of two passive transformers coupled with some coupling coefficient and the structure of cross-coupled NMOS offers the negative resistance which is useful for positive feedback to get the sustained oscillations. The tank circuit which consists of transformer offers high quality factor than that of the single inductor and also occupy the smaller area than that of inductor. The tuning of the oscillator can be done using the two PMOS varactors which are connected as shown in the figure. To improve the VCO performance in term of low supply voltage, low power and low phase noise, a transformer feedback VCO is proposed to provide extra voltage swing. The edge coupled transformer to enhance the voltage swing of the tank to achieve low phase noise and low power consumption performance.

The primary coil with self-inductance  $L_d$  of the transformer is connected to the drain terminal of the transistor, and the transistor source terminal is connected to the secondary coil with self-inductance  $L_s$  such that the drain voltage could swing above the supply voltage and the source voltage could swing below the ground potential. Because the transformer is used to force the drain and source signal to oscillate in phase, the supply voltage can be reduced for the same phase noise with lower power consumption.



### 2.3 Simulations and Results :

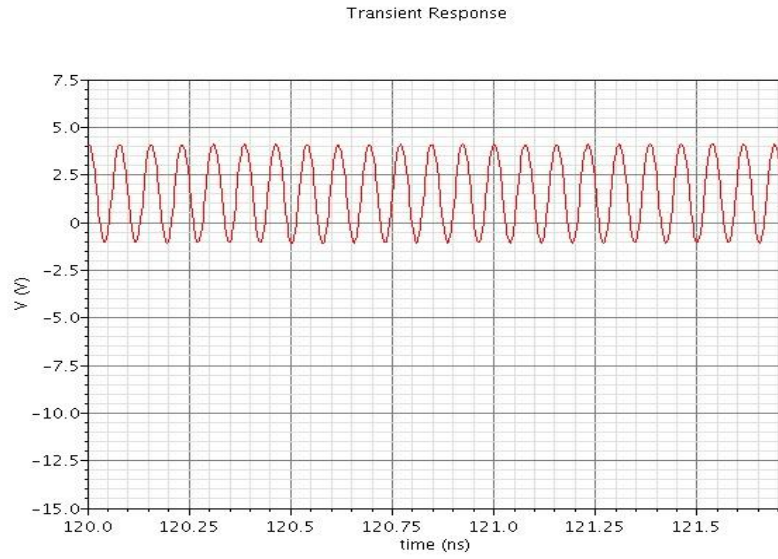


Figure 2.2 Plot of Transient Response of Passive Transformer VCO

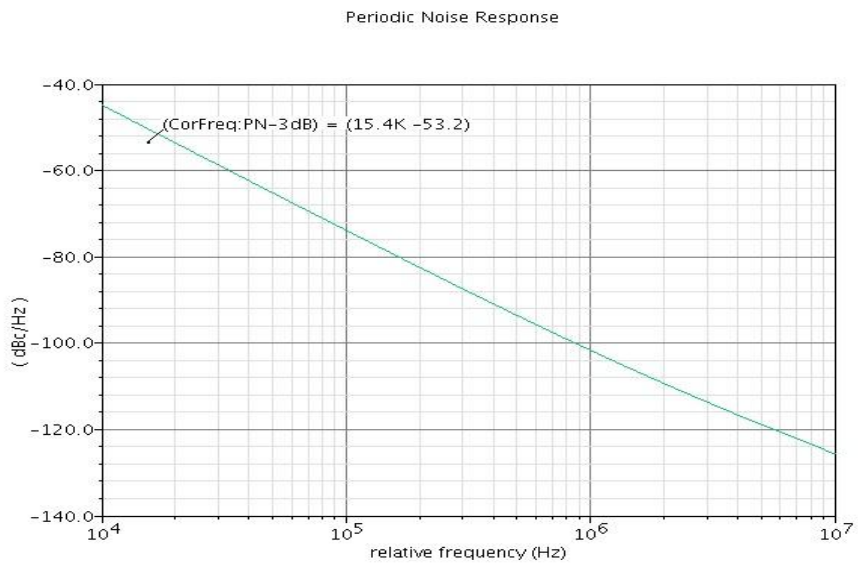


Figure 2.3 Plot of Phase Noise of Passive Transformer VCO

The phase noise at 1MHz offset is -125 dBc/Hz for the carrier frequency of 4.47 GHz.

**Tables:**

Table 3.1 components values of CMOS VCO

|             |             |                |                 |
|-------------|-------------|----------------|-----------------|
| $L_s$<br>nH | $L_s$<br>nH | $C_{gs}$<br>pF | $R$<br>$\Omega$ |
| 4           | 2           | 1              | 1K              |

Table 3.2 performance of Broad-side transformer coupled CMOS VCO

| Center Frequency<br>(GHz) | Phase Noise @ 1MHz<br>(dBc/Hz) | Core power<br>(mW) |
|---------------------------|--------------------------------|--------------------|
| 4.47                      | -103                           | 9.6                |

**Conclusion :**

By this transformer feedback low power VCO we can achieve high quality factor, high voltage swing above the supply voltage. The occupied area by the VCO also reduces due to the transformer feedback. This configuration also offers low phase noise but narrows the tuning range. The output power is between -8 to -13 dBm while the control voltage is from 0 to 1.2 V. The phase noise at 1M Hz offset is -125 dBc/Hz. The power consumption achieved is 3 mW with current of 5 mA. In this topology, a VCO for 24GHz applications implemented in a 0.18  $\mu\text{m}$  CMOS VCO also useful for the low power applications.

# Chapter 3

## Active Transformer configurations

### 3.1 Introduction :

Active transformers are designed using the semiconductor devices with NMOS and PMOS. They are mainly designed to give high quality factor, high self resonant frequency and occupy small resonant frequency. The types of active transformers used are Gyrator-C transformers, tang active transformers and tang class AB active transformers. For active transformers one circuit is used for primary windings and another circuit for secondary windings, third circuit for coupling of primary and secondary windings. The characteristics of active transformers are stability, frequency range, tunability of self and mutual inductances, turns ratio, coupling factors, voltage transfer characteristics, current transfer characteristics, linearity, noise, supply sensitivity etc. By using these active transformers we can fix the tuning range by change the values of transconductances and capacitances. The tuning of the circuit can be done using tuning voltage applied at the gate terminal of the MOS transistors of primary and secondary windings of the active transformers. The active transformers gives smaller occupied area rather than the passive transformers. Active transformers good frequency stability in case of tuning of the oscillators and also to select the resonant frequency. The also give noise performance by suppressing the supply noise and phase noise.

### 3.2 Theory and Equations :

The active transformer can be made by using two active inductors coupled through the transconductors. If we take the admittance through one end of the active inductor, then it comes as the inductive impedance. Active inductor is formed by the connection of two transconductors, one has positive transconductance and another has negative transconductance connected back to back. It also consists of a capacitor connected at one end of back to back connection.

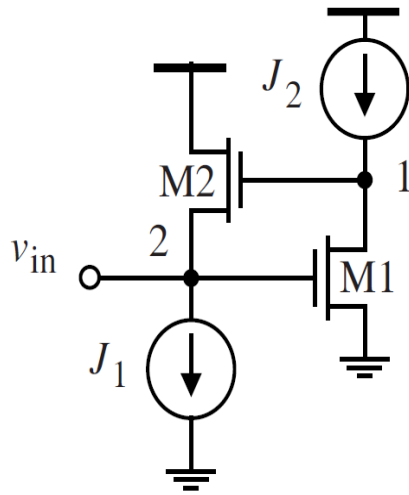


Figure 3.1 Active Inductor

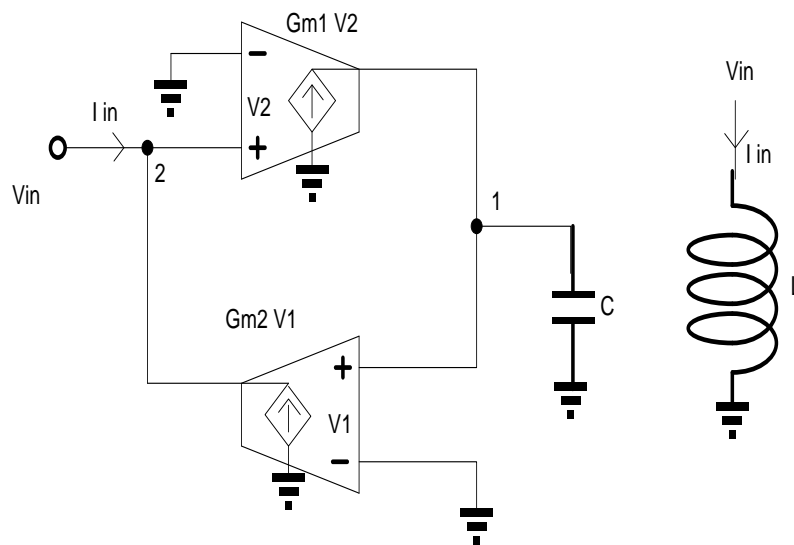


Figure 3.2 Small signal model of active inductor

The figures 3.2 and 3.3 show the schematic of gyrator-C active inductor and the small signal of that inductor. The active transformer is formed by connecting this inductor to another inductor of same type through the coupling transconductor. Coupling of primary windings and secondary windings can be done through the transconductors in which the transconductance is less than the one used in active inductor part. The admittance looking into the terminal 2 in figure 3.3 is

$$Y = I_{in} / V_2 = 1 / (S(C / G_{m1} G_{m2}))$$

This equation shows that gyrator-C circuit acts as the active inductor with inductance value

$$L = C / (G_{m1}G_{m2})$$

The equations relative to the active transformer includes the voltage-current equation, coupling coefficient equation, inductances values.

Voltage-current equations are

$$V_1 = S L_{11} I_1 + S M_{12} I_2$$

$$V_2 = S M_{21} I_1 + S L_{22} I_2$$

Coupling Coefficient equations are

$$K_{21} = M_{21} / \sqrt{(L_{11} L_{22})}$$

$$K_{12} = M_{12} / \sqrt{(L_{11} L_{22})}$$

Inductance values are

$$L_{11} = C_1 / (G_{m1}^2 \Delta) \quad M_{12} = (G_{12} / G_{m1}) * C_2 / (G_{m2}^2 \Delta) \quad \text{where } \Delta = (1 - (G_{12} G_{21}) / (G_{m1} G_{m2}))$$

$$L_{22} = C_2 / (G_{m2}^2 \Delta) \quad M_{21} = (G_{21} / G_{m2}) * C_1 / (G_{m1}^2 \Delta) .$$

### 3.3 Active Transformer configurations :

#### Existing Active transformer configurations:

1. nMOS parallel circuit.
2. pMOS parallel circuit.
3. nMOS series circuit.
4. pMOS series circuit.
5. Bidirectional nMOS circuit.
6. Bidirectional pMOS circuit.

### 3.3.1 Active Transformer configuration :

#### 1.nMOS parallel circuit

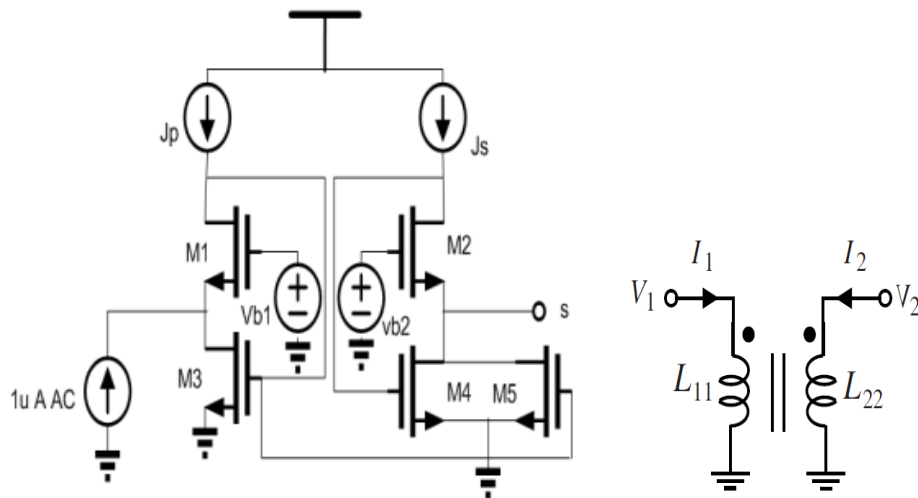
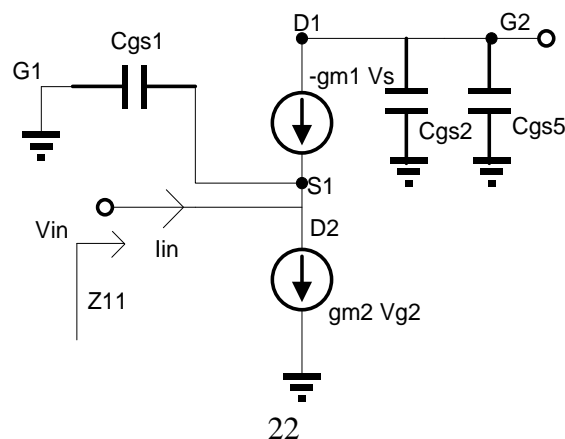


Figure 3.3 schematic of nMOS parallel active transformer circuit.

The active transformer shown in above figure is nMOS transistor parallel connection active transformer circuit. The primary side consists of one active inductor which is made up of two transconductors connected back to back. The secondary side consists of another active inductor which is made up of two transconductors. The coupling is done by one transconductor which is connected from primary inductor to the secondary. The connection done is parallel connection.  $J_p$  and  $J_s$  are current sources which are used to bias the primary and secondary.  $V_{b1}$  and  $V_{b2}$  are the voltage sources to tune inductances of primary and secondary. This nMOS parallel connection is ground connection. pMOS active transformer connection is supply connection.

#### Analysis:

The impedances  $Z_{11}$ ,  $Z_{22}$ ,  $Z_{21}$  can be calculated using the small signal of the active transformer shown above. The schematic shown in the figure 3.4 depicts the small signal model of nMOS parallel active transformer and is used to calculate the impedances and inductances.



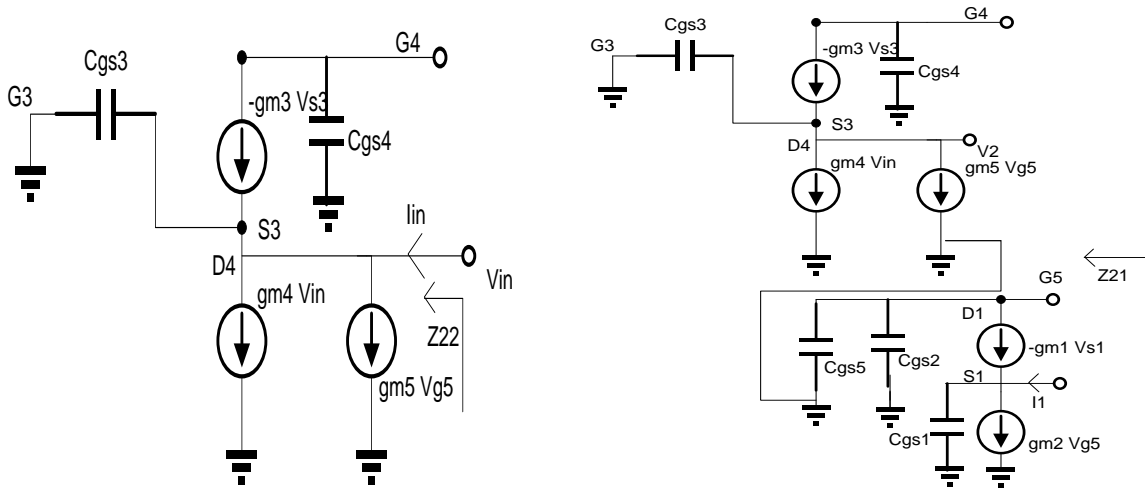


Figure 3.4 small signal model diagrams of nMOS active transformer

The first diagram shows the circuit for the calculation of the impedance  $Z_{11}$ . By applying KCL at the nodes S1 and G2 and the expression for  $Z_{11}$  can be written as

$$Z_{11} = \frac{SC_g}{S^2 C_{gs1} C_g + S g_{m1} C_g + g_{m1} g_{m2}}$$

where  $C_g = (C_{gs2} + C_{gs5})$

$g_{m1}$ ,  $g_{m2}$  are transconductances of M1 and M2

$C_{gs1}$ ,  $C_{gs2}$ ,  $C_{gs5}$  are gate to source capacitances.

From the second figure above, by applying KCL at D4, we can get equation for  $Z_{22}$

$$Z_{22} = (SC_{gs4}) / (S^2 C_{gs3} C_{gs4} + SC_{gs4} g_{m3} + g_{m4} g_{m3})$$

where  $C_{gs4}$ ,  $C_{gs3}$  are the gate to source capacitances and  $g_{m3}$ ,  $g_{m4}$  are the transconductances of M3 and M4.

From the third figure above, by applying KCL at D4, S1 we can express the equation for  $Z_{21}$  as

$$Z_{21} = \frac{g_{m5} g_{m1} S C_{gs4}}{(S^2 C_{gs1} C_g + S C_g g_{m1} + g_{m1} g_{m2})(S^2 C_{gs4} C_{gs3} + S C_{gs4} g_{m3} + g_{m4} g_{m3})}$$

## Simulation and Results:

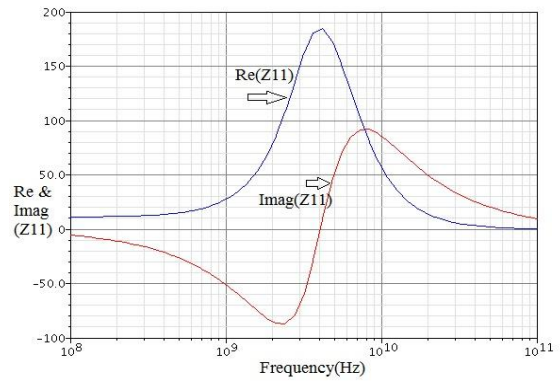
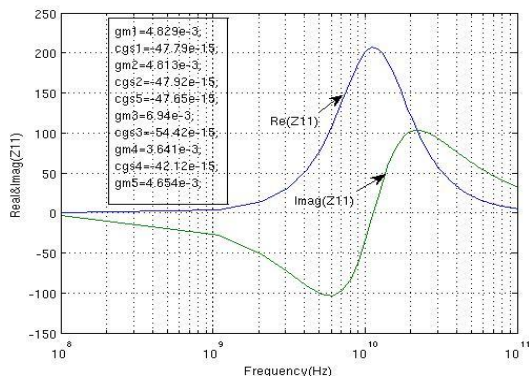


Figure 3.5 Plot of Z11 using Matlab and Cadence simulations

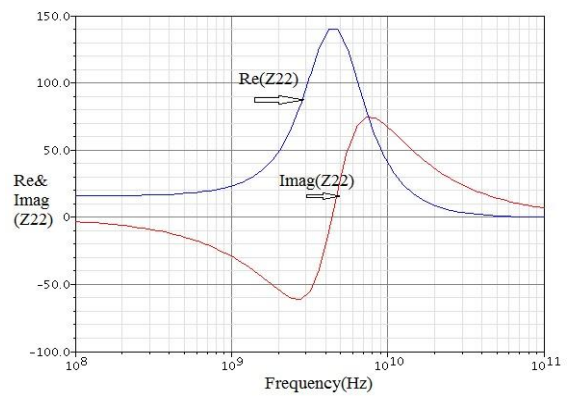
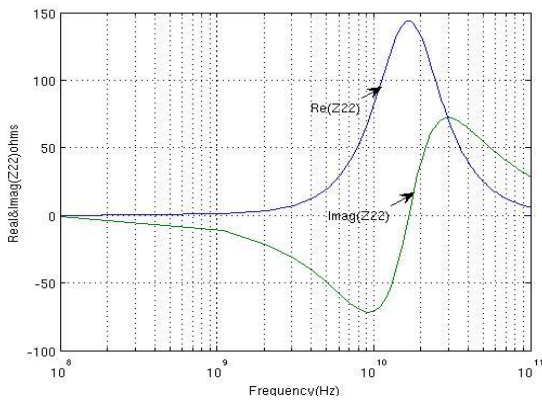


Figure 3.6 Plot of Z22 using Matlab and Cadence simulations

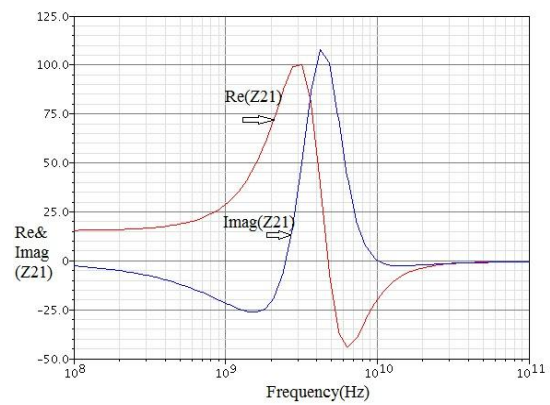
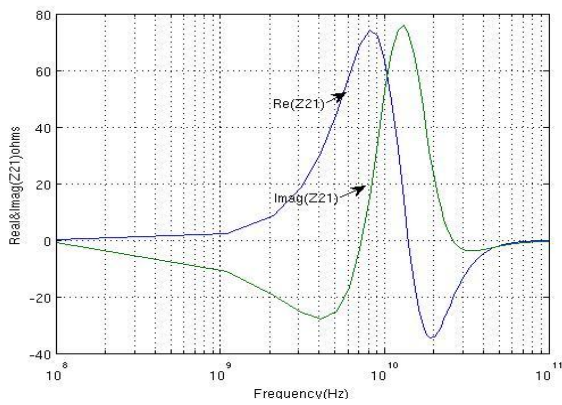


Figure 3.7 Plot of Z21 using Matlab and Cadence simulations



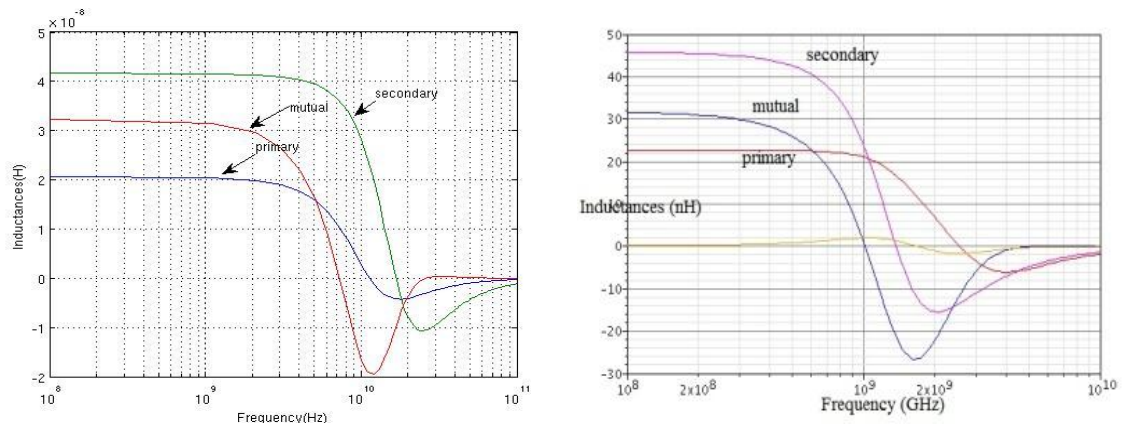


Figure 3.8 Plot of inductances using Matlab and Cadence simulations

**Tables:**

| Inductances | Matlab Simulation values(nH)<br>at 200MHz | Cadence Simulation values(nH)<br>at 200MHz |
|-------------|---|--|
| Primary     | 20  | 22   |
| Secondary   | 42  | 46   |
| Mutual      | 31  | 32   |

For nMOS parallel circuit, the values used in Matlab are

| $g_{m1}$<br>(mS) | $g_{m2}$<br>(mS) | $g_{m3}$<br>(mS) | $g_{m4}$<br>(mS) | $g_{m5}$<br>(mS) | $C_{gs1}$<br>(fF) | $C_{gs2}$<br>(fF) | $C_{gs3}$<br>(fF) | $C_{gs4}$<br>(fF) | $C_{gs5}$<br>(fF) |
|------------------|------------------|------------------|------------------|------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| 4.829            | 4.813            | 6.94             | 3.641            | 4.654            | -47.79            | -47.92            | -54.42            | -42.12            | -47.65            |

**Conclusion:**

By observing both the plots from Matlab and Cadence simulation, the inductance values in MATLAB is low because much of the parasitic effects are ignored, but in Cadence they are considered. For the impedance plots, Matlab values are almost equals the cadence.

## 2. pMOS parallel circuit:

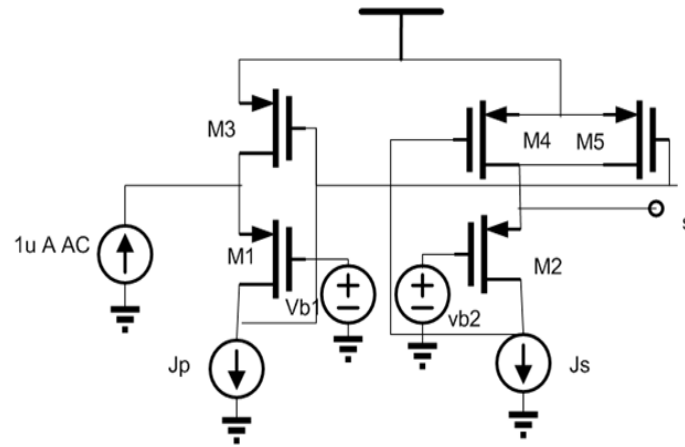


Figure 3.9 structure of pMOS parallel circuit.

## Cadence Simulation:

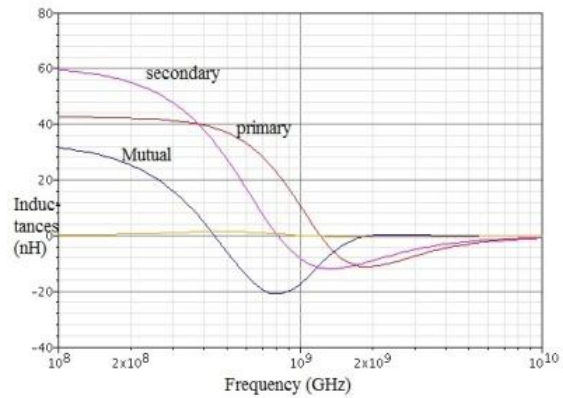


Figure 3.10 Plot of inductances

### 3. nMOS series circuit:

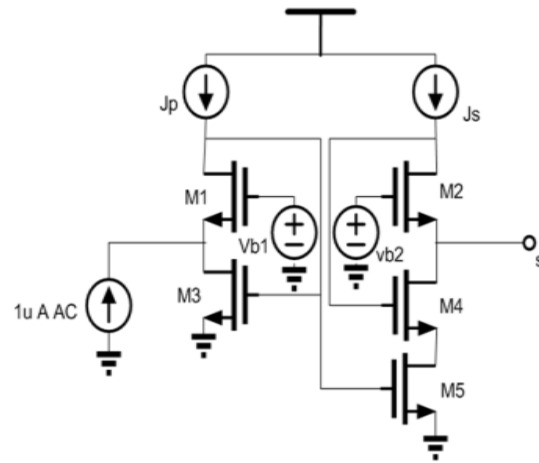


Figure 3.11 structure of nMOS series circuit

### Cadence simulation:

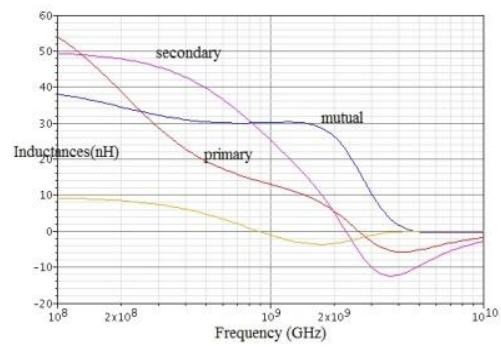


Figure 3.12 Plot of inductances

#### 4. pMOS series circuit:

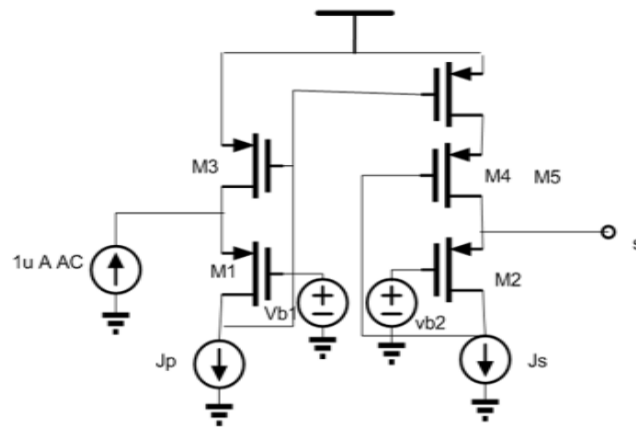


Figure 3.13 structure of pMOS series circuit

#### Cadence simulation:

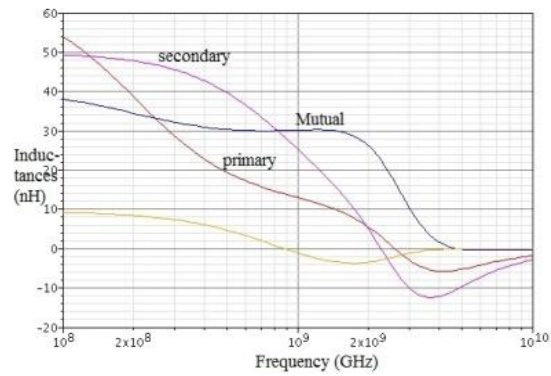


Figure 3.14 Plot of inductances

### 5. Bidirectional nMOS circuit:

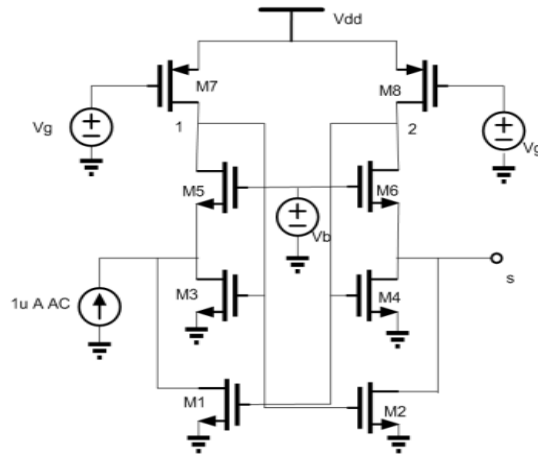


Figure 3.15 structure of Bidirectional nMOS circuit

### Cadence simulation:

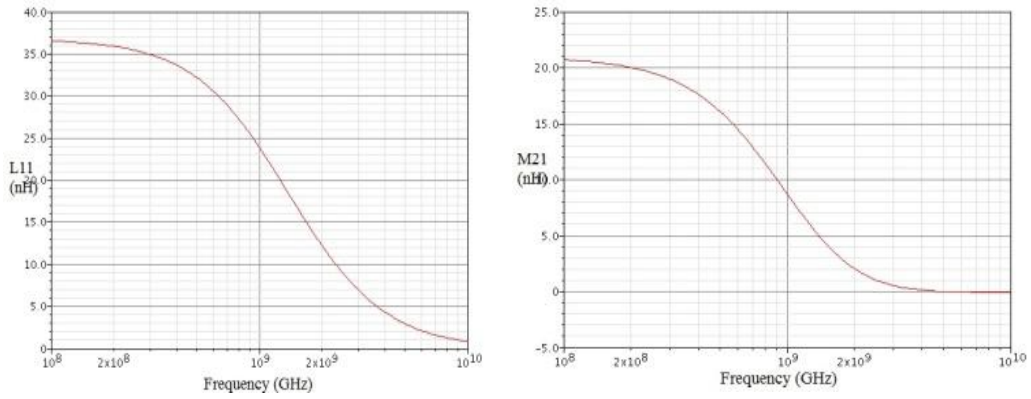


Figure 3.14 Plot of inductances

## 6. Bidirectional pMOS circuit:

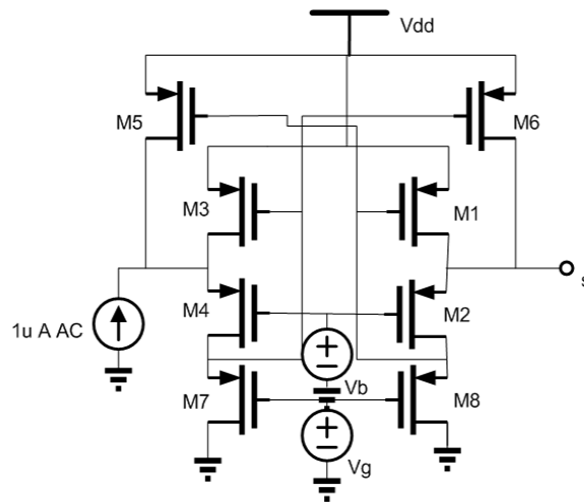


Figure 3.16 structure of Bidirectional pMOS circuit

### Cadence simulation:

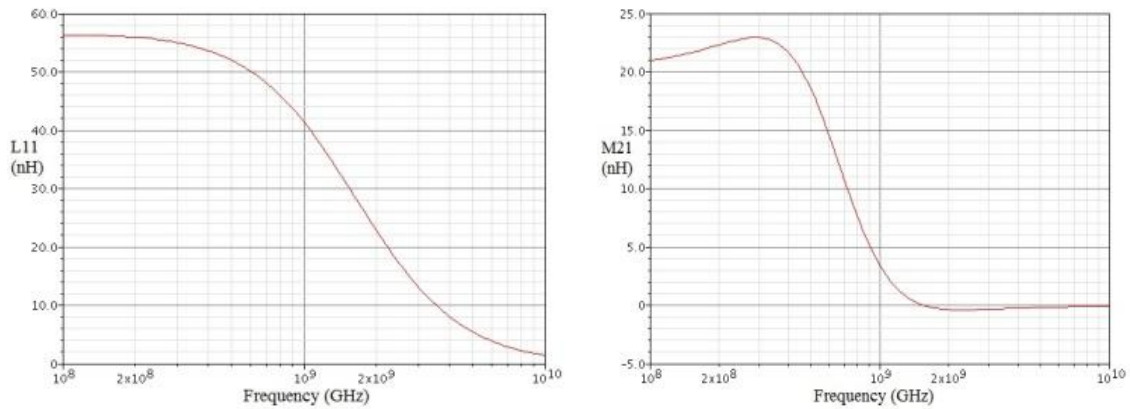


Figure 3.17 Plot of Inductances

### Conclusion:

By observing all the existing structures above and their Cadence simulation, for the unidirectional coupling secondary inductance is more than the primary because of coupling and mutual inductance is low than the self-inductance.

### 3.3.2 Proposed Active transformers :

#### Need:

The need for proposed configuration comes from the voltage controlled oscillator in which uses low supply with more phase noise performance. The signal output voltage will swing above the supply through this proposed configuration in which primary is connected to drain of the cross-coupled connection of the VCO and secondary is connected to source of cross-coupled connection of the VCO. The diagram is shown in figure 3.23 and the proposed active transformer is shown in Figure 3.24

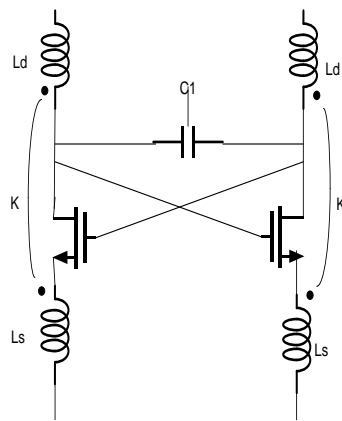


Figure 3.18 VCO configuration

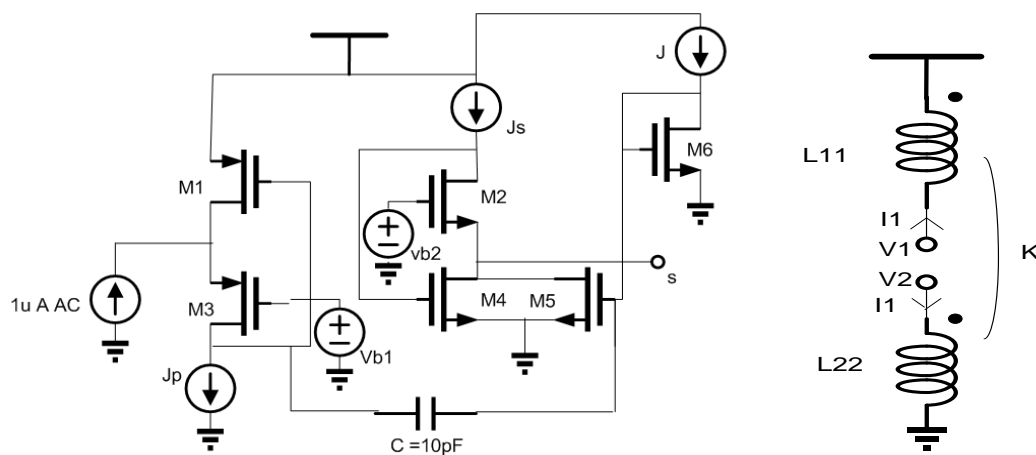


Figure 3.19 schematic of proposed active transformer circuit( pMOS-nMOS parallel circuit)

## Proposed active transformer configuration:

### 1.pMOS-nMOS parallel circuit :

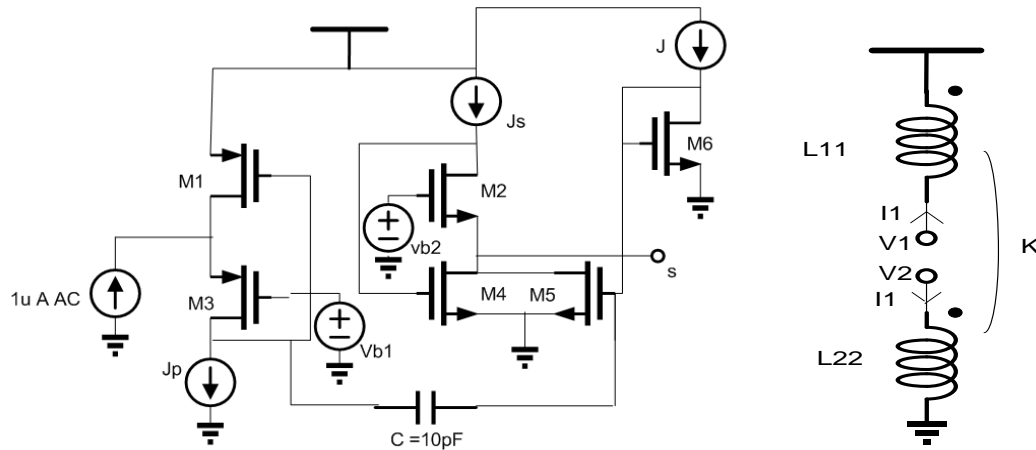


Figure 3.20 structure of pMOS-nMOS circuit

The active transformer shown in above figure is pMOS-nMOS transistor parallel connection active transformer circuit. The primary side consists of one active inductor which is made up of two transconductors(pMOS) connected back to back. The secondary side consists of another active inductor which is made up of two transconductors(nMOS). The coupling is done by one transconductor which is connected from primary inductor to the secondary. The connection done is parallel connection. One capacitor C is used to block the dc currents from primary to secondary because for the coupling transconductor biasing is giving separately. M6 forms a current mirror which biases M5 with the same voltage . J<sub>p</sub> and J<sub>s</sub> are current sources which are used to bias the primary and secondary. V<sub>b1</sub> and V<sub>b2</sub> are the voltage sources to tune inductances of primary and secondary. This pMOS-nMOS parallel connection is connected in voltage controlled oscillators in which primary is connected to supply and secondary is connected to ground .



## Analysis:

The impedances  $Z_{11}$ ,  $Z_{22}$ ,  $Z_{21}$  can be calculated using the small signal of the active transformer shown above. The schematic shown in the figure 3.20 depicts the small signal model of pMOS-nMOS parallel active transformer and is used to calculate the impedances and inductances.

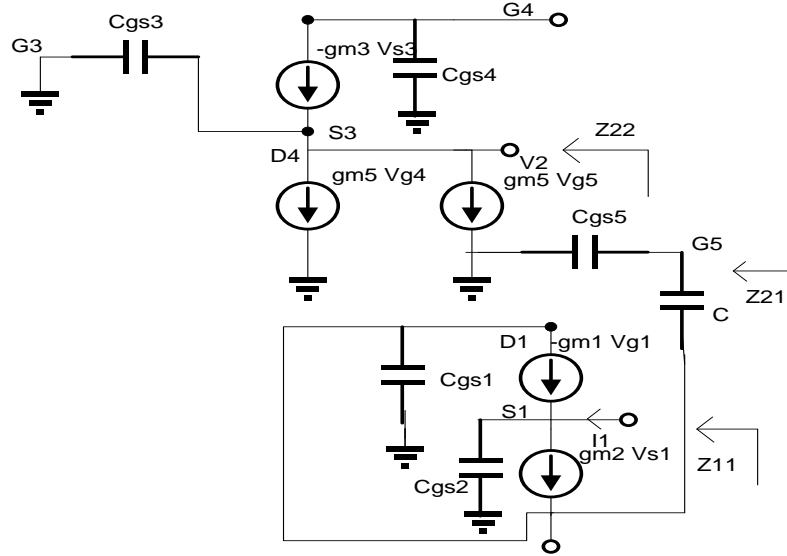


Figure 3.21 small signal model of proposed pMOS-nMOS active transformer

The first diagram shows the circuit for the calculation of the impedance  $Z_{11}$ . By applying KCL at the nodes S1 and G2 and the expression for  $Z_{11}$  can be written as

$$Z_{11} = \frac{S(C_{gs1} + (C_g \parallel C_{gs5}))}{S^2 C_{gs2} (C_{gs1} + (C_g \parallel C_{gs5})) + S g_{m2} (C_{gs1} + (C_g \parallel C_{gs5})) + g_{m1} g_{m2}}$$

From the above figure, by applying KCL at the nodes D4 and G4, the  $Z_{22}$  can be expressed as

$$Z_{22} = \frac{S C_{gs4}}{S^2 C_{gs3} C_{gs4} + S C_{gs4} g_{m3} + g_{m4} g_{m3}}$$

From the figure, by applying KCL at the nodes S1, S3, G2, the  $Z_{21}$  can be expressed as

$$Z_{21} = \frac{-S g_{m2} g_{m5} C C_{gs4}}{(C_{gs5} + C)(S^2 C_{g1} C_{gs2} + S C_{g1} g_{m2} + g_{m1} g_{m2})(S^2 C_{gs3} C_{gs4} + S g_{m3} C_{gs4} + g_{m3} g_{m4})}$$

## Simulation and Results:

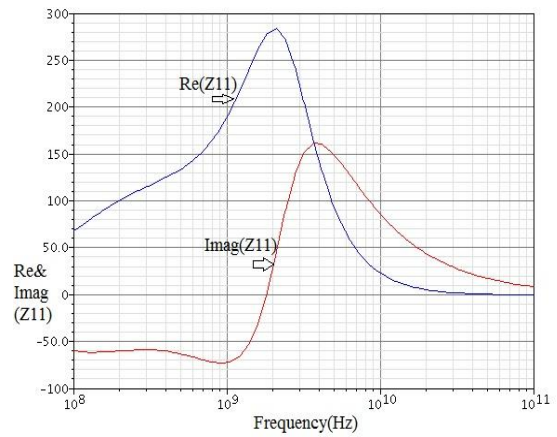
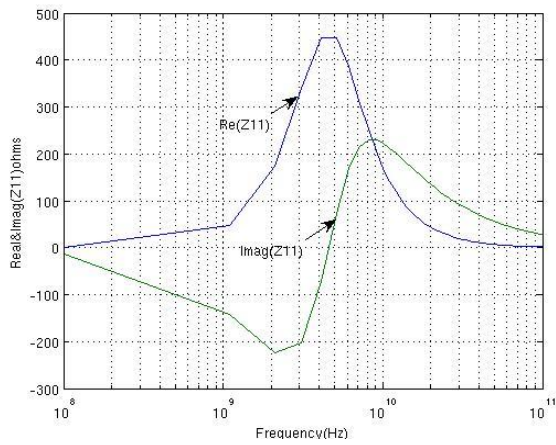


Figure 3.22 Plot of  $Z_{11}$  using Matlab and Cadence simulation

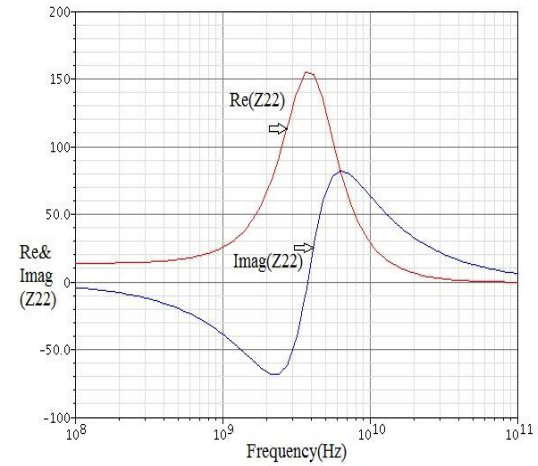
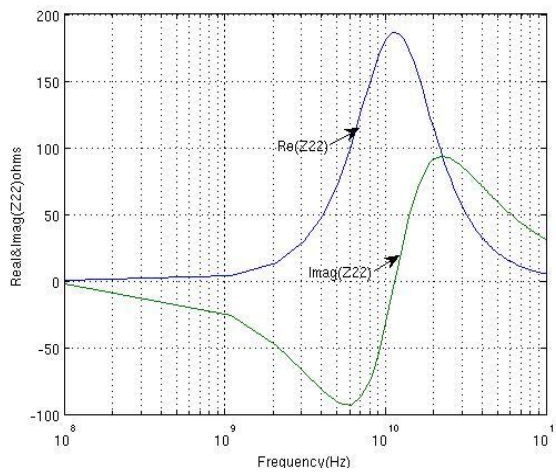


Figure 3.23 Plot of  $Z_{22}$  using Matlab and Cadence Simulation

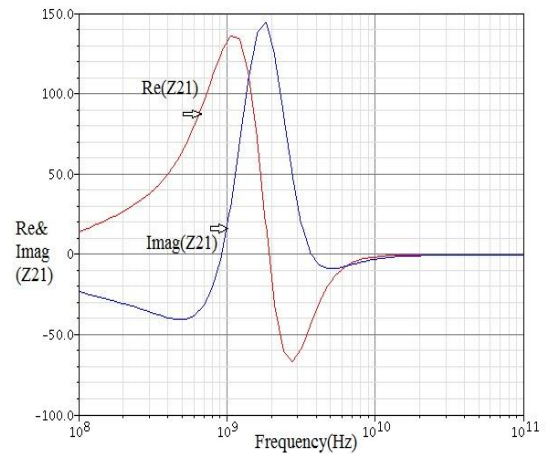
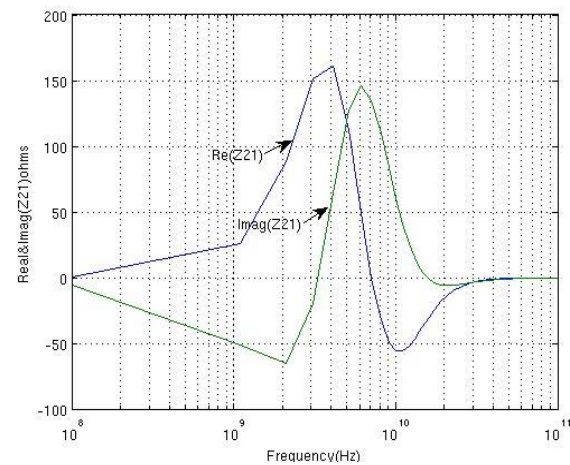


Figure 3.24 Plot of  $Z_{21}$  using Matlab and Cadence simulation

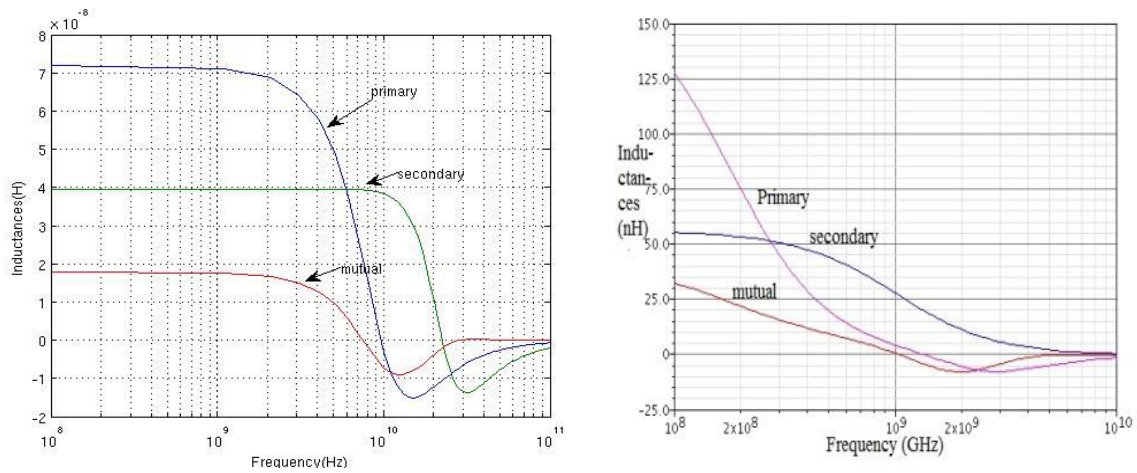


Figure 3.25 Plots of Inductances using Matlab and Cadence simulation

**Tables:**

| Inductances | Matlab Simulation values(nH)<br>at 200MHz | Cadence Simulation values(nH)<br>at 200MHz |
|-------------|---|--|
| Primary     | 72  | 75   |
| Secondary   | 40  | 50   |
| Mutual      | 20  | 25   |

| $g_{m1}$<br>(mS) | $g_{m2}$<br>(mS) | $g_{m3}$<br>(mS) | $g_{m4}$<br>(mS) | $g_{m5}$<br>(mS) | $C_{gs1}$<br>(fF) | $C_{gs2}$<br>(fF) | $C_{gs3}$<br>(fF) | $C_{gs4}$<br>(fF) | $C_{gs5}$<br>(fF) |
|------------------|------------------|------------------|------------------|------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| 2.243            | 2.173            | 5.353            | 1.224            | 4.662            | -54.39            | -56.53            | -50.55            | -25.01            | -47.85            |

**Conclusion:**

When observing above two plots, there are some significant differences between Matlab and Cadence plot. The differences are due to of unaccounted parasitic values in Matlab simulation. But in Cadence simulation, all the parasitic values are considered. For the impedance plots, both the Matlab and cadence plots are almost same.

## 2. nMOS-pMOS Parallel circuit

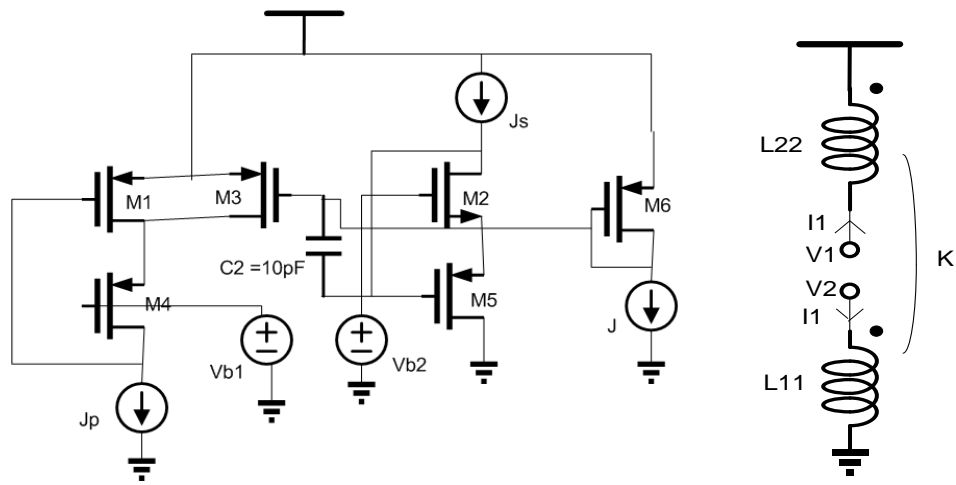


Figure 3.26 schematic of proposed active transformer (nMOS-pMOS)

## Cadence simulation:

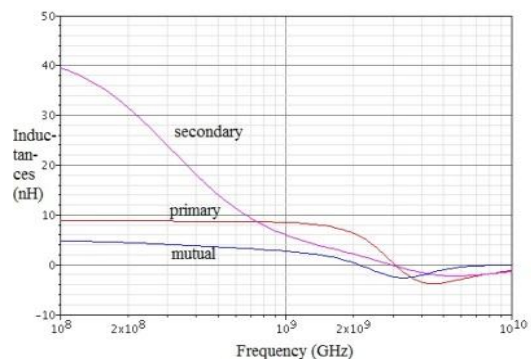


Figure 3.27 Plots of inductances

### 3. pMOS-nMOS series circuit:

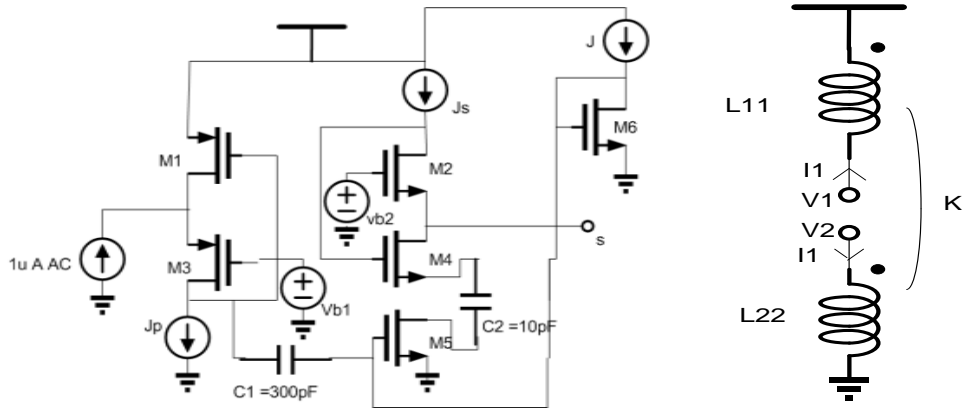


Figure 3.28 structure of pMOS-nMOS series circuit

### Cadence simulation:

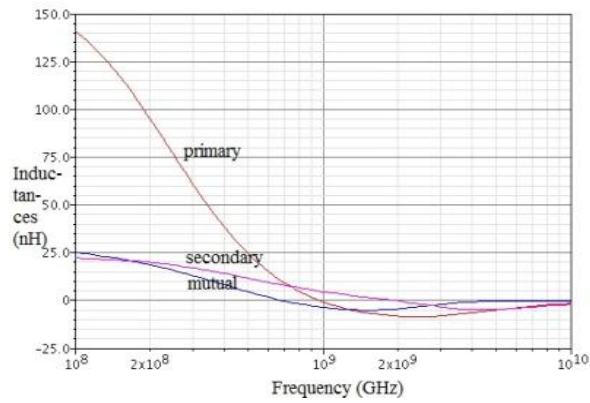


Figure 3.29 Plot of inductances

**4. nMOS-pMOS series circuit:**

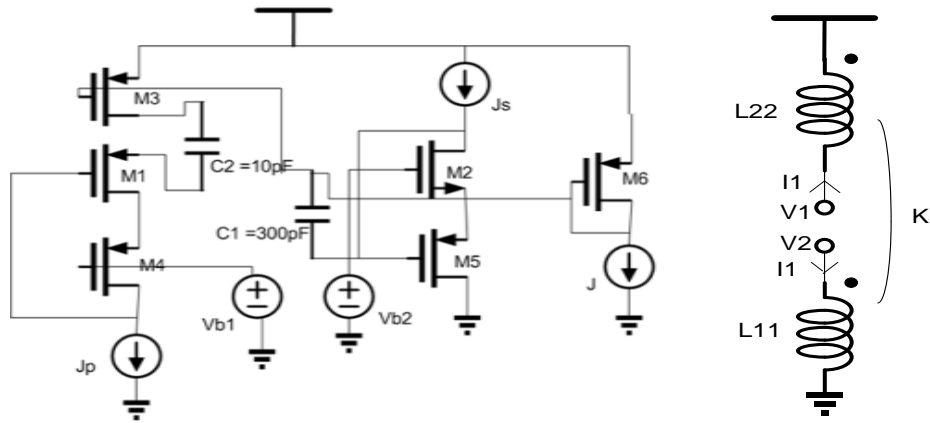


Figure 3.30 structure of nMOS-pMOS series circuit

**Cadence simulation:**

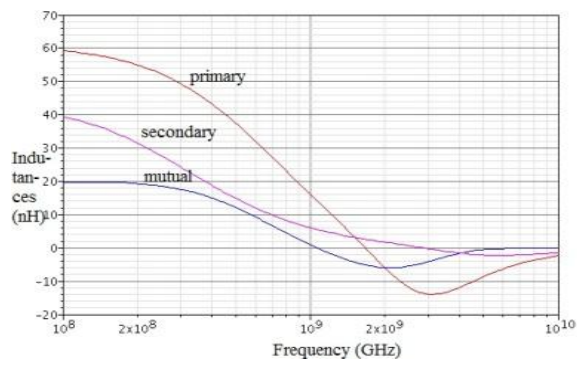


Figure 3.31 Plot of inductances

**5. Bidirectional pMOS-nMOS circuit:**

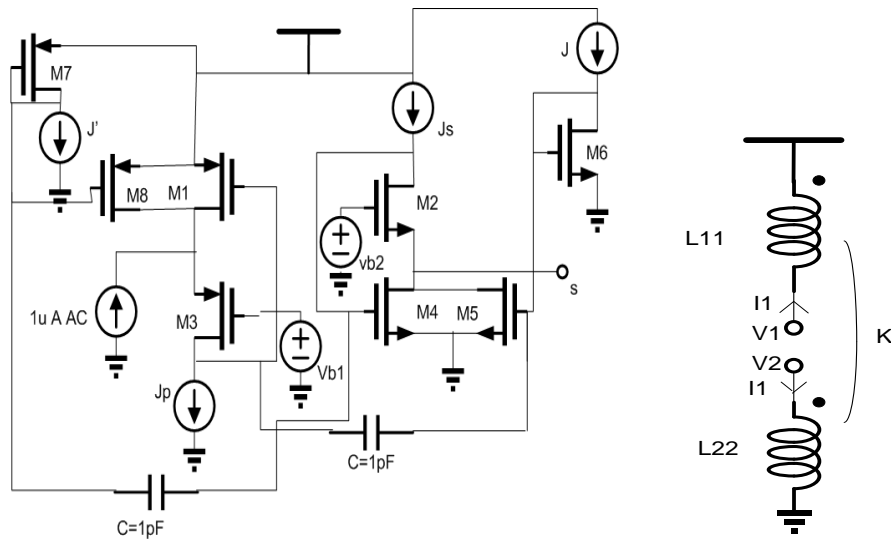


Figure 3.32 Structure of Bidirectional pMOS-nMOS circuit

**Cadence simulation:**

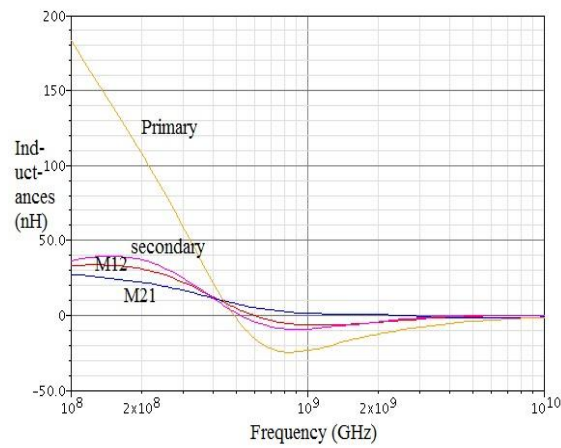


Figure 3.33 Plot of inductances

## 6. Bidirectional nMOS-pMOS circuit:

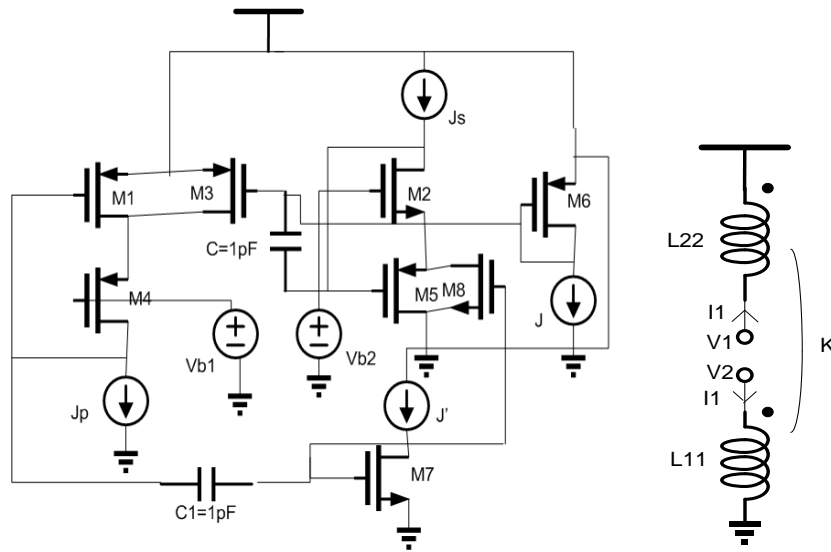


Figure 3.34 Structure of Bidirectional nMOS-pMOS circuit

## Cadence simulation:

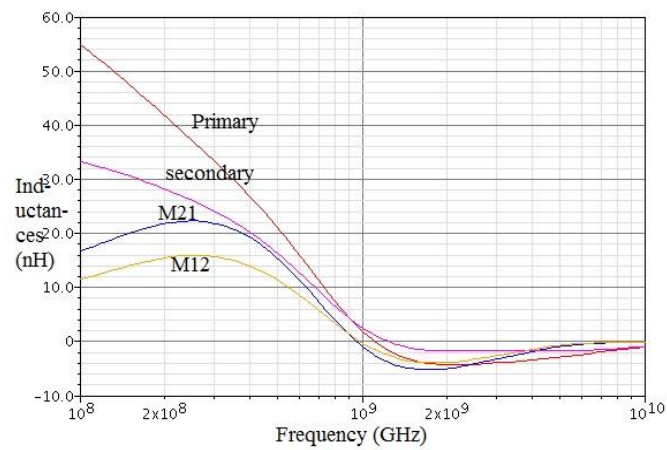


Figure 3.35 Plot of inductances

## Conclusion:

By observing the proposed active transformer circuits, the pMOS-nMOS circuits are giving high secondary self-inductances values and nMOS-pMOS circuits are giving high primary self-inductances values. Mutual inductances for both types are almost same.



### 3.4 Performances and Results :

**Table1:**

The table shows the simulation results of various active transformer configurations and proposed configurations.

| S.No. | Structure Name             | Tuning Voltages/Dimensions                                     | Biasing currents                                       | Coupling coefficient(K) at 200MHz |
|-------|----------------------------|--|--|-----------------------------------|
| 1.    | nMOS parallel circuit      | $V_{b1} = 0.8V, V_{b2} = 0.2V$<br>$W = 50\mu m, L = 0.18\mu m$ | $J_p = 150\mu A$<br>$J_s = 150\mu A$                   | 0.940                             |
| 2.    | nMOS series circuit        | $V_{b1} = 0.8V, V_{b2} = 0.2V$<br>$W = 50\mu m, L = 0.18\mu m$ | $J_p = 150\mu A$<br>$J_s = 150\mu A$                   | 0.747                             |
| 3.    | pMOS parallel circuit      | $V_{b1} = 0.8V, V_{b2} = 0.2V$<br>$W = 50\mu m, L = 0.18\mu m$ | $J_p = 150\mu A$<br>$J_s = 150\mu A$                   | 0.483                             |
| 4.    | pMOS series circuit        | $V_{b1} = 0.8V, V_{b2} = 0.2V$<br>$W = 50\mu m, L = 0.18\mu m$ | $J_p = 150\mu A$<br>$J_s = 150\mu A$                   | 0.796                             |
| 5.    | pMOS-nMOS parallel circuit | $V_{b1} = 0.8V, V_{b2} = 0.8V$<br>$W = 50\mu m, L = 0.18\mu m$ | $J_p = 150\mu A$<br>$J_s = 500\mu A$<br>$J = 150\mu A$ | 0.389                             |
| 6.    | pMOS-nMOS series circuit   | $V_{b1} = 0.8V, V_{b2} = 0.8V$<br>$W = 50\mu m, L = 0.18\mu m$ | $J_p = 150\mu A$<br>$J_s = 200\mu A$<br>$J = 300\mu A$ | 0.459                             |
| 7.    | nMOS-pMOS parallel circuit | $V_{b1} = 0.8V, V_{b2} = 0.8V$<br>$W = 50\mu m, L = 0.18\mu m$ | $J_p = 500\mu A$<br>$J_s = 300\mu A$<br>$J = 300\mu A$ | 0.25                              |

|     |                                 |   |   |                                      |
|-----|---------------------------------|---|---|--------------------------------------|
| 8.  | nMOS-pMOS series circuit        | $V_{b1} = 0.8V, V_{b2} = 0.8V$<br>$W = 50\mu m, L = 0.18\mu m$  | $J_p = 230\mu A$<br>$J_s = 300\mu A$<br>$J = 300\mu A$                    | 0.48                                 |
| 9.  | Bidirectional pMOS-nMOS circuit | $V_{b1} = 0.8V, V_{b2} = 0.8V$<br>$W = 50\mu m, L = 0.18\mu m$  | $J_p = 150\mu A$<br>$J_s = 500\mu A$<br>$J = 150\mu A$<br>$J' = 100\mu A$ | $K_{12} = 0.451$<br>$K_{21} = 0.376$ |
| 10. | Bidirectional nMOS-pMOS circuit | $V_{b1} = 0.8V, V_{b2} = 0.8V$<br>$W = 50\mu m, L = 0.18\mu m$  | $J_p = 150\mu A$<br>$J_s = 500\mu A$<br>$J = 150\mu A$<br>$J' = 150\mu A$ | $K_{12} = 0.466$<br>$K_{21} = 0.641$ |
| 11. | Bidirectional nMOS circuit      | $V_b = 1.3V$<br>$L = 180nm$ , Width<br>$M5 = M6 = 45\mu m$ ,<br>$M3 = M4 = 40\mu m$ ,<br>$M1 = M2 = 10\mu m$ ,<br>$M7 = M8 = 20\mu m$ | $V_g = 1.1V$  | 0.56                                 |

**Table 2:**

The table shows the calculated coupling coefficients of various configurations of active transformers

| Configuration      | Coupling coefficient(K)          |
|--------------------|----------------------------------|
| Nmos parallel      | 0.940                            |
| Nmos series        | 0.747                            |
| Pmos parallel      | 0.483                            |
| Pmos series        | 0.796                            |
| Pmos-Nmos parallel | 0.389                            |
| Pmos-Nmos Series   | 0.459                            |
| Nmos-Pmos parallel | 0.457                            |
| Nmos-Pmos Series   | 0.48                             |
| Bi Pmos-Nmos       | $K_{12}=0.451$<br>$K_{21}=0.376$ |
| BiNmos-Pmos        | $K_{12}=0.466$<br>$K_{21}=0.641$ |

### **3.5 Conclusion :**

The inductance values of active transformer are very high at low values of frequency and becomes to zero for high values of frequency. Also, if the tuning voltage increases, the values of inductances required for oscillations increases. The mutual inductances values are lower than the self-inductances values because transconductances of the coupling transistors are small. If the value of transconductances of active inductor transistors are small, then the value self-inductance decreases when frequency increases. In the proposed configurations, the nMOS-pMOS series circuit is getting more coupling coefficient and for the bidirectional case Bi nMOS-pMOS parallel circuit is getting more coupling coefficient.

# Chapter 4

## Active Transformer VCO configurations

### 4.1 Introduction :

In recent years, the need of active transformers in the manufacturing of voltage controlled oscillators has been increasing rapidly. First of all we have to know about the passive inductors and transformers before going into the active transformers. CMOS spiral inductors and transformers have found a broad range of applications in analog signal processing including impedance matching and gain-boosting in wireless transceivers, bandwidth improvement in broadband data communications over wire and optical channels, oscillators and modulators, RF bandpass filters, RF phase shifters, RF power dividers, and coupling of high-frequency signals, to name a few. Traditionally, passive inductors and transformers are off-chip discrete components. The need for off-chip communications with these passive components severely limits the bandwidth, reduces the reliability, and increases the cost of systems. Since early 1990s, a significant effort has been made to fabricate inductors and transformers on a silicon substrate such that an entire wireless transceiver can be integrated on a single substrate monolithically. In the mean time, the need for a large silicon area to fabricate spiral inductors and transformers has also sparked a great interest in and an intensive research on the synthesis of inductors and transformers using active devices, aiming at minimizing the silicon consumption subsequently the fabrication cost and improving the performance.

Similar to spiral transformers that are constructed by coupling two spiral inductors via a magnetic link, a gyrator-C active transformer can be constructed by connecting two gyrator-C active inductors via a “magnetic” link, which is also synthesized using an electrical network. The two active inductors constituting the active transformer are referred to as the primary winding and the secondary winding of the transformer, depending upon the flow of the signals of the transformer. Gyrator-C active inductors are two-port networks and have two pairs of nodes, namely, the interface nodes and internal nodes. The coupling between the two gyrator-C active inductors of an active transformer can be established via either the interface nodes or the internal nodes of the active inductors.

## 4.2 VCO configurations :

**First Configuration : pMOS for  $V_{dd}$  and nMOS for ground(Coupling of active transformer)**

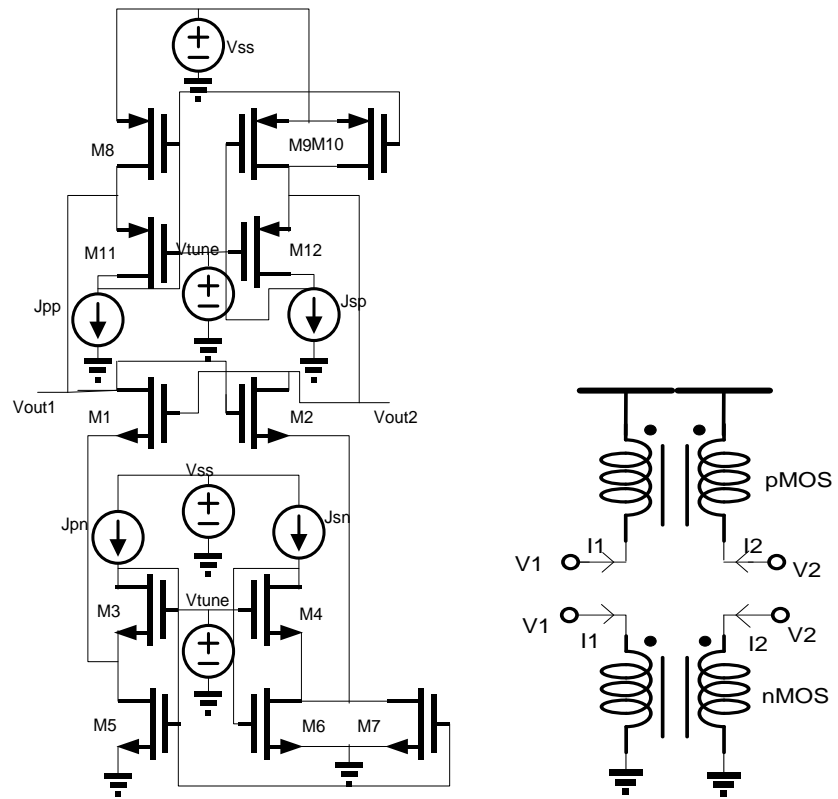


Figure 4.1 Schematic of first configuration of Active Transformer VCO

In this configuration, the active transformers are placed on both ends (drain and source) of the cross-coupled VCO structure. The PMOS active transformer is placed at drain of the cross-coupled pair and NMOS active transformer is placed at source of that pair. The transistor M1 drain is connected to primary of PMOS transformer and M2 drain is connected to secondary of PMOS transformer. The source of M1 is connected to primary of NMOS transformer and M2 source is connected to secondary of NMOS transformer. The coupling can be done using the transconductor connected from primary to the secondary and the coupling is only single-directional. The tuning voltage is applied at the gate of one of the transconductors of back to back connection of active inductor. The current sources Js and Jp are used to tune self-inductance and mutual inductance of the active transformer. They are also used to vary the quality factor values of the tank circuits.

## Simulation and Results:

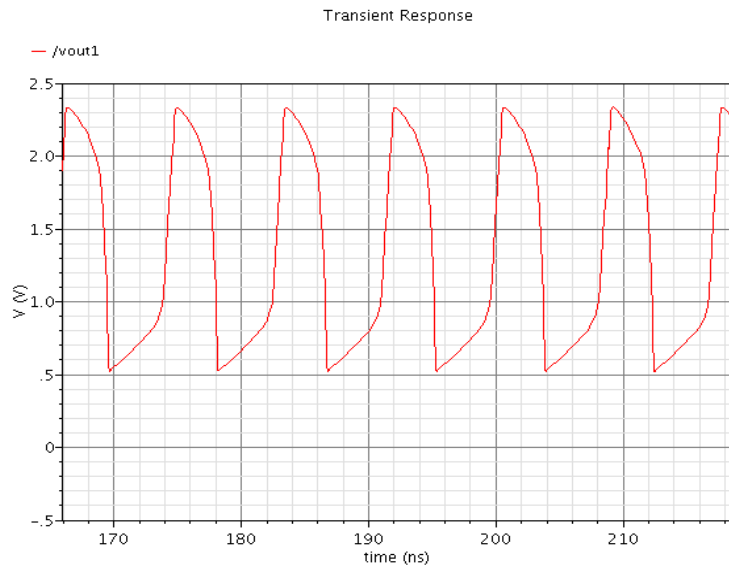


Figure 4.2 Plot of Transient Response

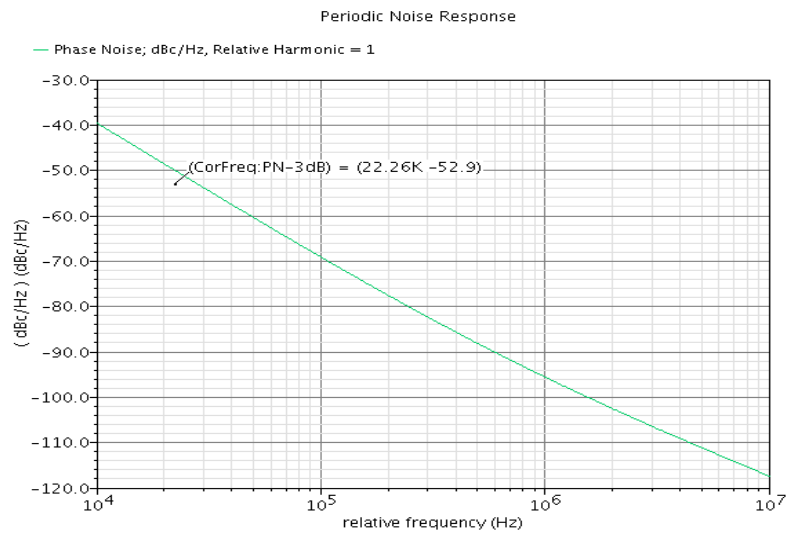


Figure 4.3 Plot of Phase Noise

**Table:**

| Dimensions   | Current sources                               | Tuning Voltages | Fundamental or carrier Frequency(MHz) | Phase noise at 1MHz offset (dBc/Hz) |
|--|---|-----------------|---------------------------------------|-------------------------------------|
| M1,M2 - 100 $\mu$ m<br>M3,M8 - 45 $\mu$ m<br>M5,M5,M11,M9 - 50 $\mu$ m<br>M4,M12 - 40 $\mu$ m<br>M10,M7 - 10 $\mu$ m | $J_{pp}=J_{pn}=J_{sn}=J_{sp}$<br>$= 500\mu$ A | $V_{tune} = 1V$ | 104.759                               | -95.44                              |

**Conclusion:**

At the carrier frequency of 1.32GHz, the VCO circuit with the active transformer of coupling of pMOS for  $V_{dd}$  coupling and nMOS for ground coupling, the phase noise of -80.59 dBc/Hz is achieved.



## Second configuration : pMOS-nMOS coupling (Unidirectional)

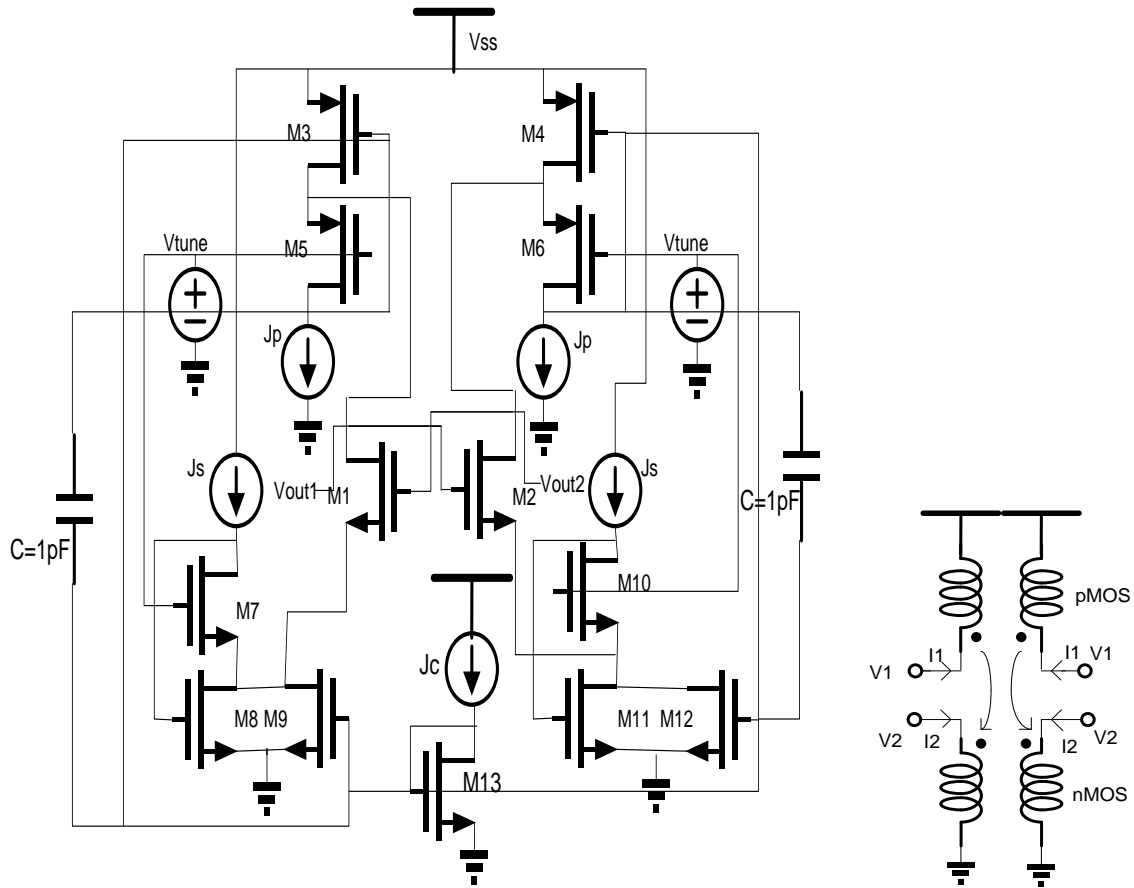


Figure 4.4 Schematic of First configuration of Active Transformer VCO

In this configuration, the active transformer is placed on both ends of the cross-coupled VCO structure. The primary of the transformer is connected to the drain of NMOS and the primary part of the transformer is the PMOS active inductor structure. The secondary part of the transformer is connected to source of the NMOS structure and the secondary part of the transformer is NMOS active inductor structure. The coupling can be done using the transconductor connected from primary to the secondary and the coupling is only single-directional. The tuning voltage is applied at the gate of one of the transconductors of back to back connection of active inductor. The current sources Js and Jp

are used to tune self-inductance and mutual inductance of the active transformer. They are also used to vary the quality factor values of the tank circuits.

### Simulation and Results:

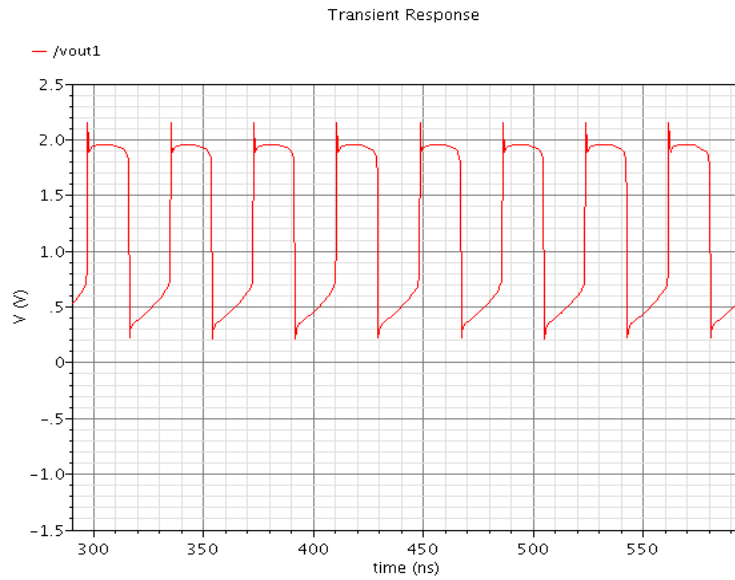


Figure 4.5 Plot of Transient Response

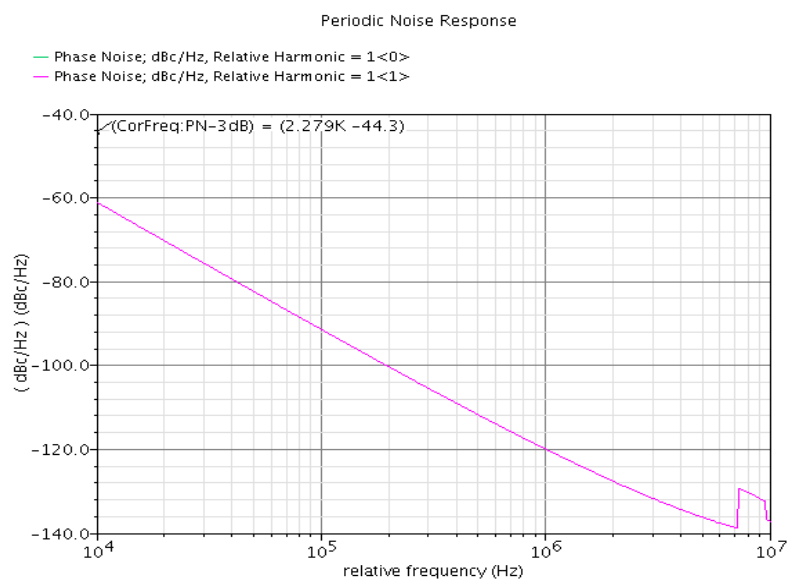


Figure 4.6 Plot of phase noise

**Table:**

| Dimensions   | Current sources  | Tuning Voltages        | Fundamental or carrier Frequency(MHz) | Phase noise at 1MHz offset (dBc/Hz) |
|--|--|------------------------|---------------------------------------|-------------------------------------|
| M1,M2,M9,M12 - 100 $\mu$ m<br>M3,M4 - 45 $\mu$ m<br>M5,M6,M11,M8 - 50 $\mu$ m<br>M10,M7 - 40 $\mu$ m<br>M13-20 $\mu$ m | Jp = 550 $\mu$ A<br>Js = 300 $\mu$ A<br>Jc = 150 $\mu$ A | V <sub>tune</sub> = 1V | 31.71                                 | -119.96                             |

**Conclusion:**

At the carrier frequency of 1.56 GHz, the VCO circuit with the active transformer of unidirectional coupling of pMOS for primary(connected to drain of cross-coupled pair) and nMOS for secondary(connected to source of cross-coupling pair), the phase noise of -98 dBc/Hz is achieved.

### Third Configuration : pMOS-nMOS coupling (Bidirectional)

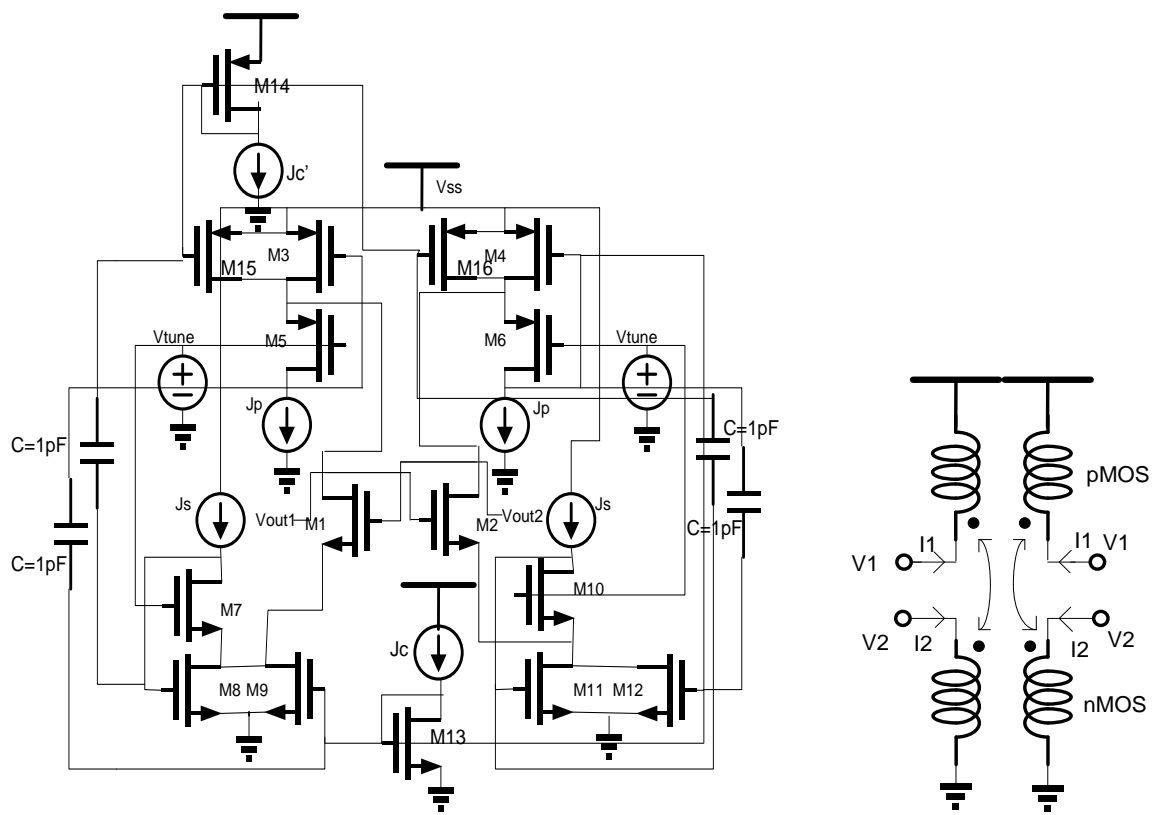


Figure 4.7 Schematic of third configuration of Active Transformer VCO

In this configuration, the active transformer is placed on both ends of the cross-coupled VCO structure. The primary of the transformer is connected to the drain of NMOS cross-coupled pair and the primary part of the transformer is the PMOS active inductor structure(primary part). The secondary part of the transformer is connected to source of the NMOS structure and the secondary part of the transformer is NMOS active inductor structure(secondary part). The coupling can be done using the transconductor connected from primary to the secondary and the coupling is bidirectional. The tuning voltage is applied at the gate of one of the transconductors of back to back connection of active inductor. The current sources  $J_s$  and  $J_p$  are used to tune self-inductance and mutual inductance of the active transformer. They are also used to vary the quality factor values of the tank circuits.

## Simulation and Results:

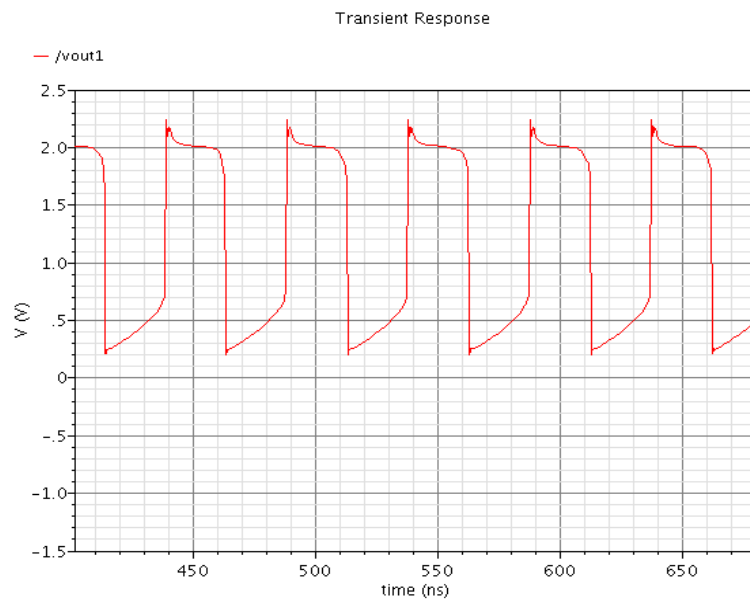


Figure 4.8 Plot of Transient response

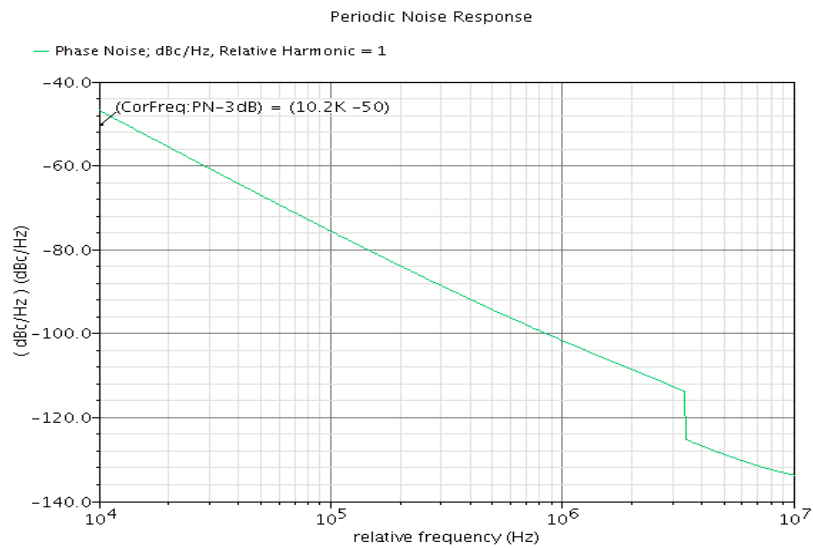


Figure 4.9 Plot of phase noise

**Table:**

| Dimensions  | Current sources  | Tuning Voltages        | Fundamental or carrier Frequency(MHz) | Phase noise at 1MHz offset (dBc/Hz) |
|---|--|------------------------|---------------------------------------|-------------------------------------|
| M1,M2,M9,M12 - 100 $\mu$ m<br>M3,M4 - 45 $\mu$ m<br>M5,M6,M11,M8,M15,M16,M14 - 50 $\mu$ m<br>M10,M7, - 40 $\mu$ m<br>M13-20 $\mu$ m | Jp = 550 $\mu$ A<br>Js = 300 $\mu$ A<br>Jc = 150 $\mu$ A<br>Jc' =100 $\mu$ A | V <sub>tune</sub> = 1V | 23.32                                 | -101.73                             |

**Conclusion:**

At the carrier frequency of 1.99 GHz, the VCO circuit with the active transformer of bidirectional coupling of pMOS for primary(connected to drain of cross-coupled pair) and nMOS for secondary(connected to source of cross-coupling pair), the phase noise of -96.0865 dBc/Hz is achieved.

**Fourth Configuration :**

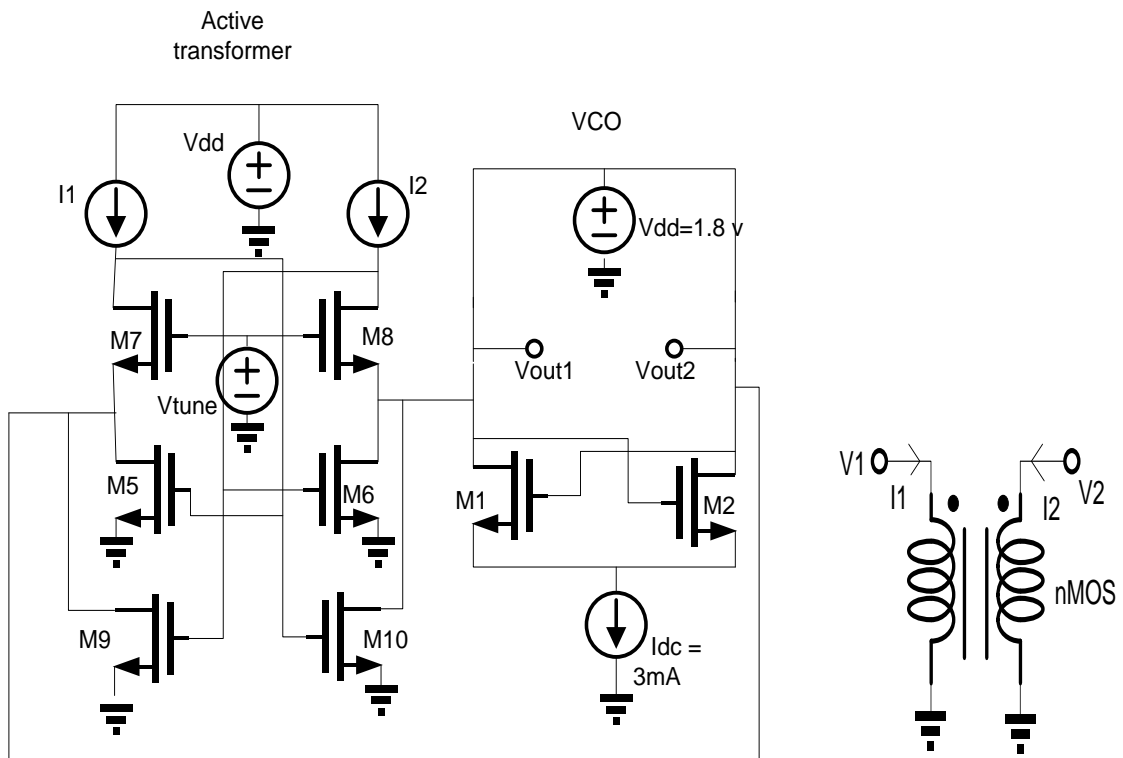


Figure 4.10 Schematic of fourth configuration of Active Transformer VCO

**Simulation and Results:**

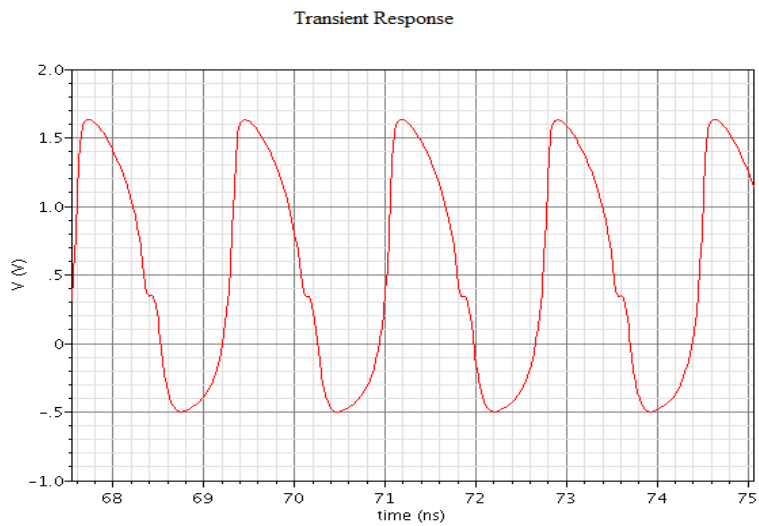


Figure 4.11 Plot of Transient Response

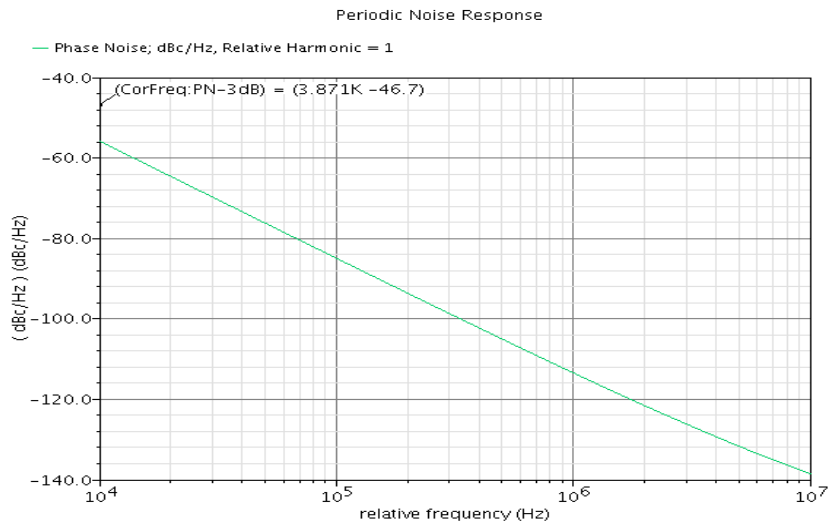


Figure 4.12 Plot of Phase noise

**Table:**

| Dimensions  | Current sources          | Tuning Voltages        | Fundamental or carrier Frequency(GHz) | Phase noise at 1MHz offset (dBc/Hz) |
|---|--------------------------|------------------------|---------------------------------------|-------------------------------------|
| M1,M2,M9,M12 - 10μm<br>M3,M4 - 30μm<br>M7,M8 - 45μm<br>M5,M6 - 40μm | I1 = 130μA<br>I2 = 130μA | V <sub>tune</sub> = 1V | 0.8                                   | -113.80                             |



### Fifth Configuration: nMOS-pMOS coupling

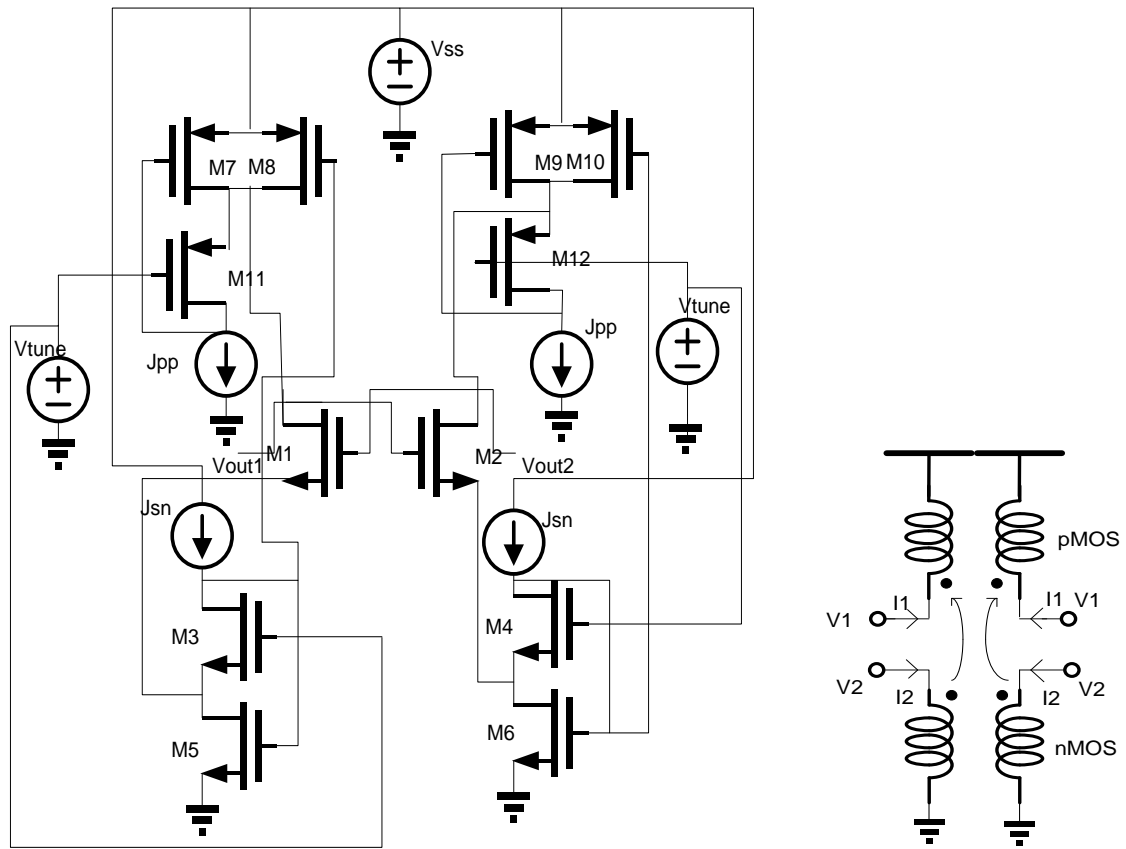


Figure 4.13 Schematic of nMOS-pMOS active transformer

### Simulation and Results:

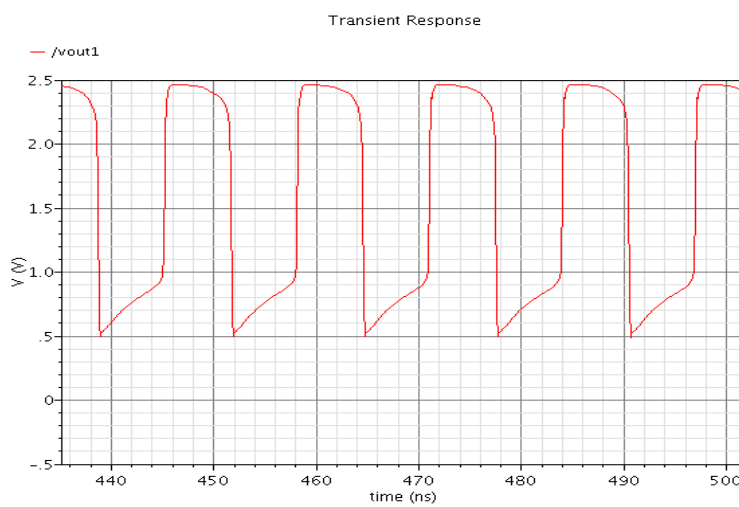


Figure 4.14 Plot of Transient response

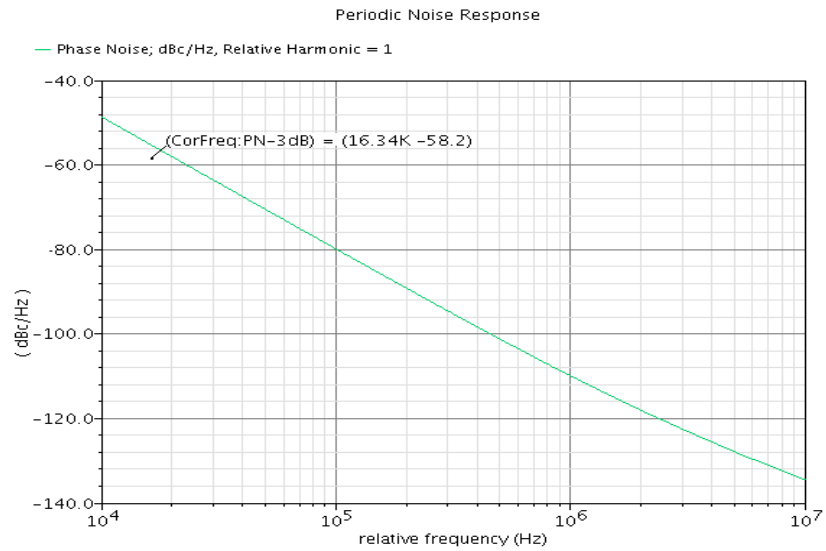


Figure 4.15 Plot of Phase Noise

**Table:**

| Dimensions               | Current sources     | Tuning Voltages | Fundamental or carrier Frequency(MHz) | Phase noise at 1MHz offset (dBc/Hz) |
|--------------------------|---------------------|-----------------|---------------------------------------|-------------------------------------|
| M1,M2 - 100 $\mu$ m      | $J_{pp} = 150\mu$ A | $V_{tune} = 1V$ | 77                                    | -110                                |
| M5,M6,M7,M9 - 50 $\mu$ m | $J_{sn} = 400\mu$ A |                 |                                       |                                     |
| M3,M4 - 45 $\mu$ m       |                     |                 |                                       |                                     |
| M11,M12 - 40 $\mu$ m     |                     |                 |                                       |                                     |

**Performances :**

|   | Frequency (Hz) | Active transformer<br>Tuning Phase Noise<br>(dBc/Hz) |
|---|----------------|--|
| Passive T VCO   | 4.47 G         | -125   |
| Active T VCO (pMOS-<br>nMOS<br>coupling)(Unidirectional)        | 31.71M         | -119.96  |
| Active<br>Transformer(pMOS-<br>nMOS<br>coupling)(Bidirectional) | 23.32M         | -101.73  |
| Active T VCO(nMOS-<br>pMOS coupling)                            | 77 M           | -110   |
| Active T VCO(pMOS<br>$V_{dd}$ and nMOS<br>grounded)             | 104.759M       | -95.44   |
| Active T VCO<br>(Grounded)                                      | 0.8 G          | -113.80  |

**Conclusion :**

The phase noise performance for passive transformer VCO is superior to any of the four configurations of the active transformer VCOs. Among active transformer VCOs, the transformer of pMOS-nMOS(Unidirectional) offers good performance . Actually, the phase noise performance of active transformer VCO is far to that of passive one, here it is approaching to passive transformer phase noise value.

# Chapter 5

## Conclusion and Future work

### 5.1 Conclusion :

In place of the passive transformer that is used in the passive transformer VCO which occupies more area and gives fixed value of inductance, low self-resonant frequency, we can use active transformers in the VCO circuits which occupies small area in the chip design and also offers tunable inductance and tunable coupling coefficient. The various configurations of active transformer connections for the VCO circuits are possible and their performances are studied. For the new topologies, the nMOS-pMOS circuit is offering more coupling coefficient as well as good phase noise performance.

### 5.2 Future Work :

The active transformers we are using are grounded transformers for nMOS structures and railed to supply voltage for pMOS structures. The floating point structure of the active transformer (i.e., neither grounded nor to supply voltage ) design and study its performances for the VCO circuits is the future development of this work.

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