A Smartphone-based High Sensitivity Impedance Readout Circuit for Milk Adulteration

Sadi Nandini

A Dissertation Submitted to

Indian Institute of Technology Hyderabad

In Partial Fulfillment of the Requirements for

The Degree of Master of Technology

भारतीय प्रौद्योगिकी संस्थान हैदराबाद

Indian Institute of Technology Hyderabad

Department of Electrical Engineering

June, 2019

Declaration

I declare that this written submission represents my ideas in my own words, and where others' ideas or words have been included, I have adequately cited and referenced the original sources. I also declare that I have adhered to all principles of academic honesty and integrity and have not misrepresented or fabricated or falsified any idea/data/fact/source in my submission. I understand that any violation of the above will be a cause for disciplinary action by the Institute and can also evoke penal action from the sources that have thus not been properly cited, or from whom proper permission has not been taken when needed.

S. Nandini

(Signature)

Sadi Nandini

(– Student Name –)

EE17MTECH11016

(Roll No)

Approval Sheet

This thesis entitled **A Smartphone based high sensitivity Impedance Readout circuit for Milk Adulteration** by **Sadi Nandini** is approved for the degree of Master of Technology.

Dr Naresh Kumar Emani
Examiner

-Name & Affiliation-
Examiner

for Dr Shiv Govind Singh
Adviser

Dr Gajendranath Chowdary
Co-Adviser

Dr Ashudeb Dutta
Chairman

Acknowledgements

First of all, I would like to thank God Almighty for keeping me in good health and for all the grace.

I would like to express my deepest gratitude to my supervisors Dr.Shiv Govind Singh and Dr.Gajendranath Chowdary, who were a constant source of encouragement and moral support. I would like to sincerely thank them for their guidance, genuine comments and valuable suggestions throughout the course of research.

I owe my special thanks to Pravanjan Patra and Suryasnata Tripathy for having patiently helped me whenever I approached them.

I would like to thank my classmates especially Rahul and Mohith and senior research scholars for being there with me at all times.

Lastly, I wish to pay tribute to my parents and my lovely sister. I couldn't have achieved anything without their support and I am indebted to them all my life.

Abstract

The proposed work develops a lab-on-chip platform to detect the milk adulteration which exploit the smartphone to overcome the external battery usage and calibration. To have a low cost and convenient platform for sensing, the interface circuit is powered through the smartphone and calibration is done through the customized built Application using Android studio and Arduino IDE.A great accuracy of 0.1Ω change is achieved by this work. The OTA designed has a high GBW of 110 MHz, high gain of 90 dB and very low noise floor .Apart from this, a wide range resistive readout circuit is also implemented which could sense the resistance ranging from 10KΩ-1GΩ.The whole design is analyzed in TSMC 0.18µ technology.

Nomenclature

AC	Alternating Current
ADC	Analog-Digital Convertor
APK	Android Application Package
DR	Dynamic Range
GBW	Gain Bandwidth Product
LSB	Least Significant Bit
ICMR	Input Common Mode Range
IDE	Integrated Development Environment
PM	Phase Margin
PVT	Process, Voltage, Temperature
PSRR	Power Supply Rejection Ratio

Contents

List of Figures

List of Tables

Chapter 1

1 Introduction

Milk adulteration has become a major problem in Indian subcontinent with 70 per cent milk samples collected across the country failing to confirm desired standards. Separate detection chemistry for individual adulterants is very time consuming and it needs laboratory set-up which is Cost-ineffective. The high frequency impedance of the unadulterated milk falls within the range 615-640 ohms. At high frequency, the capacitive elements have negligible effect on the overall milk sample, resulting in the pure resistive section. So, the proposed work develops a lab-on-chip platform where great level of accuracy is being targeted. The circuit is powered through the smartphone which opens the door for the low cost and reduced complexity. The calibration of the readout circuit is done using the customized built App using Android studio and Arduino Uno.

1.1 Thesis Organisation

- Chapter 2 describes the circuit level implementation of impedance detector and the motivation behind each block.
- Chapter 3 discusses the architecture, design specifications of OTA, and simulation results of the complete circuit under various load conditions.
- Chapter 4 describes the architecture of the wide range resistive detector and its simulation results.
- Chapter 5 presents conclusion, future scope and References.

Chapter 2

2 Impedance Readout circuit for Milk Adulteration

2.1 Introduction

The proposed circuit measures the impedance of the milk sample with different resolutions, where the adulterated milk sample can be detected with great accuracy.

So targeting for the cost effective method to measure, we make use of the cell phone to power up the board and display the calibrated impedance using Arduino board.

A separate App is being developed, to sense the output, process and back calibrate to show the exact value in the cell phone. In this work, the frequency of the on-chip oscillator can be varied using digital potentiometers which can be configured through the Arduino IDE platform.

2.2 Circuit implementation and working:

The working of the whole circuit is summarized as follow:

In order to measure the impedance of the milk sensor which falls in the range of 100-1000Ω, different resolutions are targeted in 3 different sub-ranges.

100 - 600 Ω , a resolution of 0.5 Ω is desired

600 - 700 Ω , a resolution of 0.1 Ω is desired

700 - 1000 Ω , a resolution of 0.3Ω is desired.

To achieve the specified resolutions in the particular ranges, we require 6.44 milliamps in the first range ,32.2 milliamps in the second range, 10.73 milliamps in the third range so that ADC operating at 3.3 volt supply could resolve one LSB change(3.3 millivolts for a 10 bit ADC).

To achieve the same, three different currents needs to be generated. Despite doing that, initially 2.5 milliamps AC current is pushed into the sensor. The remaining fraction of the current needed is introduced as an amplification factor to achieve the targeted resolutions in 3 sub ranges of the Impedance sensor.

Sub-range 1(100Ω-600Ω):

When the sensor is in the range 1, it occupies the voltage range of 0.25-1.5V after passing the 2.5 milliamps AC current. In this range, a resolution of 0.5Ω is targeted.

100Ω-600Ω impedance range should be completely mapped to ADC full scale voltage (0-3.3V).i.e. whenever there is a change of 0.5Ω, it should correspond to change of 1 LSB of 10 bit ADC (3.3 millivolts).In order to map the (100Ω-600Ω) range to ADC range (0-3.3V), 0.25-1.5V (Sub range 1) should correspond to ADC (0-3.3V).To implement that, a subtractor stage is employed to subtract 0.25 V from the sub range 1 with the required gain of 2.6 .

Sub-range 2 (600Ω-700Ω):

When the sensor is in this range, it occupies the voltage range of 1.5-1.74 V after passing the 2.5 milliamps AC current. In this range, a resolution of 0.1Ω is targeted.

To implement that, a difference amplifier stage is employed to subtract 1.5 V from the Sub-range 2 with the required gain of 13.

Sub range 3 (700Ω-1000Ω):

When the sensor is in this range, it occupies the voltage range of 1.74-2.5 V after passing the 2.5 milliamps AC current. In this range, a resolution of 0.3Ω is targeted.

To implement that, a difference amplifier stage is employed to subtract 1.74 V from the Sub-range 3 with the required gain of 4.3.

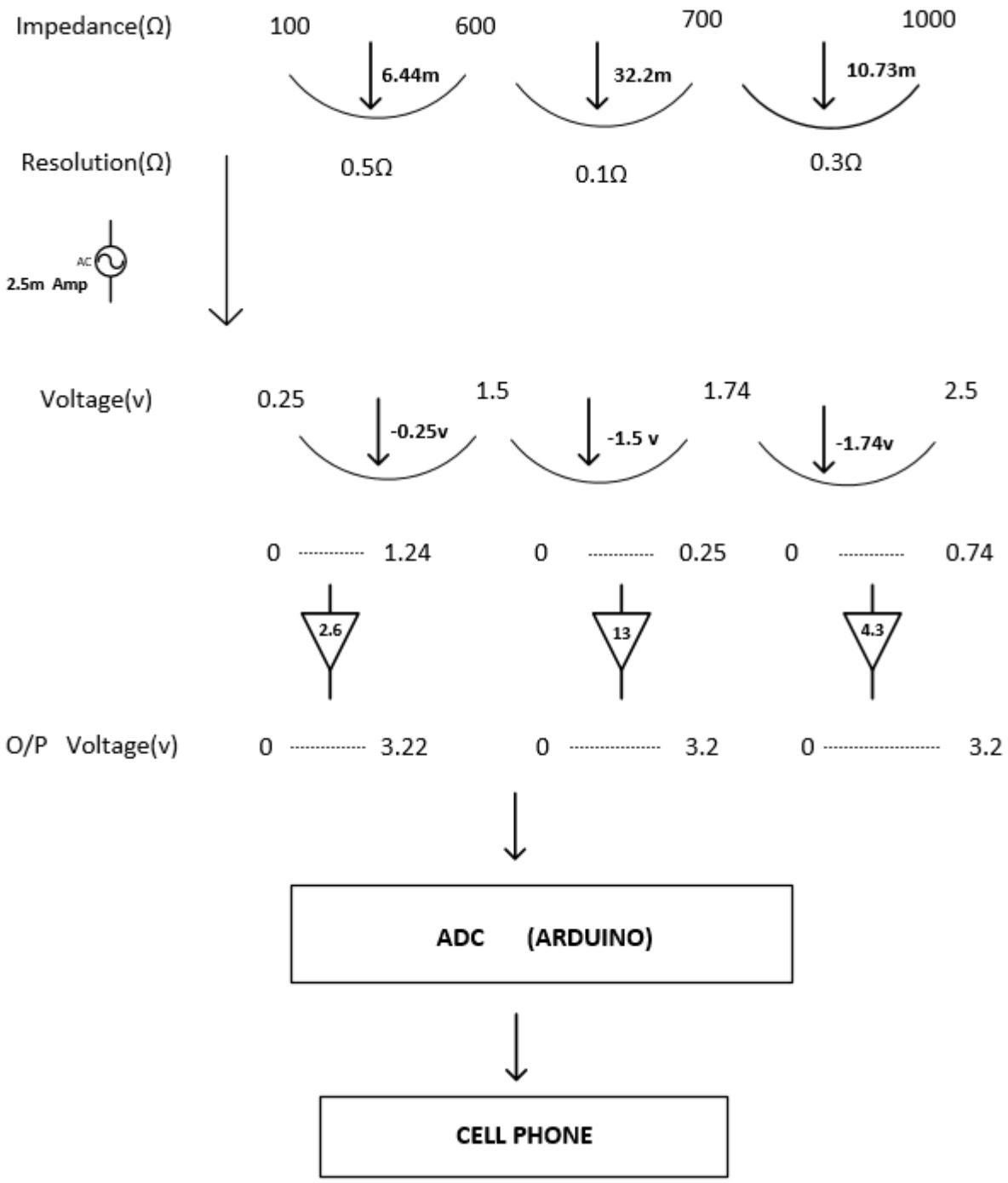


Figure 2-1 Mathematical representation

2.3 Wien bridge oscillator

Wien bridge oscillator is a sinusoidal wave oscillator .It consists of a series RC circuit connected to the parallel RC circuit which employs the positive feedback network and the voltage divider circuit (Rf and R1) employs the negative feedback network.

The op-amp is used in noninverting mode provides a phase shift of 0^0. Resistors Rf and R1 determine the amplifier gain and are selected to make the loop gain equal to 1.The feedback circuit parameters are selected such that ,there is a frequency at which there is zero phase shift for the signal fed back to non-inverting terminal.[2]

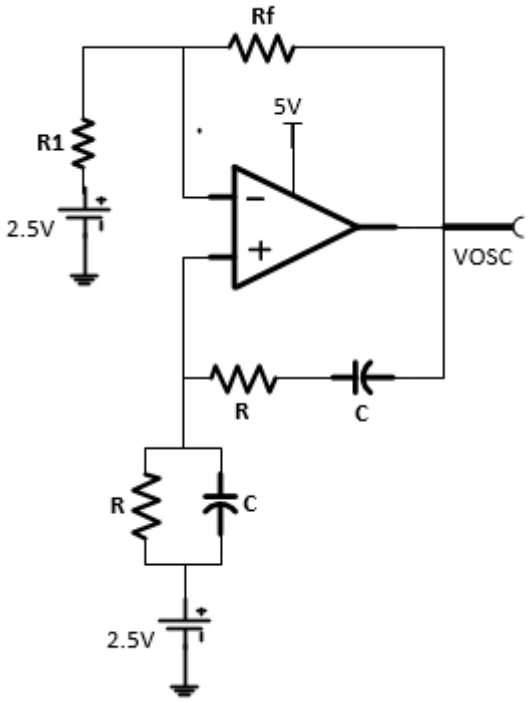


Figure 2-2 Wien bridge oscillator

The frequency of oscillation is given by

$$\text{Fosc} = \frac{1}{2\pi RC}$$

Gain required for sustained oscillations:

$$\frac{Rf}{R1} \geq 2$$

2.4 Butterworth second order low filter and high pass filter

The sine wave generated from the Wien bridge oscillator contains harmonics apart from the fundamental frequency. To get a pure sinusoidal waveform, filtering action is required.so a Butterworth second order filter is employed to remove the unwanted frequencies. The cut-off frequency is chosen such that higher frequencies beyond it rolls down at the rate of 40 dB/decade.

$$\text{F} = \frac{1}{\sqrt{2\pi R1C1R2C2}}$$

There is a positive feedback employed to ensure that there is fast transition from pass band to stop band and to avoid peaking response around cut-off frequency.

The oscillator produces a sine wave of 100 KHz with odd harmonics starting from 300 KHz, 500 KHz and so on. To limit the response till 100 KHz, cutoff frequency is chosen to be 150 KHz. To remove the dc component, a high pass filter is employed.

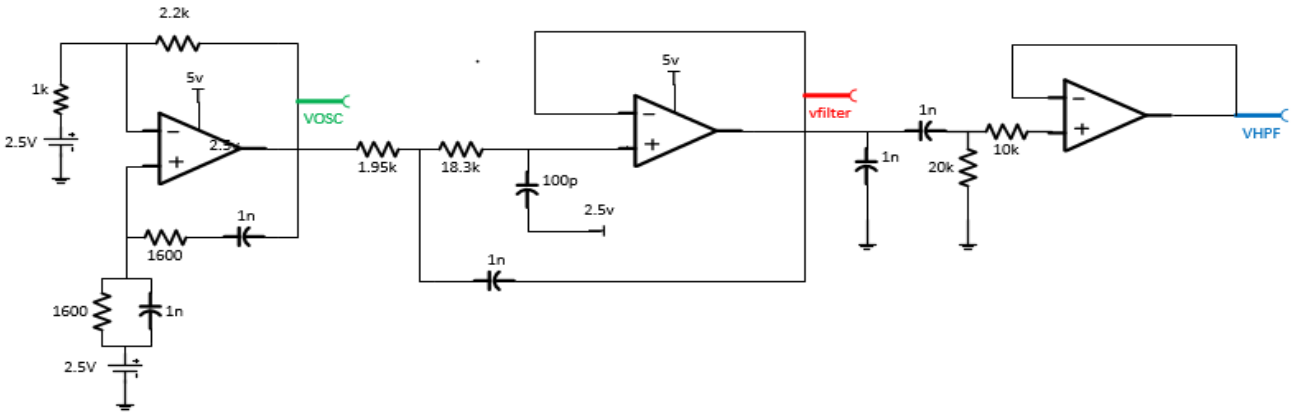


Figure 2-3 second order low pass and high pass filter

2.5 Voltage to current convertor

In most cases, the output voltage is not transmitted directly to the destination due to the addition of noise and wire impedance. In such cases, this circuit plays a vital role. As per my requirement, it is desired to send a 2.5 milliamps AC current into the sensor while making use of the above mentioned advantage.

Following circuit shows the voltage to current converter using operational amplifier[3]. It consist of simple resistance connected to the inverting and non-inverting terminals of op amp.

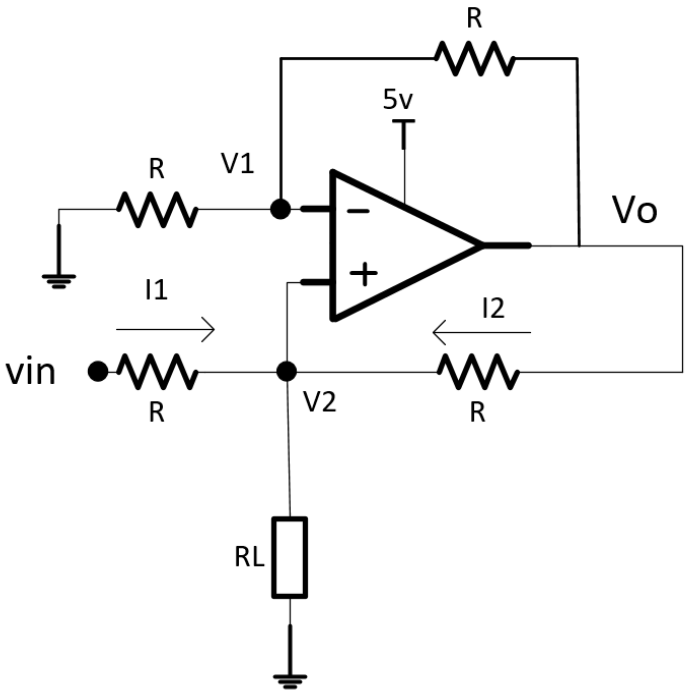


Figure 2-4 V- I convertor

Mathematical calculation for the current through the Load (sensor)

$I1 = \left(\frac{Vin - V2}{R}\right)$ $I2 = \left(\frac{Vin - V2}{R}\right)$

$$IL = I1 + I2 = \left(\frac{Vin - V2}{R}\right) + \left(\frac{Vo - V2}{R}\right)$$

And we have

Vo = 2V2

,

So the current through the load is given by

$$IL = \left(\frac{Vin}{R}\right)$$

From the filter, a pure sinusoidal wave is obtained, oscillating all the way from 0 to 5 volts (VDD supply). The V to I convertor converts the AC voltage to the sinusoidal current of 2.5 milliamps by choosing the value of R=1k ohms. Now, this current is pushed into the sensor to produce the desired output voltage which is then detected by peak detector followed by comparators to identify the different ranges wherein different resolutions are desired.
After passing the initial current of 2.5 milliamps into the sensor, an AC voltage range of 0.25-2.5 volts is obtained. So a peak detector is employed next to the V to I convertor to convert the bi-directional voltage to the unidirectional voltage.

2.6 Peak detector

It detects and holds the peak of the input signal. The circuit consisting of only diode and capacitor can pass the input voltage greater than the forward diode drop (i.e 0.7V typically).So , in order to pass the voltage less than the diode drop, say in order of few millivolts, we make use of the op-amp[3].

The operation of op-amp peak detector can be explained as follows:

Vout < Vin; The diode is ON and the capacitor charges to peak value of an input,
Vout < Vin; The diode is OFF and the capacitor holds the peak value of an input.

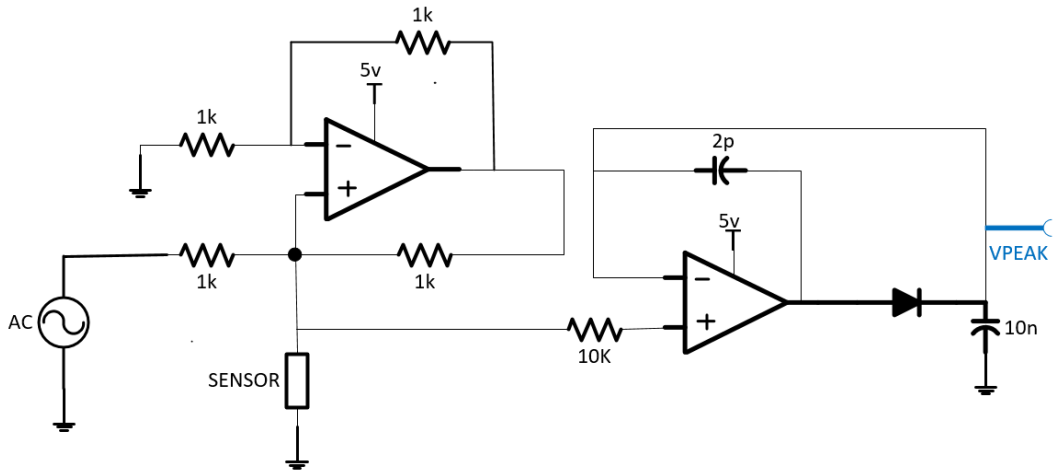


Figure 2-5 Peak detector

2.7 Comparator stage

To identify the range of operation, the peak detector output is compared with pre-defined voltage levels of 1.49 volts and 1.74 volts using op-amp as a comparator.

The output logic level of comparators is used to turn on the corresponding switches of the particular ranges.

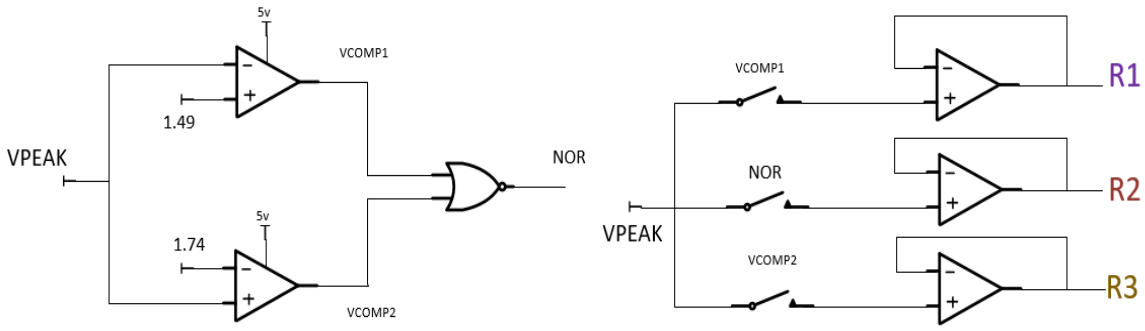
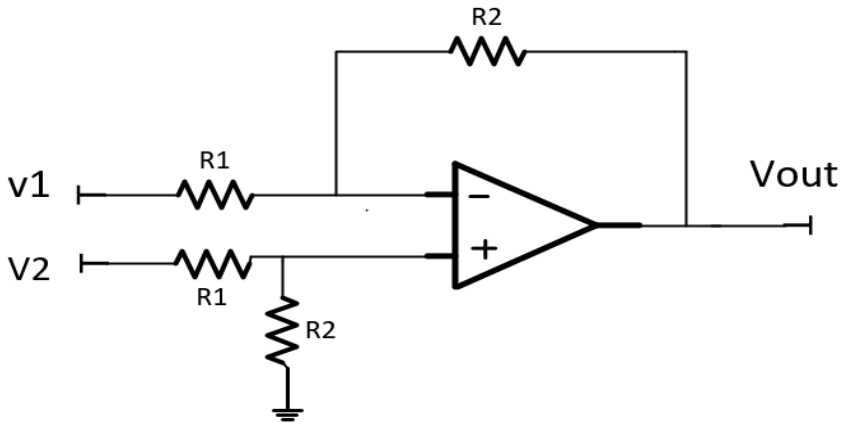


Figure 2-6 Comparator stage

2.8 Difference amplifier

It is a subtractor circuit which amplifies the difference voltage between the inverting and the non-inverting terminals. The gain of the circuit can be set using resistances R2 and R1.[3]



$$Vout = \frac{R2}{R1}(V2 - V1)$$

Figure 2-7 Differential amplifier

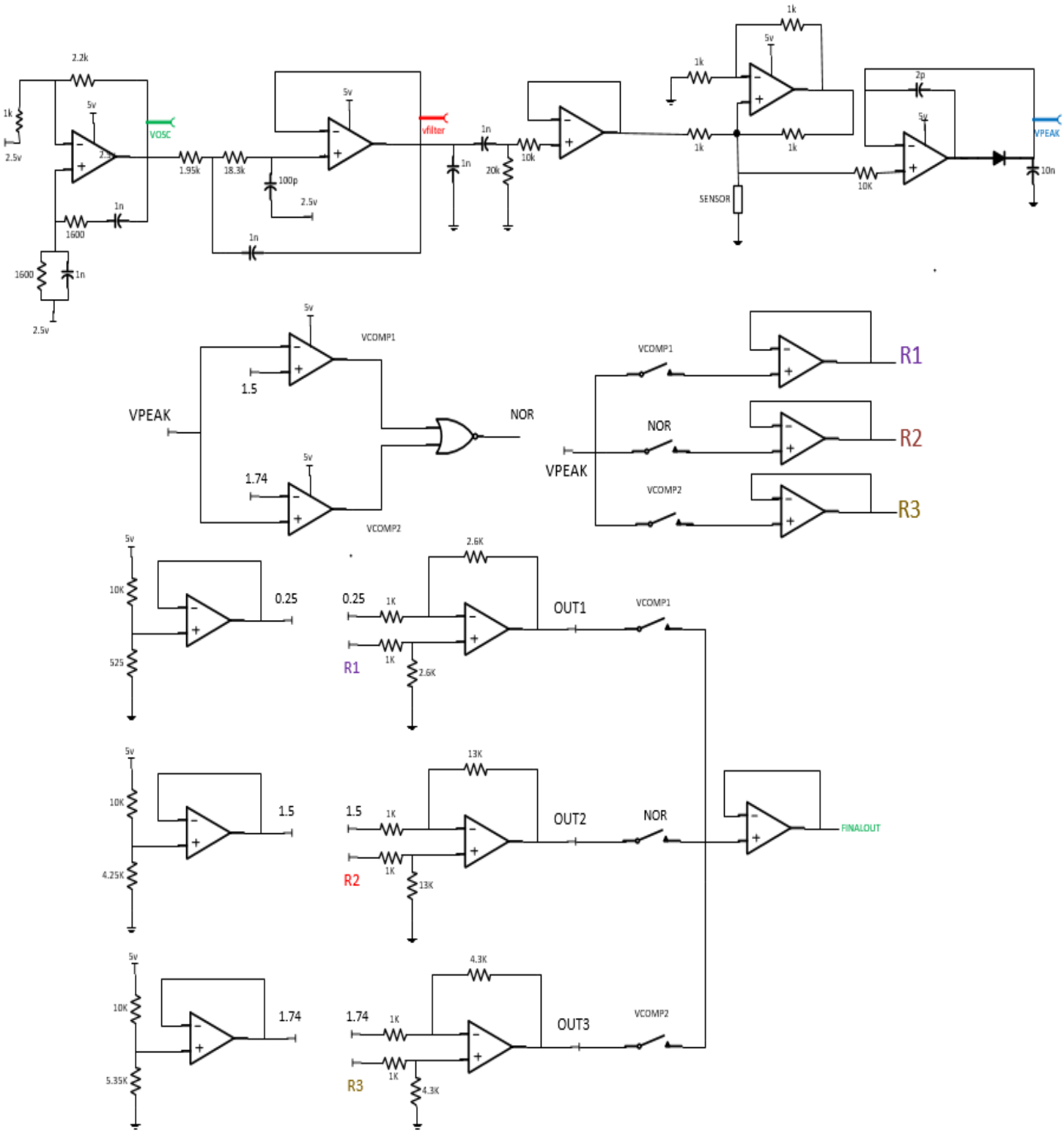


Figure 2-8 Impedance readout circuit

2.9 Custom built App for impedance readout circuit

Android Studio:

It is the official IDE platform where you can develop your Application for any Android device. The App built can work for Android Versions above 4.0.To build any Android App, you require Activity_main.xml file which contains the Layout view describing the details like Height, width, buttons you want to view on the homepage of the App. Manifest.xml file is used for defining user's permission for the external devices connected.MainActivity.java is the source code editor where you can program your Application. There is a virtual Android Emulator to view and check the output of your Application. Once the Application is developed, the APK file can be transferred to the phone.[4]

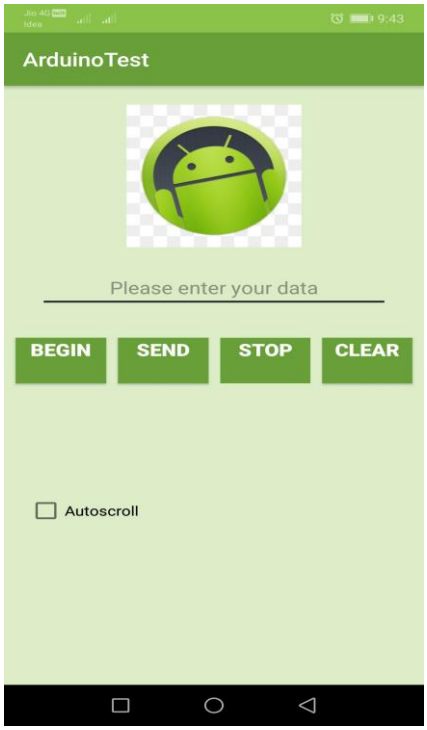


Figure 2-9 Homepage of the customized Application

Chapter 3

3 Circuit design

Circuit design for proposed impedance readout detector involves designing of OTA with 3.3 V supply. These are analyzed and designed in TSMC 0.18 µm CMOS technology.

3.1 The architecture of two-stage OTA:

The present work requires an op-amp which has high gain, low noise and moderate UGB, rail to rail input and output common range. To meet these requirements, self-biased Folded cascode configuration is chosen with both PMOS and NMOS input pair. In general two stage OTA's are designed for achieving high swing and high gain. First stage provides high gain and second stage provides high swing.

Self-biasing:

Biasing of the transistors should be done in such a way that all the transistors should be in saturation to get maximum gain. In this work, self-biasing is chosen such that additional biasing network is not required. From the Fig. 3-1, the connection from gate of M1 to drain of M2 ensures that M1 is in saturation .If the resistance is chosen in such a way such that its voltage drop is Vov, then a similar connection as above make sure that M2 is always in saturation .

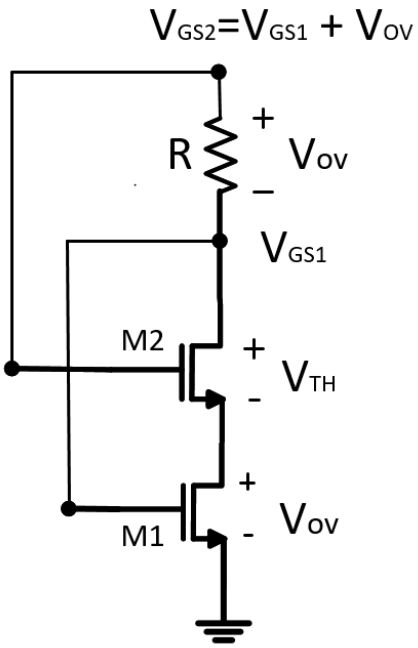


Figure 3-1 Self biasing network[5]

Maximum ICMR of Folded cascode topology:

The maximum ICMR can exceed beyond Vdd supply in this topology. For M1 to be in saturation, $V_{ICMRmax} = V_{D1} + V_{TH1,}$ where $V_{D1} = Vdd - V_{DS6.}$

$V_{ICMRmax} = Vdd - V_{DS6} + V_{TH1}$

If $V_{DS6} \leq V_{TH1,}$ then $V_{ICMRmax} \geq Vdd.$

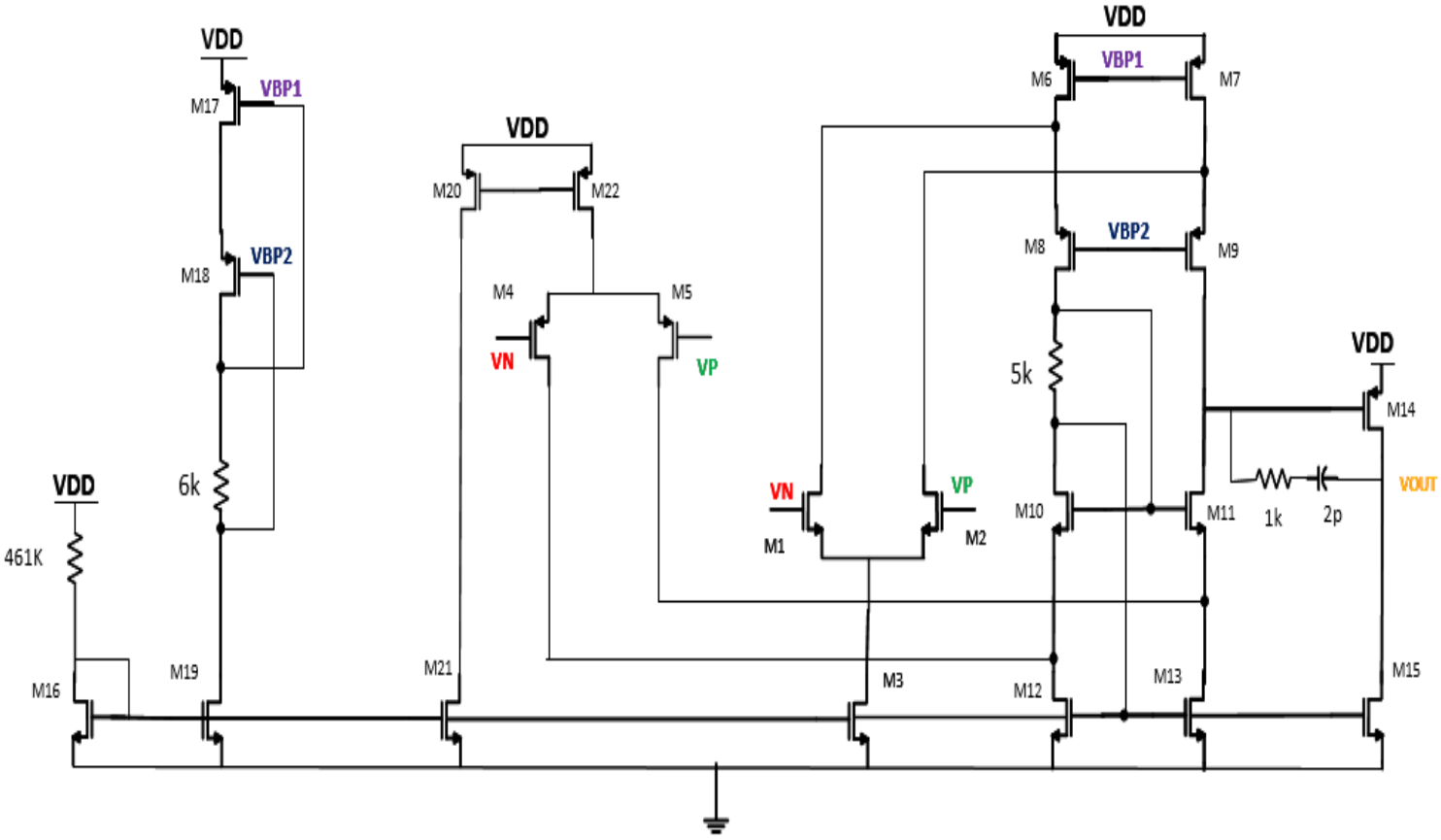


Figure 3-2 Folded cascode OTA with NMOS and PMOS input pair[5]

3.2 Design specifications of OTA:

Important OTA specifications include DC gain, Gain Bandwidth Product (GBW), phase margin (PM), ICMR, Noise, Dynamic range, offset and PSRR.

DC gain:

DC gain of minimum 60 dB is required such that finite gain error ≤ 1 mv.
This work achieves 92dB.

ICMR:

It is the input signal range for which all transistors are in saturation.
Rail to rail ICMR and output ICMR is aimed .Here, 0-3.2V ICMR is achieved

Noise:

The dynamic range of the circuit is limited by noise floor, to get the more dynamic range integrated noise floor should be small. At low frequencies, flicker noise is dominant than thermal noise. To reduce the flicker noise, Wide PMOS input pair is chosen. To reduce the thermal noise, the Gm of the input transistor is increased. DR of system is aimed for 60dB, such that the noise of input transistor is less than 1mV. This work achieves 50dB.

PSRR:

The output of the op-amp is affected by the ripple on the power supply.so, PSRR (power supply Rejection ratio) quantifies this effect. It is defined as the ratio of the Differential gain to the PSR (power supply gain) with the AC ripple on the power supply while the Differential input set to Zero.

$$PSRR = \frac{Av\,(Vdd = 0)}{Avdd\,(Vin = 0)}$$

Here, the transistor M14 is biased by the Current source M15 ,which makes the V_{SG} of M14 to be constant .AC ripple on the power supply forces the gate of the M14 to track the changes ,which in turn gets coupled to the Output by Cc(Compensating Capacitor).
The differential gain is 92 dB and the PSR gain is 1dB, so PSRR=90dB.

Offset:

It is one of the non-ideality of the circuit design that limits the accuracy and the minimal signal that can be processed. It occurs due to the device mismatch between the identical transistors owing to the physical processes during the device fabrication. By using large device sizes, the mismatch can be reduced.
This work aimed for offset ≤ 3.3 mV and achieved 1.71 mV.

3.3 Simulation results and discussions:

To verify and validate the performance of the proposed circuit across all process corners and temperature variations, simulation results have been mentioned below.
OTA is simulated with Maximum Load capacitance to verify the phase margin and the GBW.

3.3.1 Differential operation:

Figure 3-3 differential gain and phase margin at a load of 2pF. It shows that
OTA is highly stable with required GBW for a differential operation over wide range.

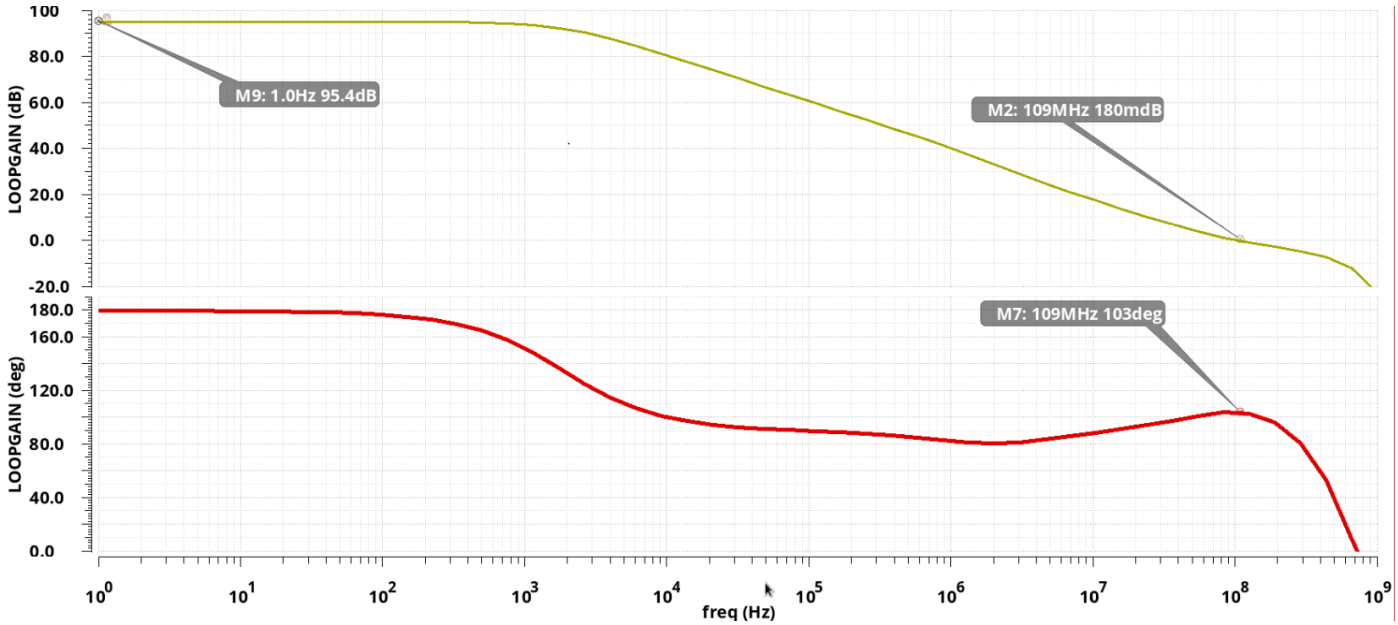
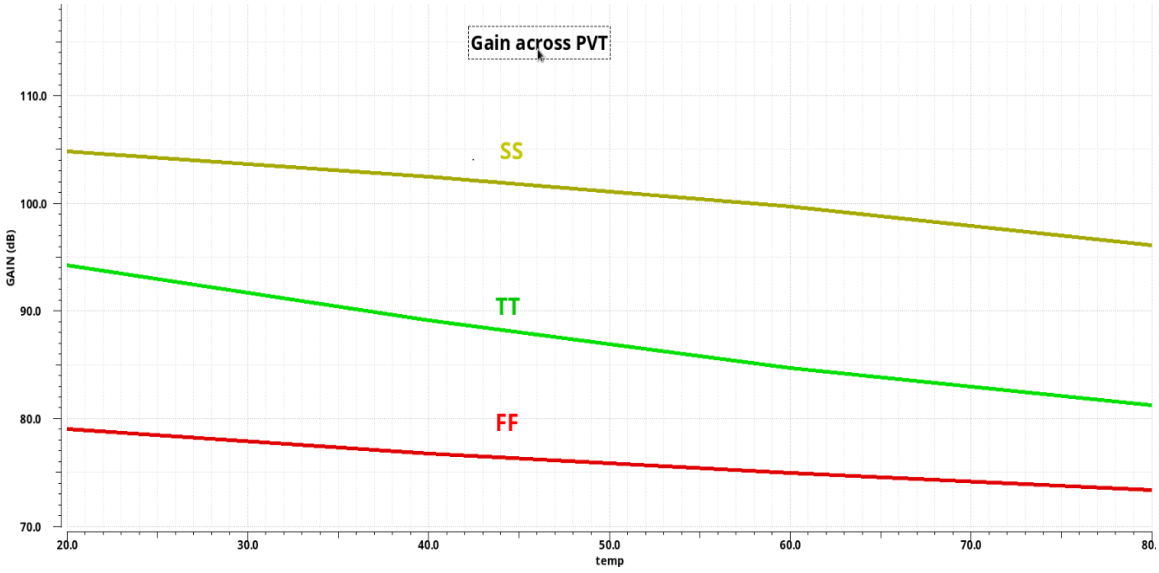


Figure 3-3 Gain and phase margin plot

3.3.2 OTA Gain and phase margin across PVT variations:

It can be seen from the below graph that the OTA Gain and PM doesn't vary much and are well defined within the acceptable range across PVT.



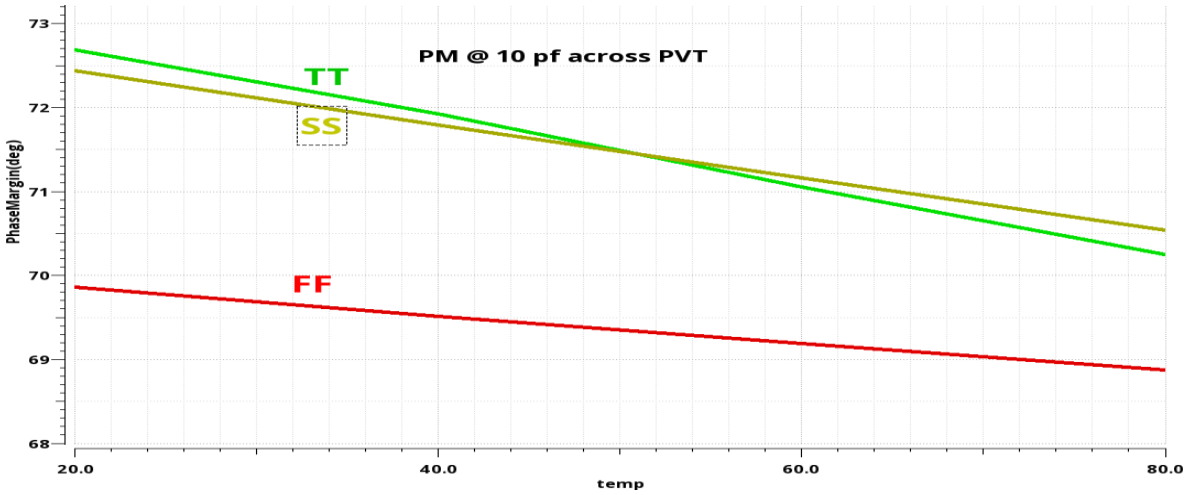


Figure 3-4 Gain and phase margin variation across PVT

	Minimum	Typical	Maximum
Gain(dB)	78	95	105
Phase Margin(deg)	69	71	73

Table 3-1 Gain and PM values across PVT

3.3.3 GBW at 10 pF load across PVT variation:

Figure 3-5 shows that the GBW is within the acceptable range across the PVT variations.

	Minimum	typical	maximum
GBW(MHz)	65	105	115

Table 3-2 GBW values across PVT

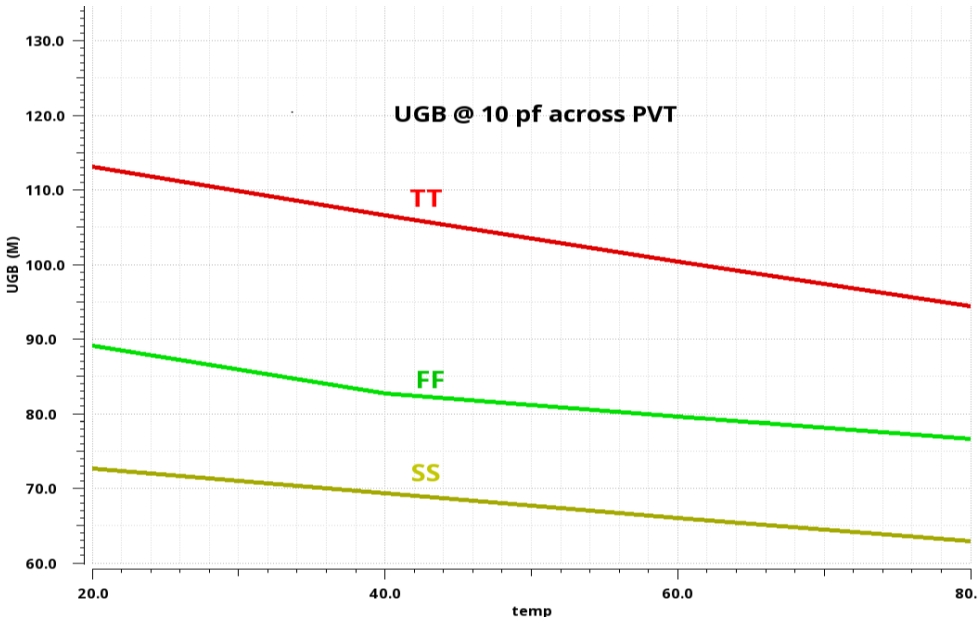


Figure 3-5 UGB @ 10 pf across PVT

3.3.4 ICMR plot:

Figure 3-6 shows the ICMR plot. The design aimed for rail –rail ICMR (0-3.3V) and achieved (0-3.2V).

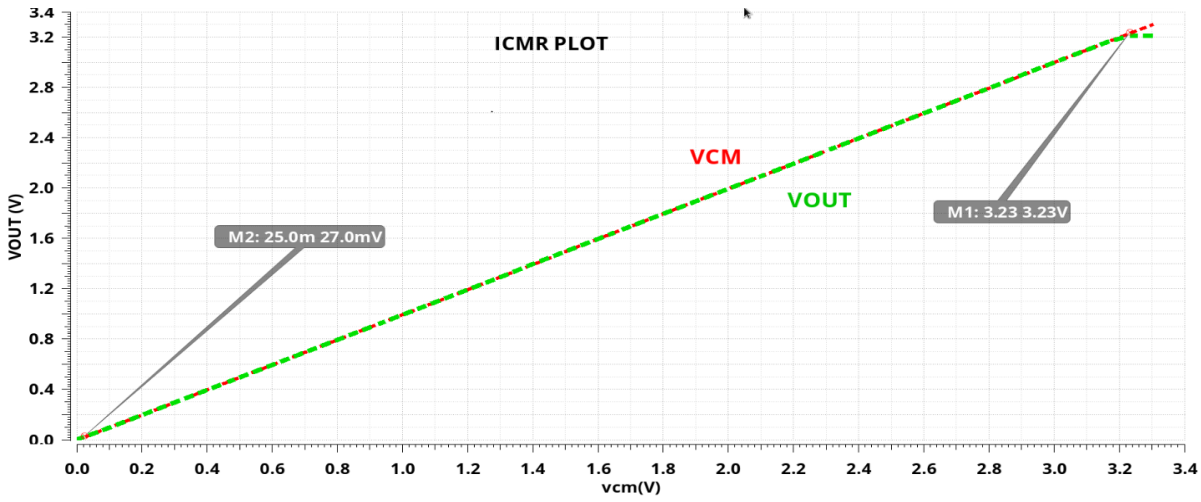


Figure 3-6 ICMR plot

3.3.5 Offset:

The design aimed for Offset ≤ 3.3mV and from the below Fig. 3-7, it can be observed that offset achieved is 1.7 mV which is quite acceptable for the design implementation.

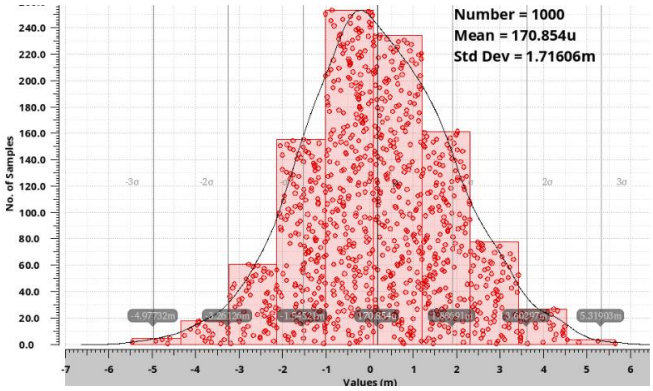


Figure 3-7 Offset (Mismatch variation)

3.3.6 Noise and SFDR plot:

The designed aimed for noise ≤ 3.3 mV and the Dynamic range ≥ 60dB.From the below Fig. 3-8, it can be seen that the total input referred noise is 23 µV and the DR achieved is around 50dB.

Device	Param	Noise Contribution	% Of Total
/I0/M20	fn	0.00582219	37.11
/I0/M18	fn	0.00581866	37.07
/I0/M7	fn	0.0032375	11.48
/I0/M4	fn	0.00323729	11.47
/I0/M8	fn	0.000880137	0.85
/I0/M3	fn	0.000878783	0.85
/I0/M30	fn	0.000595816	0.39
/I0/M32	fn	0.000595802	0.39
/I0/M20	id	0.000253704	0.07
/I0/M18	id	0.000253661	0.07

Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Summarized Noise = 0.00955713
Total Input Referred Noise = 2.30478e-05
The above noise summary info is for noise data

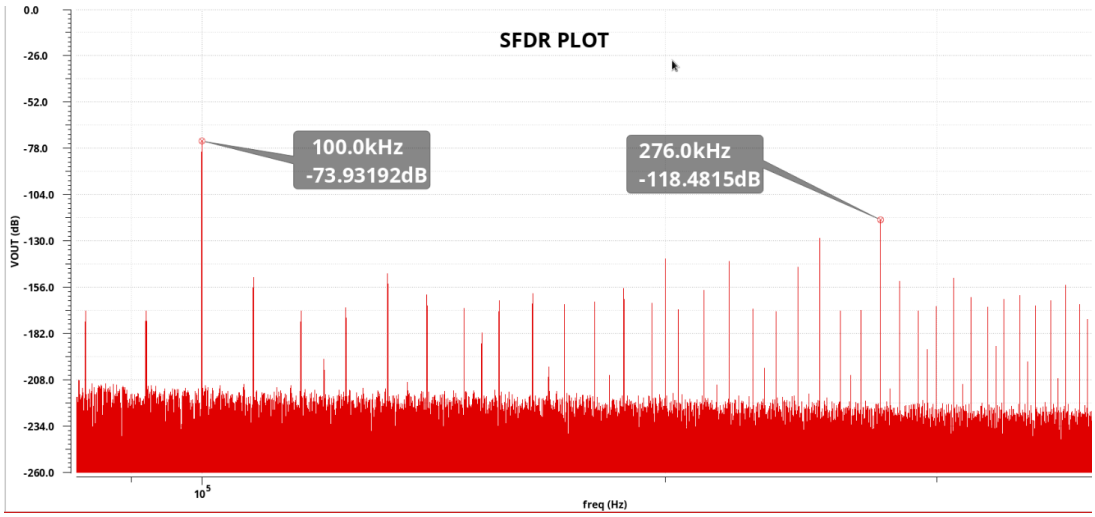


Figure 3-8 Noise and SFDR plot

3.3.7 PSRR:

From the Fig. 3-9, it can be seen that PSR gain is 0 dB and the differential gain achieved is 95 dB .So, the PSRR =differential gain – PSR gain=95-0=95dB.

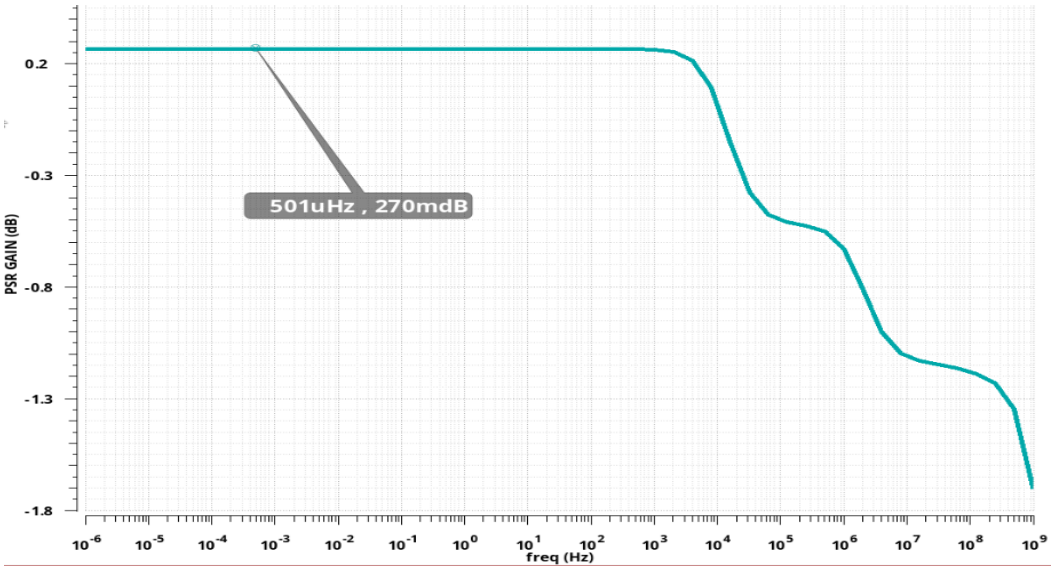


Figure 3-9 PSRR plot

3.3.8 Performance summary:

	Units	Targeted Specs	Achieved Specs
Supply voltage	V	3.3	
Gain	dB	≥60	95
Phase Margin	degrees	≥60	71
GBW	MHz	≥100	105
ICMR	V	0-3.3	0-3.2
Noise	V	≤3.3m	23µ
Dynamic Range	dB	≥60	50
PSRR		≥60	95
offset	millivolt	≤3.3	1.71
Power consumption	milliwatt	≤15	10

3.4 Simulation results of the impedance readout circuit:

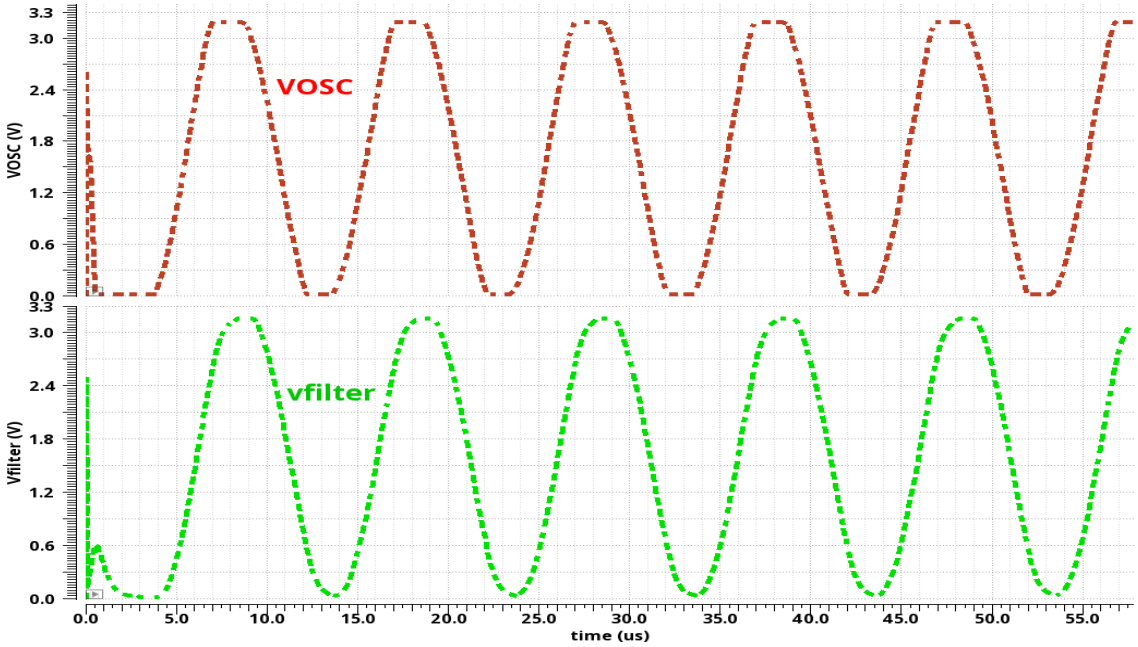


Figure 3-10 Transient simulation of oscillator and filter

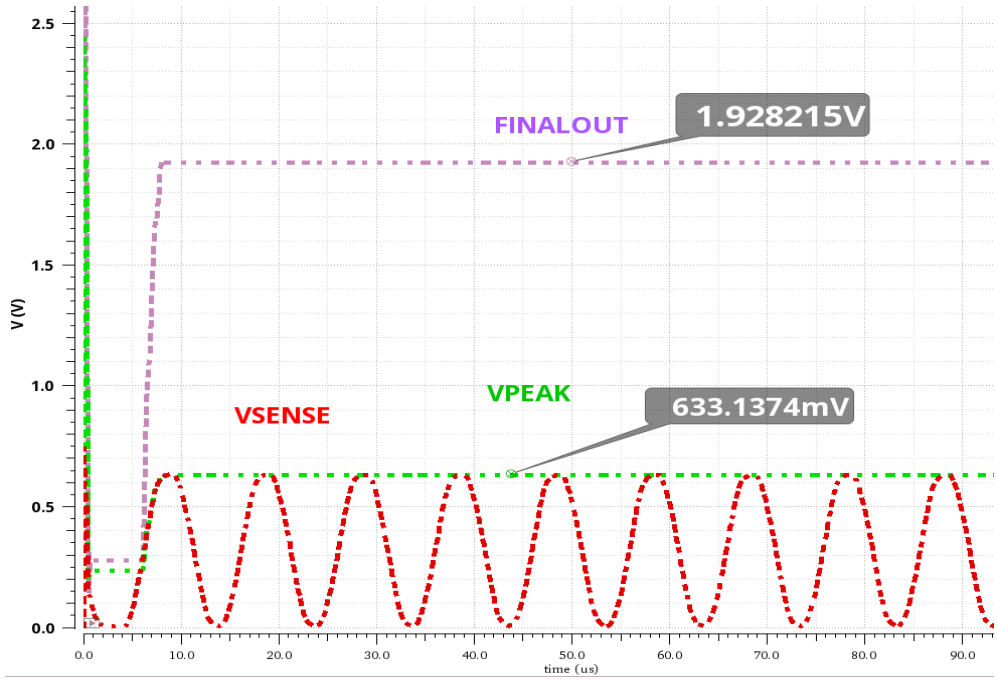


Figure 3-11 Transient response of V-I convertor, peak detector and the final output for a load of 395 Ω

Load(Ω)	Ideal Output(V)	Achieved Output(V)
395	1.9291	1.9282

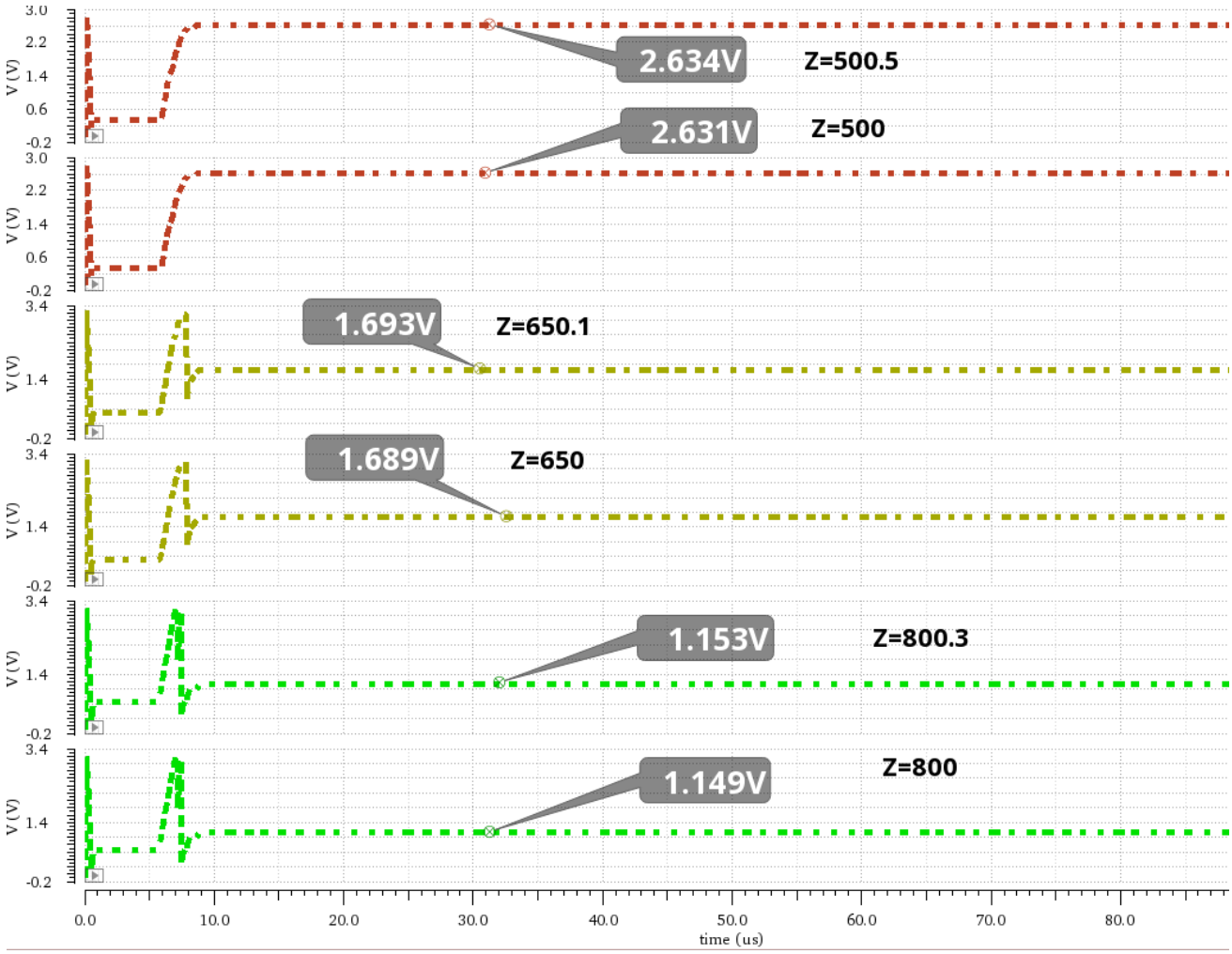


Figure 3-12 Simulation results of the impedance in subranges with the targeted resolutions

Impedance (Ω)	Final Output(V)
250	0.9968
250.5	0.9995
400	1.9529
400.5	1.9554
550	2.9543
550.5	2.9574
630	1.0325
630.1	1.0367
680	2.6706
680.1	2.6739
750	0.567
750.3	0.571
800	1.149
800.3	1.153
930	2.636
930.3	2.640

Table 3-3 Final output of the impedance in 3 subranges with the desired resolutions, corresponding to a change of 3.3 millivolt.

3.5 Output of the PCB board integrated with the cell phone and Arduino UNO

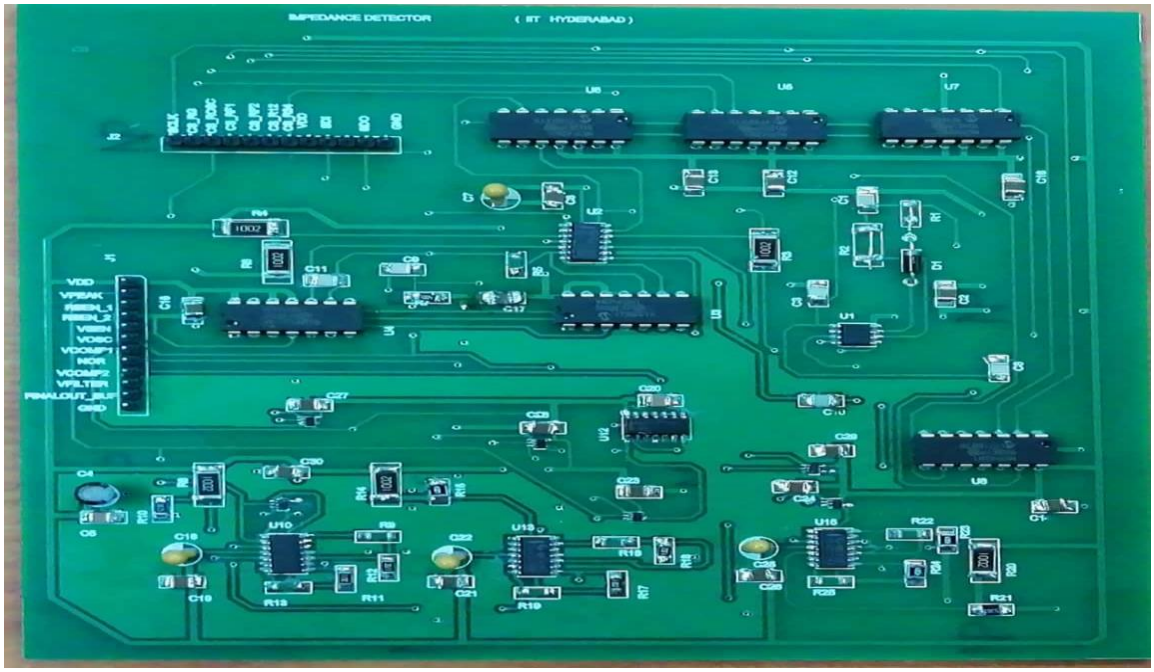


Figure 3-13 PCB board for impedance readout circuit

Figure 3-14 The board interfaced with cell phone and Arduino Uno

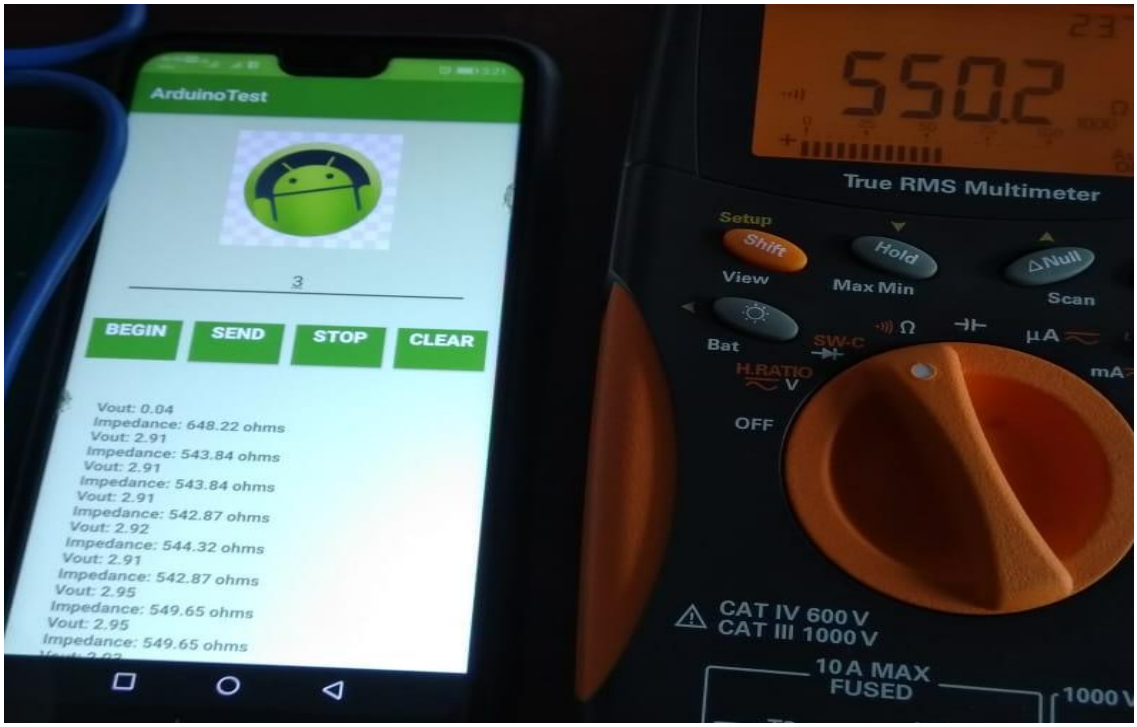


Figure 3-15 For a load of 550Ω, 549Ω displays on cell phone

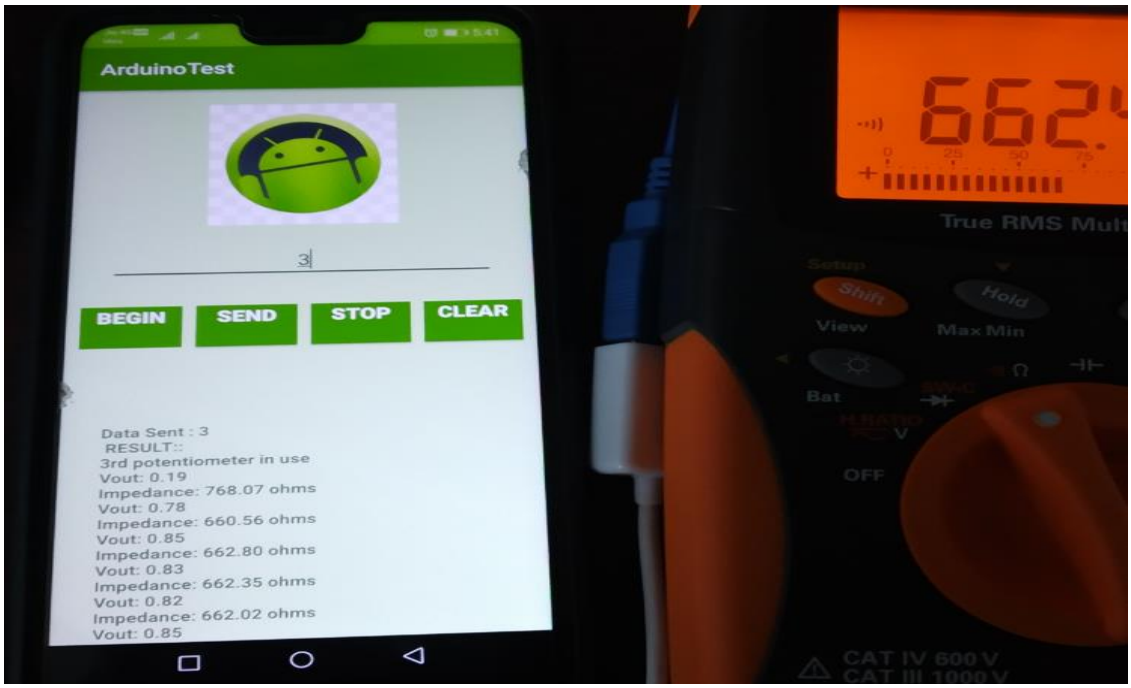


Figure 3-16 For a load of 662 Ω, 660Ω displays on cell phone

Figure 3-17 For a load of 807Ω, 800Ω displays on cell phone

Chapter 4

4 Design and Implementation of wide Range Resistive Readout circuit

4.1 Introduction:

Many resistive based gas, chemical and pressure sensors exhibit a wide range performance. So, the proposed design uses a subrange detector based on comparators to cover an input resistance ranging from 10kΩ to 1GΩ .Here, the resistance(R_{IN}) is first converted to a voltage , by fixed current source and then measured by an ADC . However, accommodating a high R_{IN} range results in one of two issues: the ADC input voltage will saturate at high R_{IN} or an extremely high resolution ADC is required to sense low R_{IN} that produce very small voltages. So, a common approach is to divide the R_{IN} range into Sub-ranges and apply different currents for each sub-range using a current DAC. This technique greatly increases accuracy across the total R_{IN} range. After the correct sub-range is found for a particular sub range, the corresponding current is selected and V_{IN} is generated from the resulting IR drop. [1]

4.2 Circuit design:

First, a 1.5nA initial current is applied to the unknown R_{IN}. This initial current is chosen to map the entire R_{IN} range (10kΩ−1GΩ) to the comparator operating range. This 1.5n× R_{IN} drop is compared to 3 threshold values(1.5m,150m,1500mV) to determine 2 fine sub-ranges(10M-100M ,100M-1G) and 1 one coarse sub range(10k-10M). According to the coarse sub-range, a second current (150n A) is activated resulting in a 150n× R_{IN} spanning 1.5-1500mV. The same procedure repeats to divide coarse sub-range into 3 fine sub-

ranges(10k-100k,100k-1M,1M-10M), yielding total 5 sub-ranges. Here, an edge-triggered D flip-flops are used to avoid unnecessary switching of the comparators and the current sources during the activation of the second initial current.

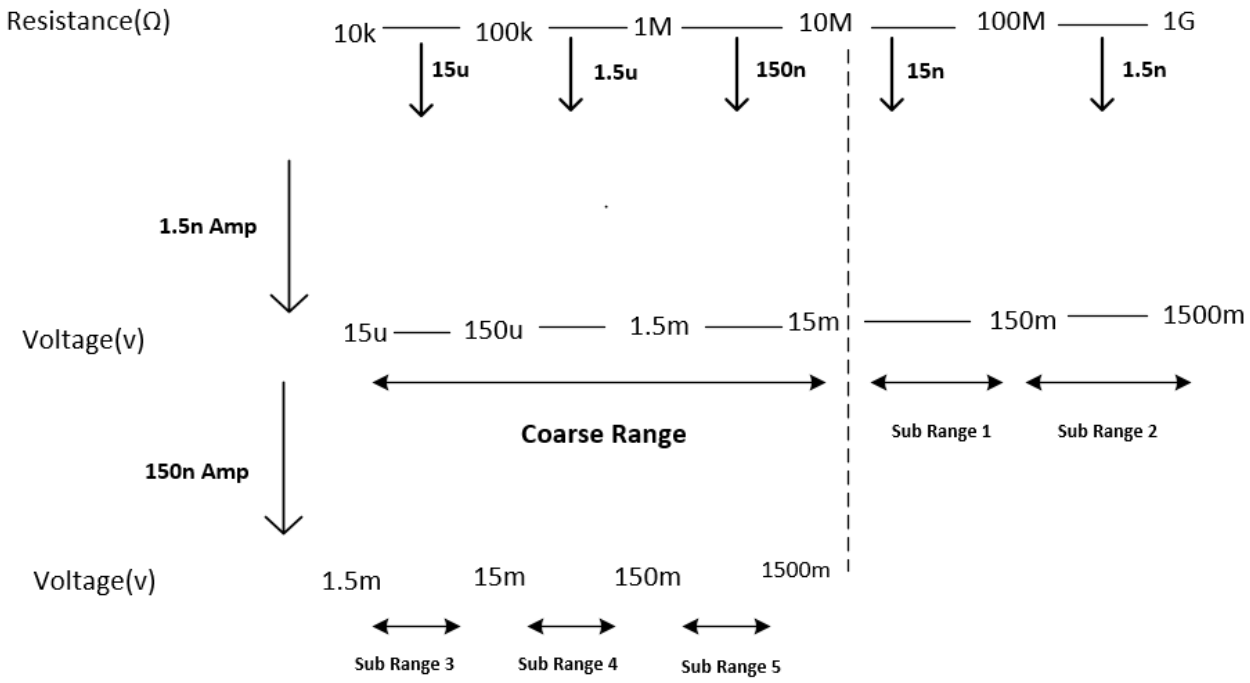


Figure 4-1 Mathematical representation

4.3 Circuit implementation:

Circuit design for wide range resistive readout circuit involves designing of OTA with 1.8V supply, D flip-flop and logic gates .These are analyzed and designed in TSMC 0.18 µm CMOS technology. Here, the voltage drop I^*R_{IN} is biased with Vcm voltage such that the comparator is always in the maximum gain region for better resolution.

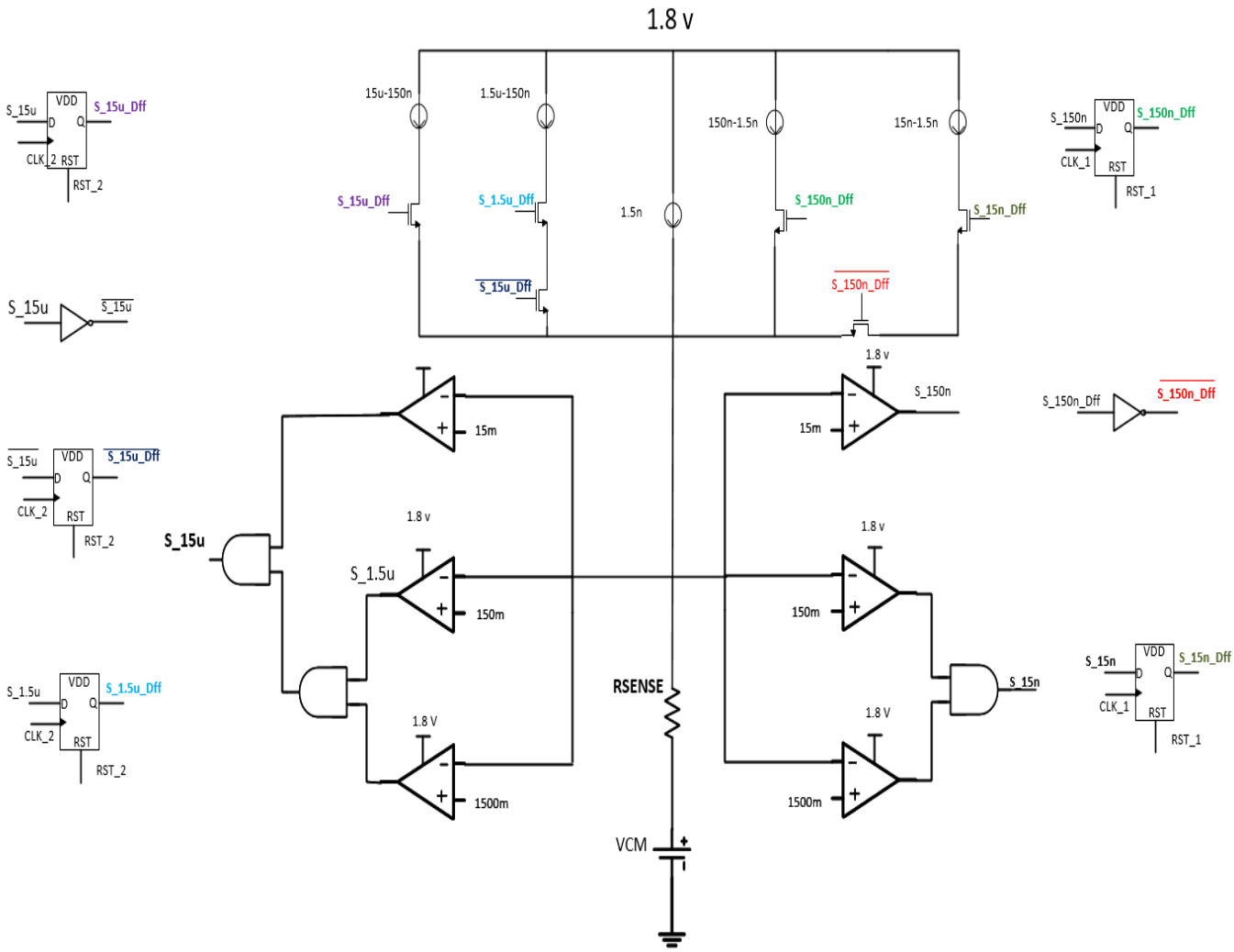


Figure 4-2 Wide range resistive readout circuit

D FILP_FLOP LEVEL TRIGGERED

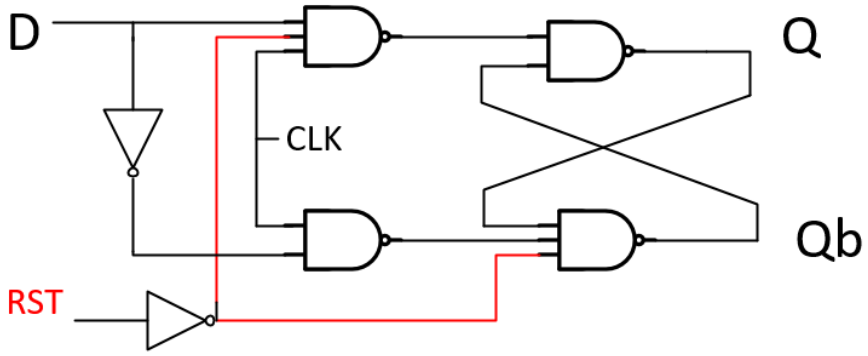


Figure 4-3 Level-triggered D flip-flop

DFF +VE EDGE TRIGGERED

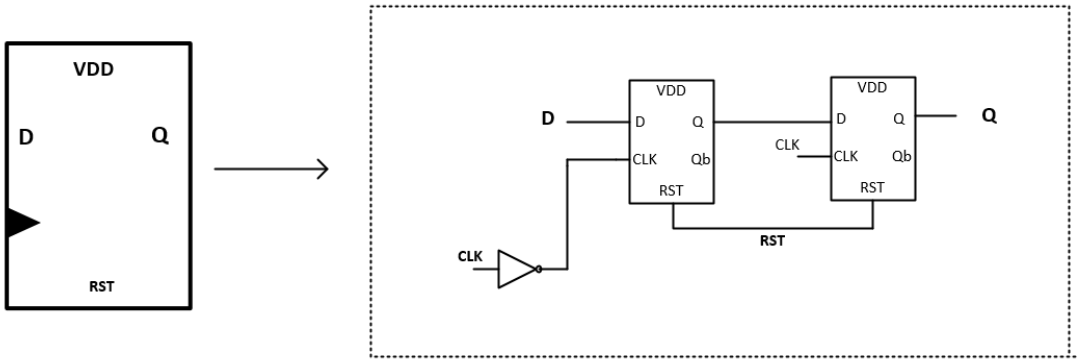


Figure 4-4 Edge-triggered D flip-flop

4.4 OTA with 1.8 V supply:

4.4.1 Architecture of two stage OTA:

The present work requires an op-amp which has high gain, low noise and high UGB. To meet these requirements, Folded cascode configuration is chosen with NMOS and PMOS input pair.

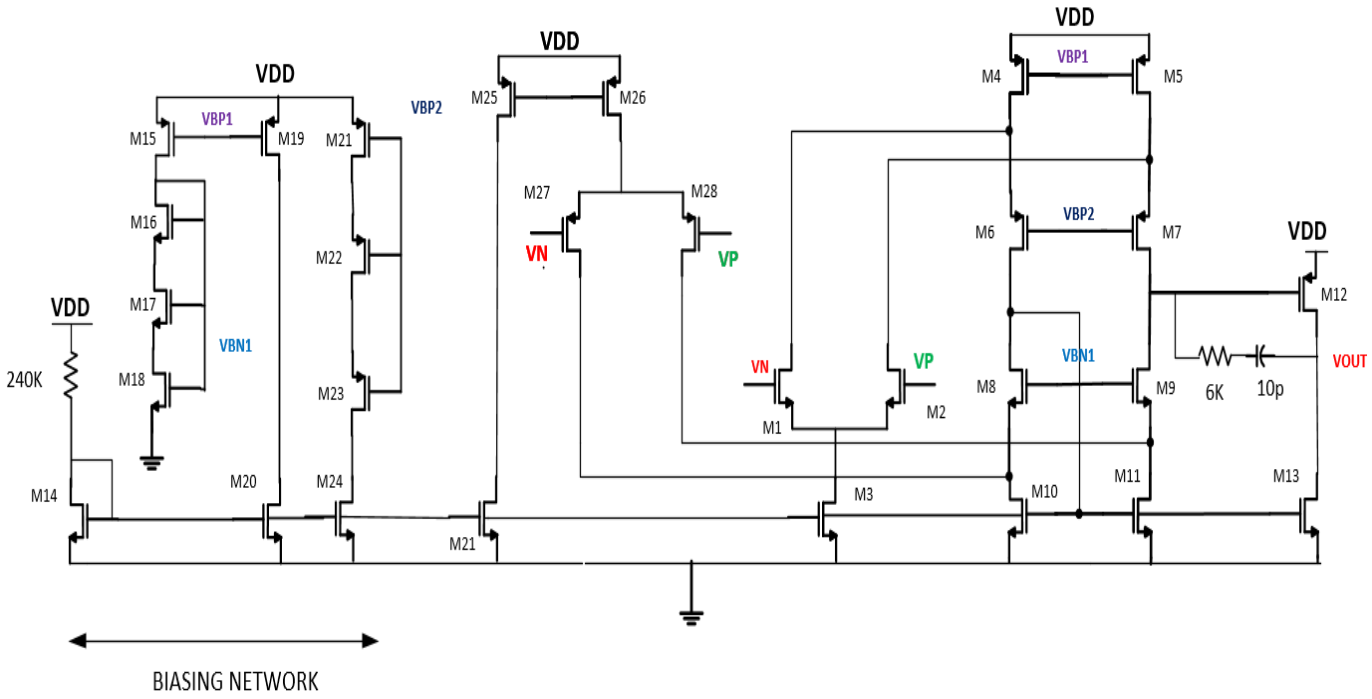


Figure 4-5 Folded cascode OTA[5]

4.5 Simulation results of OTA:

To verify and validate the performance of the proposed circuit across all process corners and temperature variations, simulation results have been mentioned below. OTA is simulated with maximum load capacitance to verify the phase margin and the GBW.

4.5.1 Differential operation:

Figure 4-6 shows differential gain and phase margin plot. It can be seen that OTA is highly stable with required GBW for a differential operation over wide range.

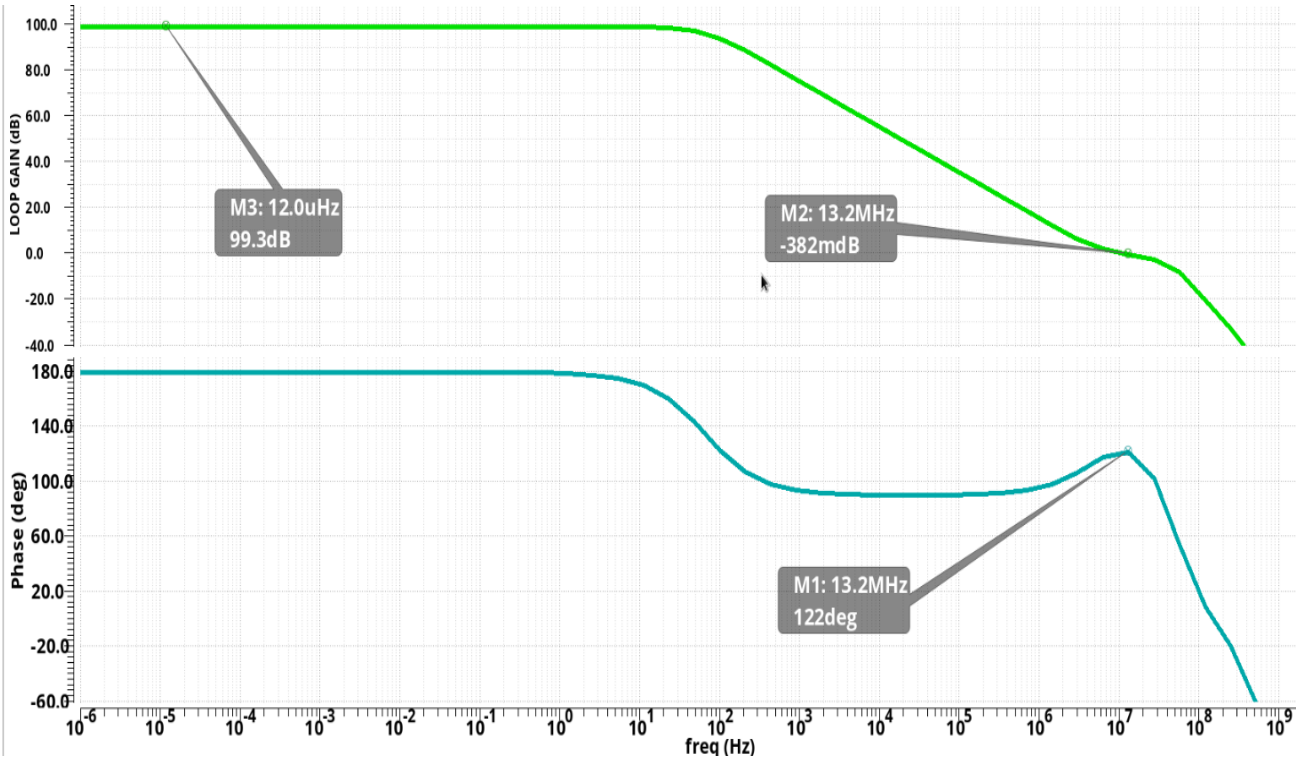


Figure 4-6 Gain and phase margin plot

4.5.2 OTA Gain and phase margin across PVT variations:

It can be seen from the below graph that the OTA Gain and PM doesn't vary much and are well defined within the acceptable range across PVT.

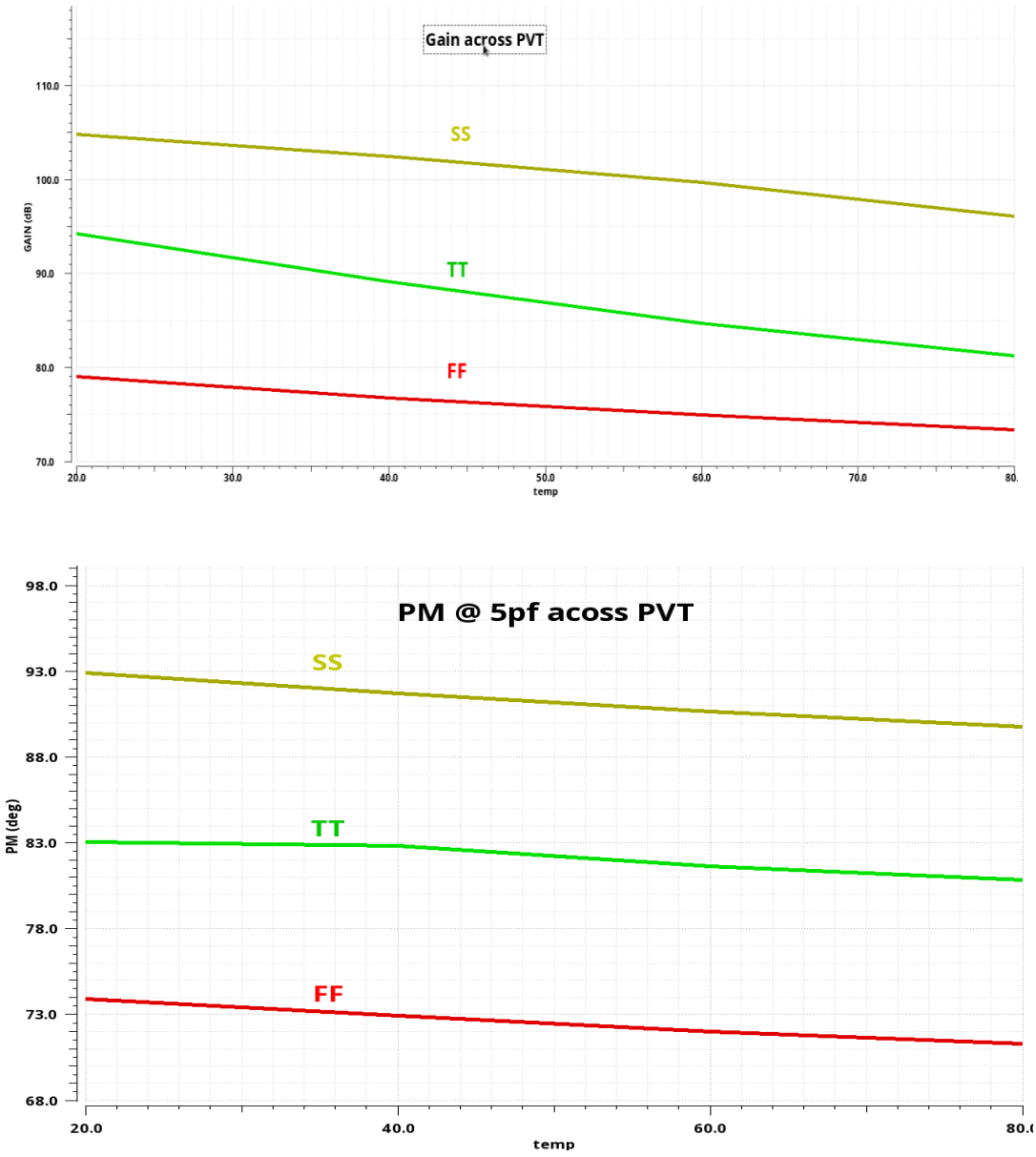


Figure 4-7 Gain and phase margin plot @ 5 pF

	Minimum	Typical	Maximum
Gain(dB)	80	99	105
Phase margin (deg)	73	83	93

Table 4-1 Gain and PM values across PVT

4.5.3 GBW at 5 pF load across PVT variation:

Figure 4-8 shows that the GBW is within the acceptable range across the PVT variations.

	Minimum	typical	maximum
GBW(MHz)	4	11	12

Table 4-2 GBW across PVT

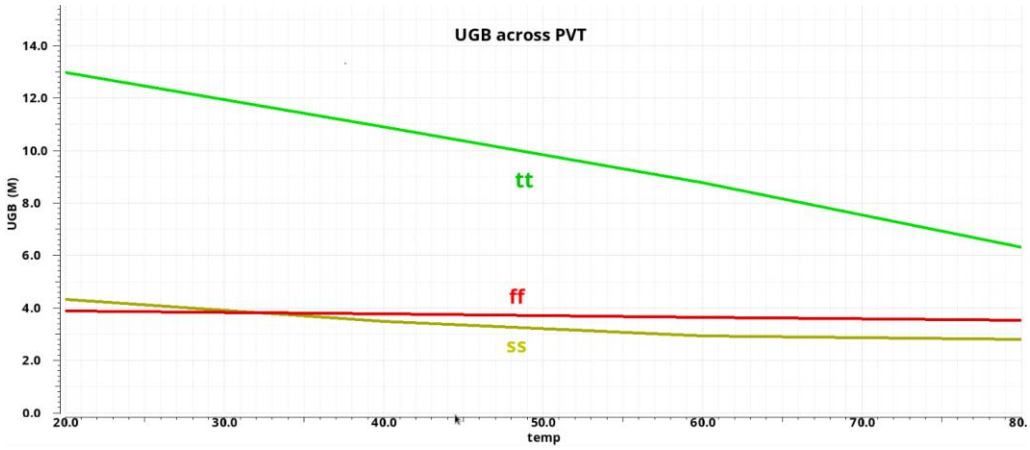


Figure 4-8 UGB @ 5 pf across PVT

4.5.4 ICMR plot:

Figure 4-9 shows the ICMR plot. The design aimed for ICMR (0-1.5V) and achieved (0.01-1.5 V).

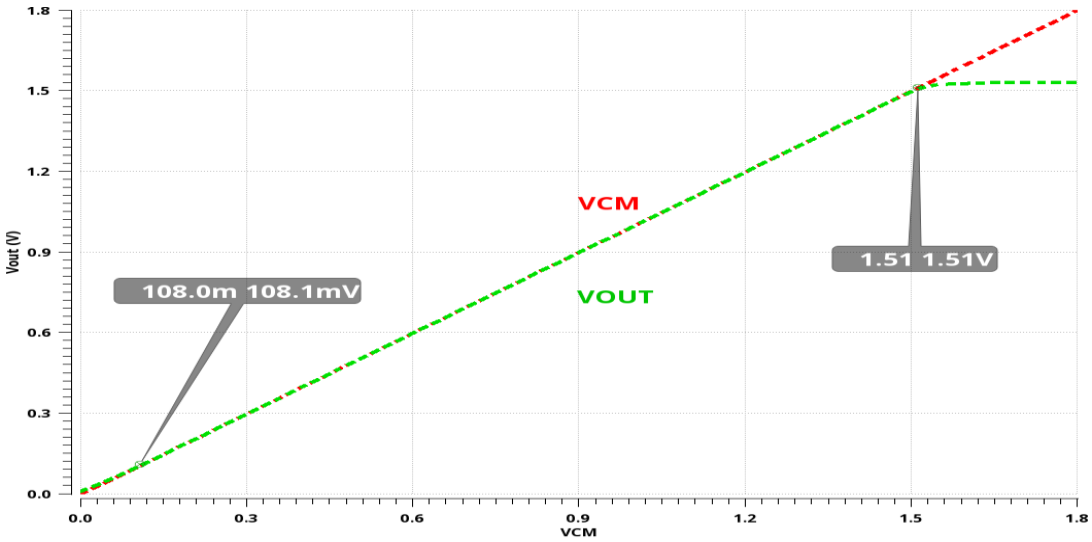


Figure 4-9 ICMR plot

4.5.5 Offset:

The design aimed for Offset ≤ 1.8mV and from the below Fig. 4-10, it can be observed that offset achieved is 0.8 mV which is quite acceptable for the design implementation.

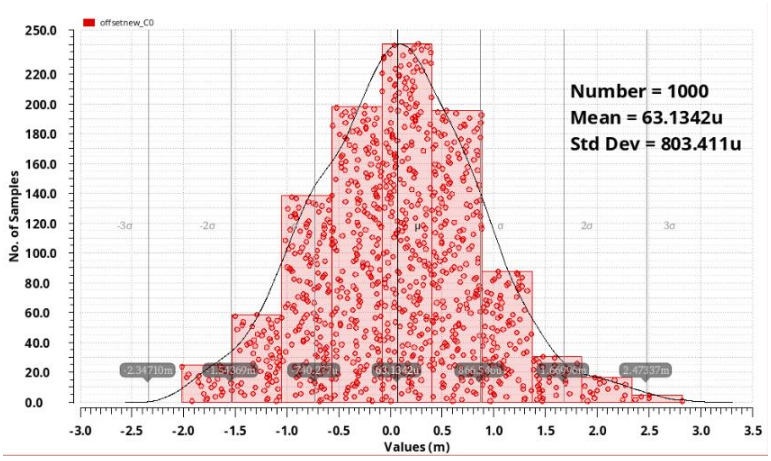


Figure 4-10 Offset (Mismatch variation)

4.5.6 Noise and SFDR plot:

The design aimed for noise ≤ 1.5 mV and the Dynamic range ≥ 60dB.From the below figure, it can be seen that the total input referred noise is 14 µV and the DR achieved is around 120dB.

Device	Param	Noise Contribution	% Of Total
/I0/M8	fn	0.0148697	28.21
/I0/M9	fn	0.0148696	28.21
/I0/M5	fn	0.011883	18.01
/I0/M6	fn	0.0118811	18.01
/I0/M20	fn	0.00443701	2.51
/I0/M19	fn	0.00443633	2.51
/I0/M20	id	0.00209575	0.56
/I0/M19	id	0.00209543	0.56
/I0/M5	id	0.00197612	0.50
/I0/M6	id	0.00197581	0.50
/I0/M8	id	0.00123462	0.19
/I0/M9	id	0.00123461	0.19
/I0/M11	fn	0.000354384	0.02
/I0/M10	fn	0.000354329	0.02
/I0/M20	rs	0.000132256	0.00
/I0/M19	rs	0.000132235	0.00
/I0/M5	rs	8.89221e-05	0.00
/I0/M6	rs	8.89083e-05	0.00
/I0/M8	rs	8.52241e-05	0.00
/I0/M9	rs	8.52235e-05	0.00

Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Summarized Noise = 0.0279985
Total Input Referred Noise = 1.4492e-05
The above noise summary info is for noise data

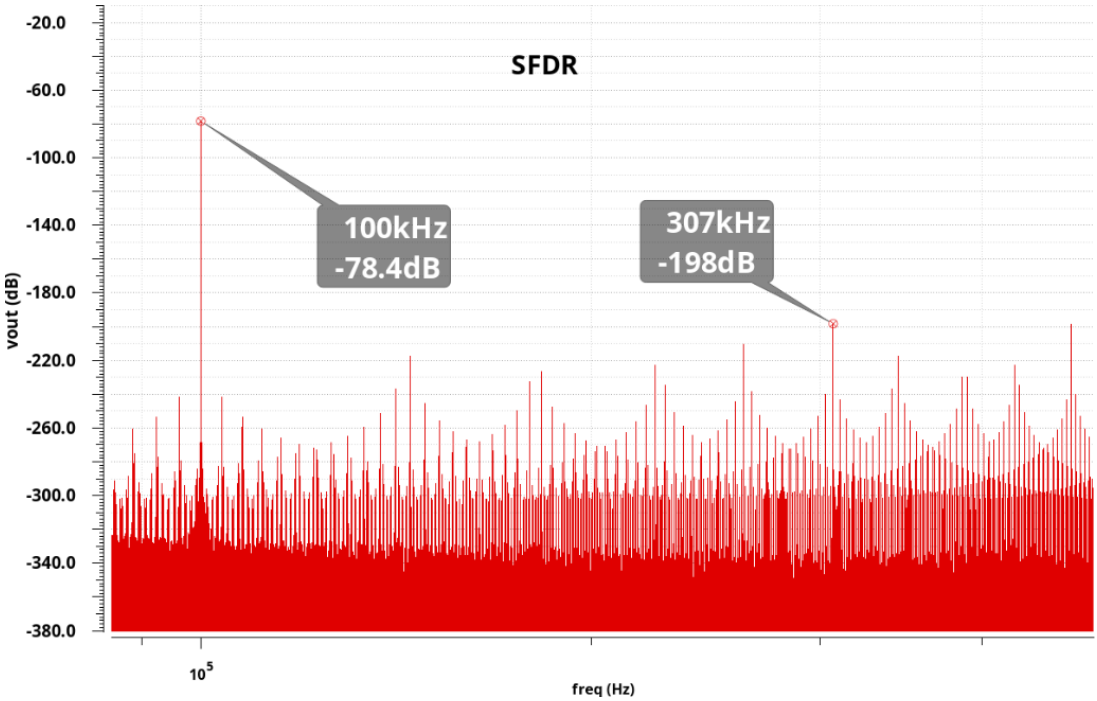
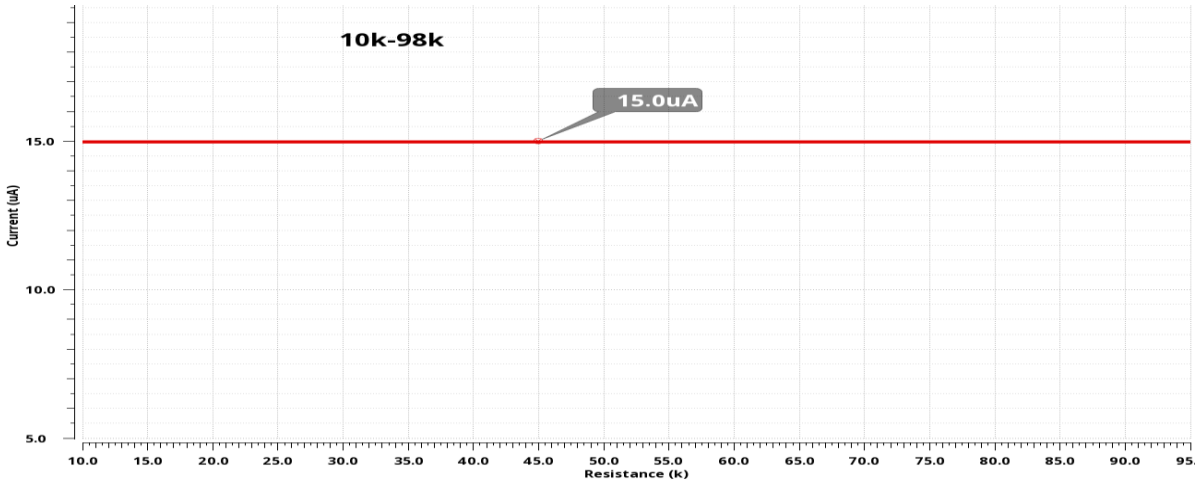


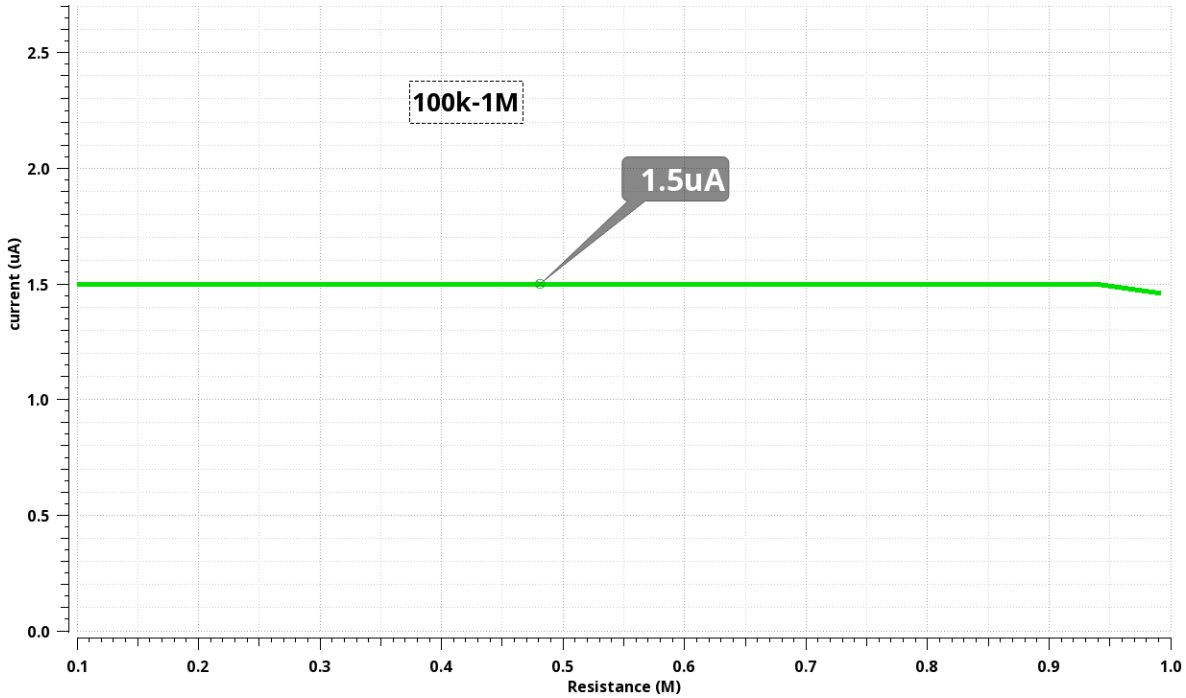
Figure 4-11 Noise and SFDR plot

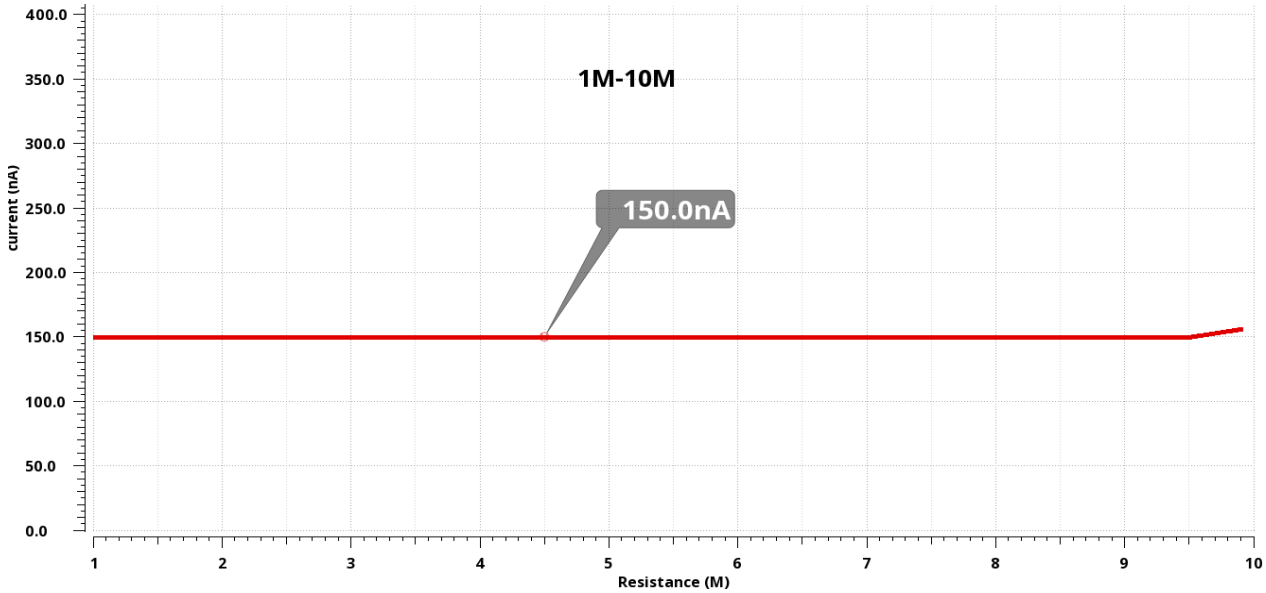
4.5.7 Performance summary:

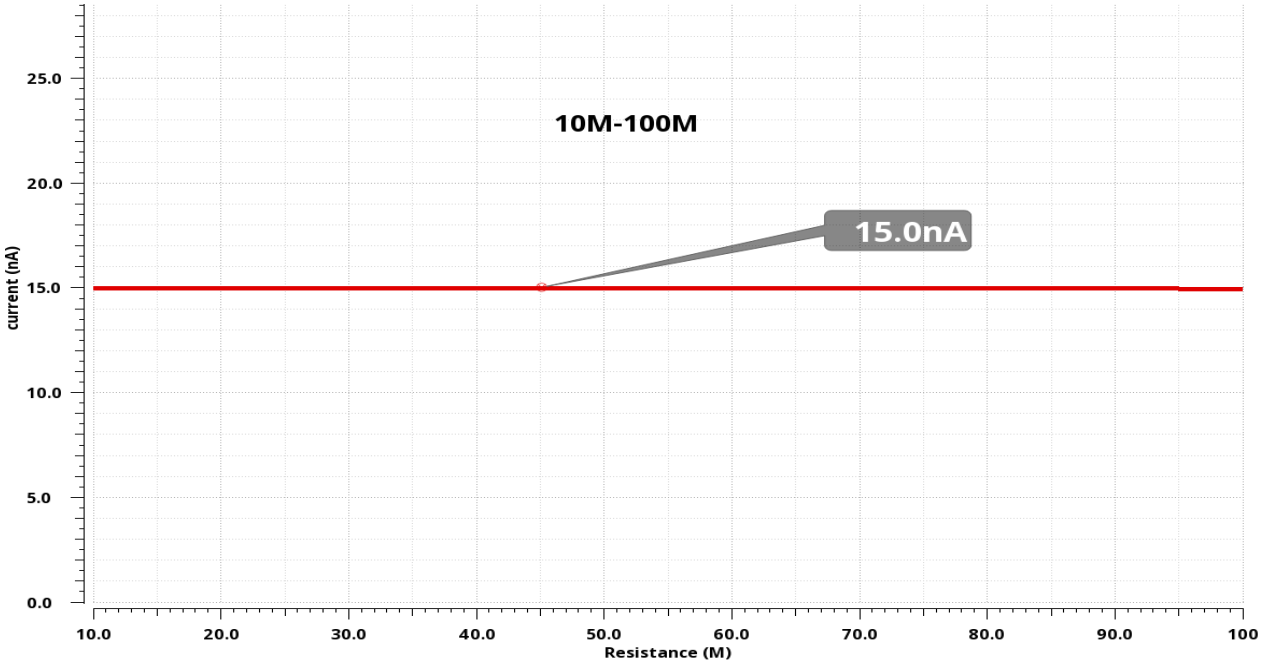
	Units	Targeted Specs	Achieved Specs
Supply voltage	V	1.8	
Gain	dB	≥60	100
Phase Margin	degrees	≥60	83
GBW	MHz	≥10	11
ICMR	V	0-1.5	0.01-1.5
Noise	V	≤1.8mv	14µ
Dynamic Range	dB	≥60	100
PSRR		≥60	70
offset	millivolt	≤1.8	0.8
Power consumption	µ watts	≤800	720

4.6 Simulation results of wide range readout circuit:






1M-10M
150.0nA
current (nA)
400.0
350.0
300.0
250.0
200.0
150.0
100.0
50.0
0.0
1
2
3
4
5
6
7
8
9
10
Resistance (M)


10M-100M
15.0nA
current (nA)
25.0
20.0
15.0
10.0
5.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100
Resistance (M)

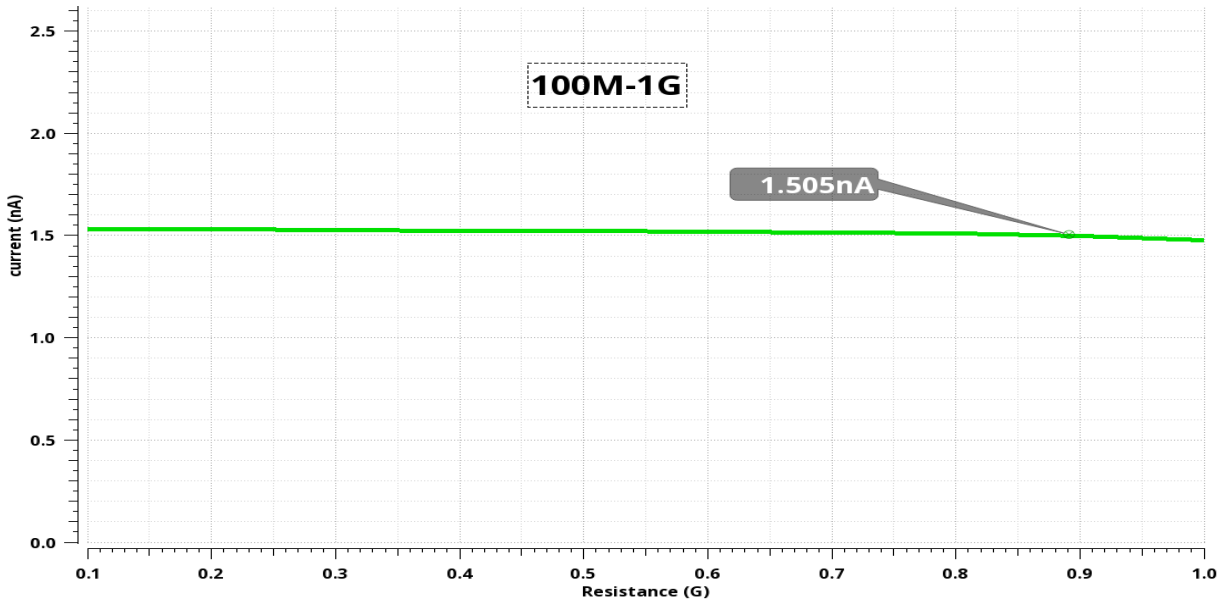


Figure 4-12 Current vs resistance plots showing targeted currents in each corresponding resistance sub ranges.

Chapter 5

5 Conclusion:

Impedance readout circuit for the Milk Adulteration and the Wide range resistive detector is designed and verified across all process corners and temperatures varying from 20°C to 80°C.Interfacing the cell phone with the PCB board and Arduino Uno is also shown.

5.1 Future work:

For the Wide range resistive detector, the currents are realized with ideal current sources.so, replacing the ideal current sources with BGR current reference circuit can be done.

5.2 References:

[1] Choi, M., et al. Wide input range 1.7 μW 1.2 kS/s resistive sensor interface circuit with 1 cycle/sample logarithmic sub-ranging. in 2015 Symposium on VLSI Circuits (VLSI Circuits). 2015. IEEE.

[2]https://nptel.ac.in/courses/Webcourse-contents/IIT-ROORKEE/Analog%20circuits/lecturers/lecture_24/lecture24_page2.htm.

[3] Roy, D.C., Linear integrated circuits. 2003: New Age International.

[4] https://developer.android.com/studio/intro.

[5] Allen, P.E. and D.R. Holberg, CMOS analog circuit design. 1987: Oxford university press.