Solar Energy Based Self-Sustainable Power Management System

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Dedication

My Family

Abstract

Frequent battery replacement is a big challenge faced in Wireless Sensor Nodes (WSNs) operating in remote places due to high maintenance cost and inaccessibility. The solution for this is harvesting energy from various sources like solar, wind, thermal, vibration. Solar energy harvesting is the best option among them because of its abundant availability.

The battery gets charged through solar energy during daylight and when solar energy is not available, the system gets power up through the charge stored in the battery.

The Maximum Power Point (MPP) of the solar cell is tracked by comparing the MPP voltage with respect to the input solar cell voltage. The reference MPP voltage is generated by sampling 0.7 times the open circuit voltage (V_{OC}) of solar cell periodically in a capacitor (C_{MPP}).

A self sustainable high power battery management system is developed where the system works in two modes, the first one is the main converter mode and the second is the startup mode. startup mode is used when the battery is almost drained. None of the other control circuitry function in this mode. Cold start circuit only goal is to charge output capacitance until it crosses the threshold voltage required to power the entire system. Power On Reset (POR) circuit decides between startup mode and main converter mode.

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Chapter 1

Introduction

Wireless Sensor Nodes (WSNs) are used everywhere due to advancements in technology. WSNs consist a transceiver for transmission or reception of control and data and a processing unit for data acquisition consisting of signal conditioning circuits and ADCs, DACs, etc., These WSNs are supposed to have a long life. Most of them are operated in remote places and it is difficult to access the system and replace the battery frequently.

1.1 Energy Harvesting

Even though the batteries have a good energy density, in many cases, they will show a large impact in terms of size, operational price, and life cycle. To cope up this situation alternative solutions to batteries are being investigated. They are

- Replacing the batteries with energy storage systems having larger energy density, e.g., miniaturized fuel cells.
- Providing the energy necessary to the device in a wireless mode,but it requires dedicated transmission infrastructures. e.g., RFID tag
- Harvesting the energy from ambient energy sources like solar, thermal, vibration, RF, wind...

Wind energy harvesting will not be of much use for micro and nano level systems due to the area and power constraints. RF and Vibration systems are inherently ac systems which require rectification and regulation circuits to power the load at a constant DC level.Even in the case of TEG (Thermo Electric Generator) which generates direct DC power, the power extracted is very low. Moreover,

Table 1.1: Characteristics of various energy sources available in the ambient and harvested power of [1].

Source	Source power	Harvested power
Ambient light		
Indoor	0.1 mW/cm^2	10 μW/cm^2
Outdoor	100 mW/cm^2	10 mW/cm^2
Vibration/motion		
Human	0.5 m @ 1 Hz - 1 m/s^2 @ 50 Hz	4 μW/cm^2
Industrial	1 m @ 5 Hz - 10 m/s^2 @ 1 kHz	100 μW/cm^2
Thermal energy		
Human	20 mW/cm^2	30 μW/cm^2
Industrial	100 mW/cm^2	1-10 mW/cm^2
RF		
Cell phone	0.3 μW/cm^2	0.1 μW/cm^2

the power that can be extracted from them is very minimal compared with solar energy harvesting systems. The above Table 1.1 clarifies and provides a clear picture of different energy harvesting techniques and the power levels.

1.1.1 Solar Energy Harvesting

Solar energy harvesting is the most preferred technique in outdoor deployments due to its relatively high power density. Despite being available in most of the periods, solar energy scavenging is done in both micro and macroscale. Micro-scale solar energy harvesting is done for applications like battery charging, driving low power loads, powering wireless sensor networks whose average power consumption is low. Macroscale energy extraction from solar power is used in solar powered inverters, solar water heaters, solar smart inverters, etc.

Micro-scale solar energy harvesting has many advantages right from the fact that solar cells being made with silicon until the abundant availability. Hence reliability is ensured undoubtedly. However, solar energy harvesting faces many challenges due to area constraints even though solar panels size has been reduced to a good extent. Other major challenges in these systems are the design of the start-up circuit and MPPT technique to extract maximum power from the solar cell.

The heart of any solar energy harvesting system is the step-up DC-DC converter, which is needed to charge the battery with the boosted voltage from the low voltages obtained from the tiny solar cell. To a broader level, micro-scale solar energy harvesting systems are classified into two major categories concerning for the energizing element used namely the inductor and capacitor. Converter

systems are categorized into inductor-based and inductor-less systems, latter being more compatible for SoC (on-chip) and the former one, though cannot be fabricated is preferred due to its higher efficiency and relatively higher power extraction. Due to very low power availability at the source side, efficiency is the major concern in micro-scale energy harvesting systems.

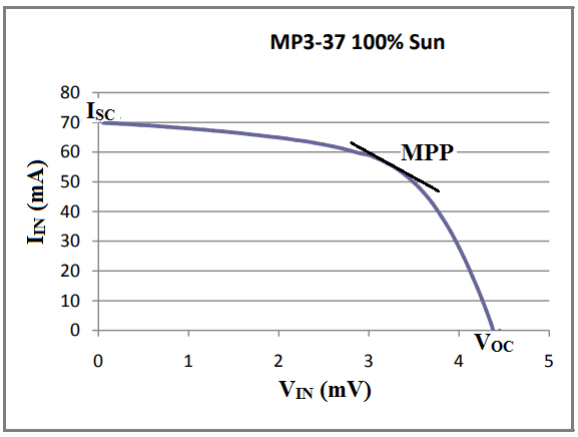

Figure 1.1: Current-Voltage characteristics of solar cell MP3-37 at 100% solar irradiation of [3].

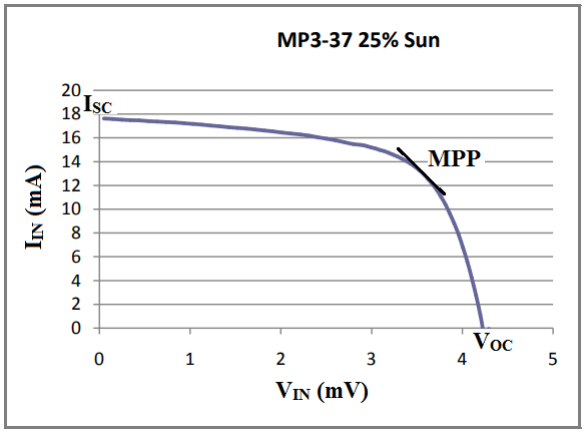

Figure 1.2: Current-Voltage characteristics of solar cell MP3-37 at 25% solar irradiation of [3].

As earlier mentioned, the energy available is relatively scarce and it is mandatory to utilize it to the maximum extent possible. The basic underlying criteria for maximum power extraction is that the impedance of the source (solar cell) should match with the impedance of the harvester circuit incorporated to extract the maximum power out of it. Solar Input power varies widely with the solar irradiation as shown in Figures 1.1, 1.2. Overwhelming research has been done in this field which makes the system operate at a point most often called maximum power point (MPP) of the solar cell. The power extracted at that point of operation is always the maximum possible power that can be extracted from that solar cell for the particular irradiation at that particular temperature.

Henceforth technique for extracting maximum power is mentioned as MPPT (Maximum Power Point Tracking) and the various prevalent techniques used for the same are discussed.

Many MPPT techniques have been developed in the last years. The following are some of them :

- The hill-climbing method directly computes the MPP by measuring the gradient of the output power in the dependence of the output voltage.
- Perturb and observe continuously disturbs the system to detect the MPP, and the operating voltage of the panel oscillates around it.
- The incremental conductance method is based on the fact that the slope of the power curve of solar cell is zero at the MPP, positive on the left of the MPP, and negative on the right. A micro-controller periodically checks and tunes the current operating point, resulting usually in good accuracy and efficiency.
- The fractional open-circuit voltage (FOCV) technique exploits the existing nearly linear relationship between MPP voltage (V_{MPP}) and the open-circuit voltage (V_{OC}) under varying irradiation and temperature levels,in which the input voltage of solar cell is regulated at a reference voltage which is found to be $0.7 \times V_{OC}$, to get the maximum power. This technique is simple and less power consuming. Since V_{OC} changes with the irradiation, we need to do periodic sampling to update the new Voc value for which we need to switch off converter which is again wastage of power. But still, most of the industrial products BQ25505 [8], ADP5090, LTC3105, etc use FOCV technique for MPPT.

1.2 Objective of Work

A self-sustainable energy harvesting system that maintains battery voltage at 5 V is designed. The solar cell is used to charge the battery if the battery goes lower than the over-voltage potential (5 V). The battery supplies power whenever the load demand.

1.3 Thesis Organisation

For making WSN energy autonomous, it is proven that energy harvesting is the prominent solution. The focus of the work is on the design of a medium power solar energy harvesting system

(0.5-1 W). In Section 1.1.1 it is explained how, among the available energy sources, solar is the best solution to meet the increased power demand of WSN, Chapter 2 discusses the need of DCM mode of operation and also the component selection. Chapter 3 discusses in detail the complete architecture of energy harvester with the proper explanation of sub-blocks in the system including the MPPT technique. Chapter 4 includes the simulation results for validating the proposed schematic.

Chapter 2

Mode of Operation and Component Selection

2.1 Continuous and Discontinuous Conduction Modes

As mentioned earlier the inductor based step-up DC-DC converter is preferred for boosting the solar cell voltage as shown in Fig. 2.1. The basic boost converter is The boost converter operation is broadly classified into two modes depending on the nature of the inductor current. They are Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). In CCM the inductor current flows during the entire cycle and never reaches zero, whereas in DCM the inductor current flows only during part of the cycle. In DCM it falls to zero, remains at zero for some time interval, and then starts to increase as represented in Figures 2.2,2.3.

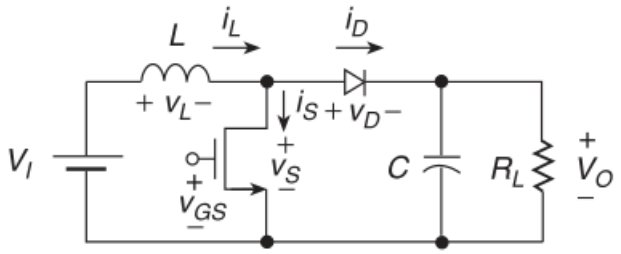

Figure 2.1: DC-DC boost converter from [5].

In CCM, power transfer is a two-step process. When the switch is ON, energy builds in the inductor. When the switch turns OFF, energy transfers to the output through the diode.

In DCM, a switching cycle is composed of three intervals. The first two are the same as in CCM,

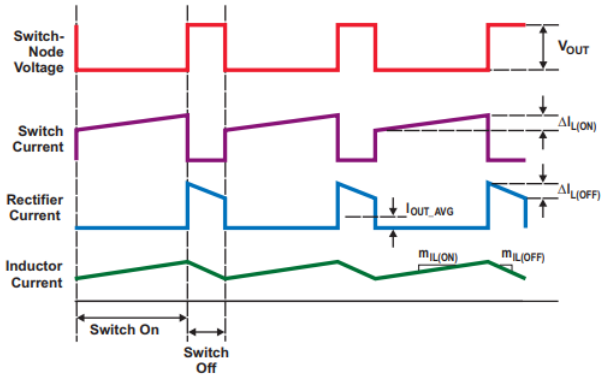

Figure 2.2: Representative CCM waveforms of [6].

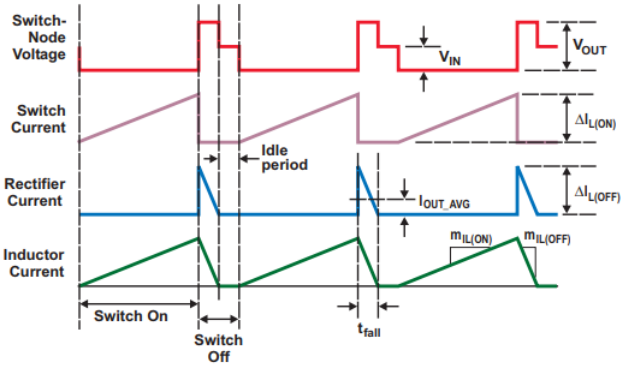

Figure 2.3: Representative DCM waveforms of [6].

where energy is stored in the inductor during the ON time of the switch in the first interval, and transferred to the load during the OFF time of the switch in the second interval. In DCM, however, all of the energy in the inductor transfers to the load during this second interval. The third interval begins when the energy in the inductor is depleted and continues until inductor starts charging again in the next switching period.

Since all the energy in the inductor discharges in each switching cycle during during the OFF time of the switch,for driving same load the peak inductor current (I_{L-pk}) current must be higher in DCM than in CCM.

By assuming zero losses, ON-time slope of the inductor current(I_L)

$$m_{IL(ON)} = \frac{V_I}{L} \tag{2.1}$$

During OFF time, the slope of I_L is

$$m_{IL(OFF)} = \frac{V_I - V_{OUT}}{L} \tag{2.2}$$

To maintain the inductor current steady at a value, CCM requires high-frequency switching when compared with DCM. Hence, Switching and recovery losses become significant in CCM.

The load is pulsating load, ie ., for most of the time it will be in sleep mode, taking less current in the order of mA. If the converter is operated in CCM for less current, very high switching frequency is required. Switching and recovery losses will dominate. So, by operating the system in DCM and selecting proper switches, all the losses can be minimized. RMS losses will be negligible because the load is pulsating as mentioned before.

2.2 Component Selection

The system should work for desired frequency in DCM with minimal losses and meet requirements of the load. Depending on this the main components of the boost converter (inductor, capacitor and switches) are selected.

2.2.1 Inductor Considerations

Inductance(L) is calculated from the CCM-DCM boundary condition

$$L \leq \frac{(R \times T \times (M-1))}{2M^3} \tag{2.3}$$

where M= $\frac{V_{OUT}}{V_I}$;
with V_{OUT} = 5 V, V_I = 2 V, and R =50 Ω the calculated value of L is:

$$L \leq \frac{(50 \times 50\mu \times (2.5-1))}{2 \times 2.5^3} \tag{2.4}$$

ie., $L \leq 78.125\ \mu H$ for system to operate in DCM
Allowing for start-up transients, a standard-value inductor L = 47 μH can be used.

2.2.2 Output Filter Capacitance

Depending on the required Ripple Voltage ($\triangle V_{C_{STOR}}$), the amount of capacitance needed (C_{STOR}) and the capacitors equivalent series resistance (r_{ESR}) are selected. Power Dissipation, ripple Performance, and transient Performance depend on r_{ESR}.

Ripple Voltage across the capacitor is

$$\triangle V_{C_{STOR}} = \frac{\triangle Q_{C_{STOR}}}{C_{STOR}} = \frac{I_{L-pk} \times (1-D) \times T}{C_{STOR}} \tag{2.5}$$

The above equation is based on the assumption that all inductor ripple current flows through the capacitor.

If the desired output ripple voltage is 125 mV, then the capacitance needed is:

C= 58 μF

Where effective series resistance of C_{STOR} (r_{ESR}) is:

$$r_{ESR} = \frac{\triangle V_{r_{ESR}}}{\triangle I_{L-pk}} \tag{2.6}$$

where $\triangle V_{r_{ESR}}$ is ripple voltage across r_{ESR} For $\triangle V_{r_{ESR}}$=100 mV , r_{ESR} =100 mΩ

The ripple voltage cross output filter capacitor should be 25 mV to maintain overall voltage ripple below 125 mV. Capacitance calculated by considering r_{ESR} is C= 220 μF.

2.2.3 Power Switches

MOS Power Switches are always preferred over diodes because of flexible voltage and current control and also very less power dissipation.As the converter system is operated in DCM conduction losses dominate in switches.

$$\triangle P_D = I_{rms} \times r_{dc}^2 \tag{2.7}$$

To reduce the conduction losses,r_{dc} should be reduced. For this huge switches of width 10 mm with minimum length 600 nm are employed and are preceded by buffers to reduce the loading effect.

Chapter 3

Self-Sustainable Power Management System Modeling and Architecture

3.1 Introduction

Energy harvesting has become an attractive solution since it ensures the continuous operation of WSN devices for a much longer lifetime. Some of the main issues involved with the energy harvesters are a) very less average input power, b) unregulated input power, c) input power is sporadic in nature, d) gives maximum power for a particular load and cant handle a wide variety of load with the same efficiency. So an energy harvesting system should be capable of addressing all these issues. A generic block diagram for a typical energy harvesting in Fig. 3.1 shows the big picture of energy harvesting system along with the sub-blocks needed in an energy harvesting module.

In this figure energy harvester is connected to charger and MPPT block through an interface. The charger is nothing but a step-up DC-DC converter to boost the input voltages and MPPT block is required to extract maximum power from the solar cell. The interface circuit connects the MPPT block and charger with energy harvester so that impedance seen by harvester matches with the characteristic impedance of harvester for maximum power transfer. The harvested power is dumped into storage devices at a boosted voltage, and they work as energy buffers from harvester to the load.

It is not possible to directly drive the load from harvester since the input power is un-deterministic in nature. So a battery is required to collect the maximum power from the harvester at any instant. This harvested power with the regulator is supplied to the load as per load requirement. Since these storage devices (battery, solid-state cell, super-capacitor) have certain under and over-voltage limits to ensure proper longer life operation, under-voltage and over-voltage protection is also present in the system which is collectively called as battery management. Also one of the crucial blocks is cold start which is required when the battery got drained out fully. Since the whole system is powered through the harvested power itself by storage device so in a scenario when storage device does not have any charge, the cold start-up will become functional as it is directly supplied by harvester input and charge the storage device to some level from where the main converter will overtake the charging operation. The main converter includes all the circuits other than start-up circuit and usually very much efficient than the start-up circuit.

3.2 Energy Harvesting System Architecture

The solar energy harvesting system in this work is using boost converter as DC-DC step-up converter so that a sufficient amount of power can be extracted with greater efficiency as briefed by Section 2.1. Boost converters are classified into synchronous and asynchronous based on the control to the high side switch. Synchronous type converters use two non-overlapping clock signals NMOS and PMOS which act as control switches. Asynchronous converters use a single clock signal to control NMOS and a diode is connected instead of PMOS. The synchronous converter has much higher controllability than asynchronous converter which is rather simple but incurs high power losses.

On the basis of the type of NMOS and PMOS clocks are given (abbreviated as CLKN and CLKP in this thesis), there are many controlling techniques for boost converter namely (a) Pulse Width Modulation (PWM) (b) Pulse Frequency Modulation (PFM) and (c) Pulse Skipping Modulation (PSM) is also used.

- In (a), a fixed frequency clock signal is used for CLKN and CLKP and the on-time/ duty cycle of the control pulse is varied according to the system behaviour [11], [7] (for regulation/MPPT purposes).

- In (b), the frequency of the clock signal itself varied and the duty cycle may or may not be

fixed [12] and

- In (c) a fixed frequency, fixed duty cycle pulse is used (Constant Frequency Constant Pulse Width) but pulses are sent to switches or stopped depending on the system behaviour [13]. In our case owing to its controllability, Pulse Frequency Modulation is used to drive the synchronous high and low side switches.

The reason for preferring DCM mode operation of boost converter over CCM is already discussed in Section 2.1. In DCM mode operation zero current switching is one of the critical issues or bottleneck to be handled carefully as negative inductor current as mentioned above leads to the wastage of harvested energy thereby degrading system efficiency to a much greater extent. The methodology used to prevent negative inductor current in this work is explained later in this section.

On a shorter note, in this work, an inductor based DCM operated PFM controlled boost converter is used as a DC-DC converter for charging the output battery. The complete architecture is shown in Fig. 3.1 below. Block-wise description of the system components along with chronological order of execution is explained in following sub-sections.

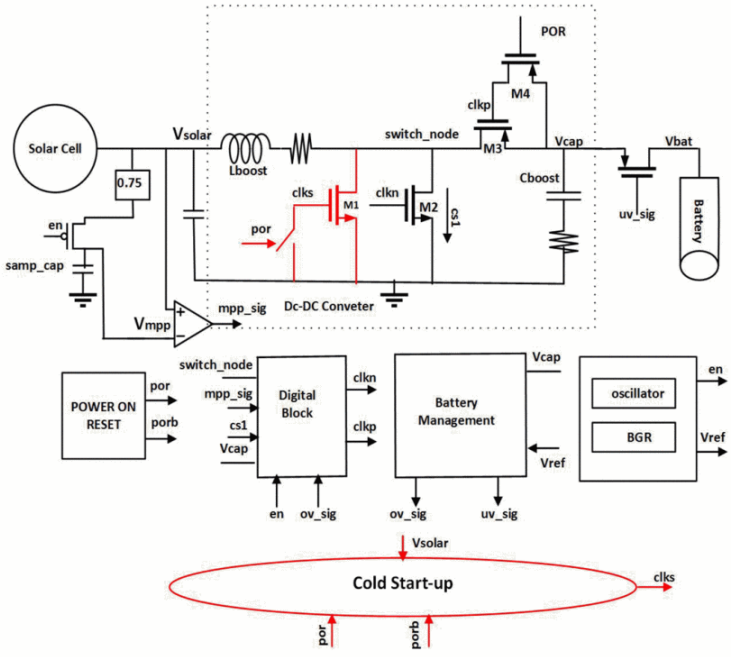

Figure 3.1: Complete architecture of solar energy harvesting system of [9].

3.2.1 Boost Converter

Boost converter become operational once the system enters into main converter mode. It is the main entity for boosting up the low input voltage (of around 1V-3V) to a higher output voltage (until 5V in this work) is analysed in a brief manner here. As shown in the Fig. 3.1, initially M2 is ON (NMOS) and M3 is OFF (PMOS), so that inductor is connected with the input voltage source (solar cell), and shorted to ground through NMOS. The inductor current is allowed to rise until a preset value denoted as I_{SAT} , after which M2 is OFF and M3 is ON. Now, the charged inductor current is discharged to the storage capacitor C_{STOR} through the PMOS switch M3, until the inductor current drops down to zero.

The charging slope of inductor current is given by V_{SOLAR}/L and the discharging slope is given by $(V_{SOLAR} - C_{STOR})/L$ (negative since for boost converter $V_{OUT} > V_{SOLAR}$), and in this case since V_{SOLAR} is regulated at V_{MPP} as will be discussed later in this section, and C_{STOR} charges from 2.4 V to 5 V.The charging slope is relatively constant compared with the discharging slope which increases gradually as C_{STOR} is getting charged. This justifies the PFM operation of the boost converter.

The efficiency of the converter is dependent on the switching and conduction losses incurred by the inductor series resistance, capacitor series resistance, M2, M3 on resistance (for conduction loss) and losses caused by parasitic capacitances of MOSFETs proportional to the frequency of operation (for switching losses). To achieve best efficiency MOSFETs are sized properly by analysing conduction and switching losses as explained in Section 2.2.3. The mechanisms through which V_{SOLAR} is regulated to V_{MPP}, the inductor current is limited between I_{SAT} and 0 A and the switches are controlled by CLKN and CLKP generation are discussed in the following sub-sections. Since the system is used for charging rechargeable batteries quite often, it is essential to make sure that the battery voltage must be maintained in a required rated range for its better lifetime without draining it so low or charging it to much higher voltage. To maintain battery operation limits ,battery management unit is also designed which performs under-voltage, over-voltage protection and is also explained later in this section.

3.2.2 Regulating Solar Cell Potential at Maximum Power Point

The need and types of maximum power point tracking are discussed exhaustively in Introduction and also in Section 1.1.1. As mentioned earlier MPPT technique used in this work is FOCV technique which relies on the fact that maximum power from a solar cell can be extracted if it is made to operate at a voltage V_{MPP} which is 0.7 times its open circuit voltage (V_{OC}). To do so, the system needs to be open circuited for long enough time for solar cell to reach to its V_{OC} and a fraction of the open circuit voltage should be held in a off-chip capacitor so that it can be used as reference for MPP regulation for rest of the time period until the circuit is to be open circuited again. As shown in the Fig. 3.1 an enable pulse EN is used for maintaining this periodic sampling. V_{SOLAR} is open circuited (disconnected from the rest of the system) for the first 100 ms of off-period of EN pulse and then as EN goes high system is connected back to the harvester input. During the open-circuit period, V_{SOLAR} reaches V_{OC} and 0.7 times V_{OC} is stored in C_{MPP} as V_{MPP} through the resistor ladder, the same reference V_{MPP} is used until the end of the 2 s open circuit cycle until the circuit is open circuited again which occurs after 2 s.

As EN goes high, the charger is operational and MPP unit, which is basically a continuous rail to rail comparator, is enabled and it starts comparing the instantaneous solar input voltage V_{SOLAR} (which has just then started decreasing from its V_{OC}) with the reference MPP voltage V_{MPP} held in C_{MPP} and gives a high output as and when $V_{SOLAR} > V_{MPP}$). As charger is turned ON, the solar input voltage drops as the current is taken from it, by the charger circuitry. Whenever the solar voltage just drops below V_{MPP} value, the charger is turned off by the digital controller (explained in Section 3.2.6), hence the solar voltage again rises, since its load is disconnected. Again as V_{SOLAR} goes above V_{MPP}, charger is connected V solar slowly drops down and this process continues, and through this V_{SOLAR} is regulated very closely about V_{MPP} , with a very small ripple dependent on harvester cap and the comparison delay introduced by the comparator. It is preferable for this comparator to give a small amount of delay so that the regulation happens slowly, otherwise, V_{SOLAR} will toggle so fast making $V_{MPP-SIG}$ (comparator output) also to toggle so fast, which will increase the operating frequency for boost converter and lead to more switching losses. Delay introduced by sub-threshold rail to rail comparator is favorable to system.

Since the system is designed to cover wide solar input voltage range, V_{SOLAR} varies widely due to solar illumination and type of solar array from 700 mV to 4 V . In order to compare this rail to

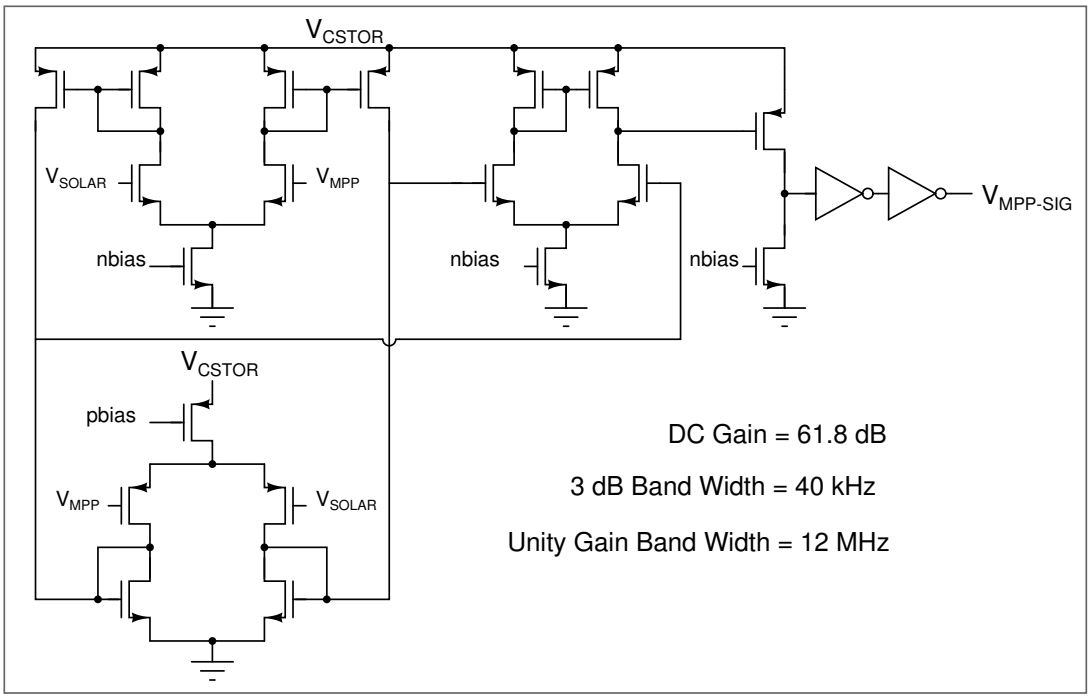

Figure 3.2: Rail to rail comparator architecture.

rail range of voltages, it is essential for a rail to rail comparator as shown in Fig. 3.2 which has both PMOS input and NMOS input structures (differential to differential), followed by a differential to single ended NMOS input conventional structure.

3.2.3 Current Sensor

The inductor current is limited to a fixed peak value I_{SAT} (in our case maintained at 1 A), decided based on inductor used (47 μH in our case) and design specification for maximum power (500 mW in our case). A current sensor circuit as shown in Fig. 3.3 is used to sense the current flowing through the switch node into switch M2. The Drain terminal potentials of power MOSFET M2 and sensing MOSFET M6 are made equal by opamp operating in negative feedback. Since M6 is sized 116666 times lower than NMOS switch, sensing current will scale down to 8 μA and same current will flow to M7. The current is mirrored from M5 to M7 and allowed to flow through a resistor which will produce the voltages corresponding to current flowing in inductor. A 300 fF capacitor is used to filter the current glitches in the switch which may false trigger the I_{SAT} comparator and the controller operation would then become unexpected and hence would seriously affect the system functionality.

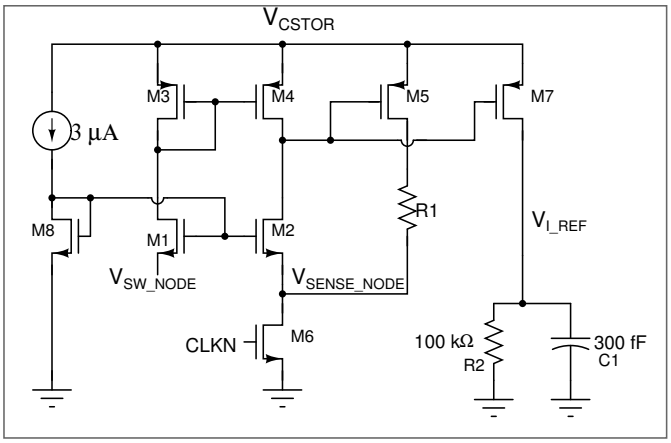

Figure 3.3: Current sensor architecture used in the main converter.

3.2.4 Limiting the inductor current between 0 A and 1 A

A conventional NMOS input two stage continuous time comparator is used whose common mode range varies from 900 mV to 5 V so that a wide range of peak current values from 125 mA to 4 A can be detected. The I_{SAT} comparator compares the instantaneous inductor current value with predefined fixed reference scaled from BGR output and generates a high signal I_{SAT} whenever inductor current crosses I_{SAT} value fixed. The comparator is designed with high gain of 85 dB across all process corners and a good unity gain bandwidth of 25 MHz sufficient enough to operate even at the highest system frequency.

For zero current switching same comparator is reused, denoted as I_{ZERO} comparator, to compare the voltage across the PMOS switch. During discharge phase of inductor current, the current flows from inductor to C_{STOR} and hence switch node will be at higher potential compared to C_{STOR} node voltage value (V_{CSTOR}). As the current decreases and crosses zero, if the PMOS switch is not turned off, then in order to maintain the current continuity, the inductor current flows negative which means current is flowing from C_{STOR} towards inductor by which time switch node will be at lesser voltage than C_{STOR} node voltage. By monitoring both switch node and C_{STOR} voltages, it can be inferred whether inductor current is positive or negative. This simple method eliminates the use of another current sensor across PMOS switch, and I_{ZERO} comparator compares switch node and C_{STOR} nodes during discharge phase and gives a high signal I_{ZERO} when, V_{CSTOR} goes above switch node. An important point to note in the design of this comparator is that, it always compares V_{CSTOR} value with a little bit higher value, but V_{CSTOR} is the supply of the system itself. So the comparator is designed to provide a high gain with common mode voltage equal to supply voltage,

and the robustness of this comparator is very crucial since it is essential for zero current switching as mentioned before.

3.2.5 The Requirement of the Free Running Clock When $V_{SOLAR} > V_{C_{STOR}}$

As the load requires maximum power of 0.5 W and with 5 V DC supply, solar panel should have high power density for the system to work even at low irradiation.Typical value of V_{OC} of the solar cell considered is about 3 V.There arises a condition where V_{SOLAR} and V_{CSTOR} become equal due to which slope of inductor current become zero when C_{STOR} is charging. Because of this CLKP is always on and CLKN is always off. To solve this problem, until V_{CSTOR} crosses V_{SOLAR} converter is operated in open loop. V_{SOLAR}, V_{CSTOR} signals are given to a comparator. The comparator output $V_{SOLAR-CSTOR}$ will be high if $V_{SOLAR} > V_{CSTOR}$ and it will be zero when $V_{SOLAR} < V_{CSTOR}$. A free running clock is used for switching until the $V_{SOLAR-CSTOR}$ become zero. As soon as V_{CSTOR} become greater than V_{SOLAR} system is operated in normal boost converter mode of operation.

3.2.6 Digital Controller

Digital controller serves as the heart of the system, which takes care of maintaining V_{SOLAR} at MPP point, switching the low and high side drivers to charge the capacitor C_{STOR} to 5 V from 2.4 V, preventing zero inductor current from flowing and thereby maintaining the entire system performance. The inputs to digital controller are EN signal discussed earlier, I_{SAT}, I_{ZERO} and $V_{SOLAR-CSTOR}$ signals provided by three comparators which are explained above, OV_{SIG} given by the battery management unit and $V_{MPP-SIG}$ from the MPP block as mentioned above indicating V_{SOLAR} is greater than V_{MPP} . The basic digital controller is a simple SR flip flop which is Set by I_{ZERO} signal and Reset by I_{SAT} signal from the respective comparators discussed before and the flip flop output gated with OV_{SIG} and $V_{MPP-SIG}$ signals. But there are yet a lot of crucialities and logical issues in implementing the same, which are elaborated below.

General operation is that if $V_{SOLAR} > V_{MPP}$ and $V_{CSTOR} < V_{OV}$ (over-voltage), then the boost converter should work in the same way as mentioned above i.e inductor current should be limited from I_{SAT} to zero. Otherwise, both the switches M2 and M3 need to be off to make the charger off. There are some other critical issues which are mentioned below and digital controller is modified accordingly to cater all these issues.

- NMOS and PMOS both can be turned off together, but must not be ON at the same time since this would provide a direct path to ground for C_{STOR} which would discharge through a huge current and suffer from

- Since in addition to just charging C_{STOR} by maintaining the inductor current between I_{SAT} and zero, it is also required to maintain MPP condition to extract maximum power from solar cell input, hence digital controller should take care that V_{SOLAR} is regulated around V_{MPP} closely.In order to account for the case in which $V_{MPP-SIG}$ is low but inductor current is yet to charge to I_{SAT}, $V_{MPP-SIG}$ is given higher priority and hence discharge phase starts immediately without waiting for the inductor current to reach I_{SAT}.

- While implementing this the complexity that may arise is that, if V_{SOLAR} falls down V_{MPP} and $V_{MPP-SIG}$ goes low at an instance when inductor current is non-zero, the system may stop both the clocks as $V_{MPP-SIG}$ is low. But this will cause switch node to rise one V_{th} above the voltage on C_{STOR}, which can be higher than the maximum voltage (5 V devices) seen by the CMOS devices. In this situation CMOS devices will be stressed every time and may lead to device failure in longer run.

- To avoid this situation, care should be taken that even if $V_{MPP-SIG}$ goes low, PMOS M3 should be off only when inductor current reaches zero. To make sure that $CLKP$ is not high before inductor current reaches zero even if $V_{MPP-SIG}$ goes low, it is necessary to mask $V_{MPP-SIG}$ from influencing the clock output, which is done with the help of a D Flip Flop, through which $V_{MPP-SIG}$ is transferred only if I_{ZERO} is received and a mux is used to select between clock signals for the D Flip Flop with select signal being D Flip Flop Output.

- Similar case is to be taken care for OV_{SIG} also, since it demands for same as $V_{MPP-SIG}$ i.e. Turning off the boost converter.

To implement a robust logic considering all these constraints, digital controller designed is given by the below Fig. 3.4 and the explanation is as follows:

To begin with, the SR flip flop is used for the main logic to generate clock signals, to turn ON NMOS when I_{ZERO} is received, by pulling clock to VDD (hence given in set input of SR FF) and

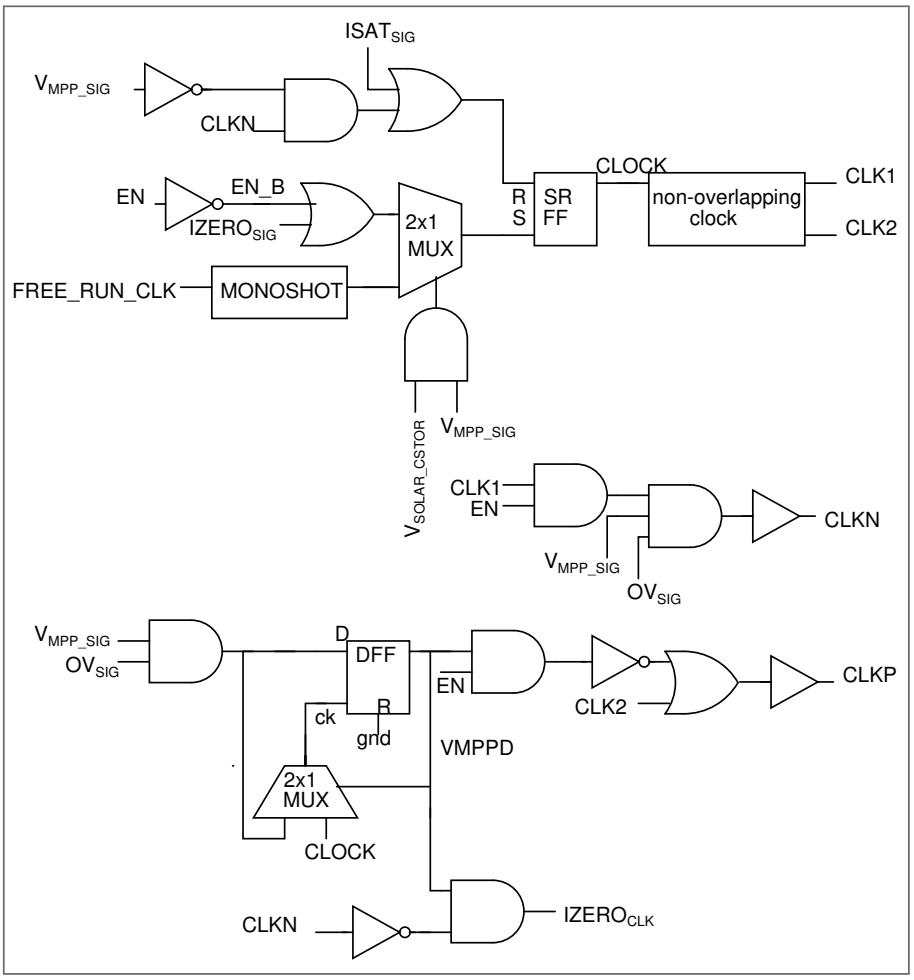

Figure 3.4: Digital controller architecture used in the main converter.

to turn ON PMOS when I_{SAT} is received by making clock zero (hence given in reset input of SR FF). $CLKN$ and $CLKP$ are generated from the non overlapping clock signals by taking the above specified critical issues into consideration.

Since these digital level signals will not be able to drive huge MOSFET switches, buffers are used as gate drivers for NMOS and PMOS switches. OV_{SIG} from battery management is also another criterion to be taken care which also plays almost same role as $V_{MPP-SIG}$, so that's why AND gated with $V_{MPP-SIG}$ as shown in Fig. 3.4. Comparators and digital controller part can be best realized by simulation results in Chapter 4.

3.2.7 Battery Management

Battery Management subsystem is responsible for the maintenance of the battery voltage V_{BAT} within the upper and lower bounds hence ensuring a good life for the battery. It is very essential for the battery that it should not be drained below a voltage or overcharged above a voltage, which differs from one battery to another. In this case, the under-voltage limit for battery is taken as 4 V and the over-voltage limit is 5 V. However, it can be made programmable as shown below.

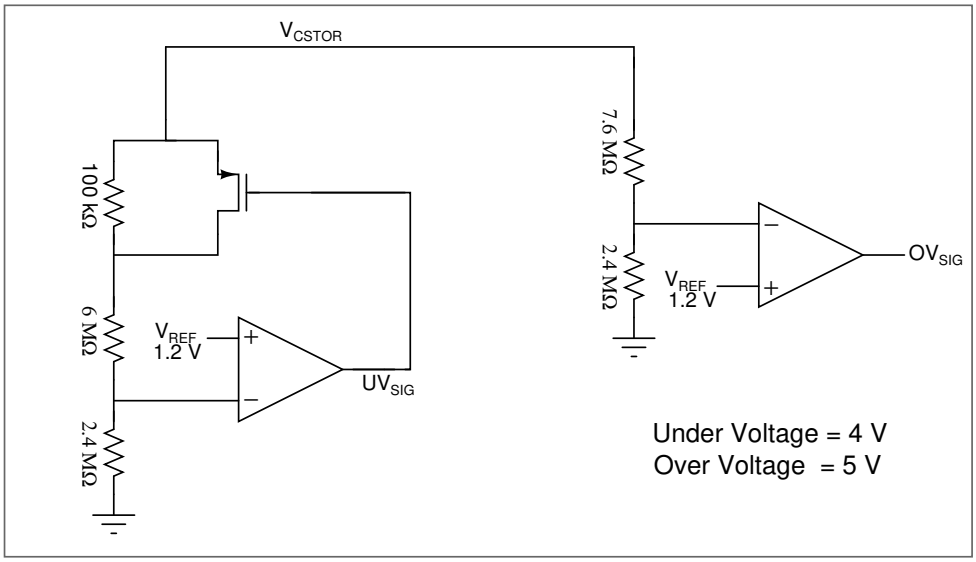

Figure 3.5: Battery management architecture used in the main converter

The Fig. 3.5 shows the battery management system used in the architecture, it consists of two conventional continuous time comparators and some logic circuits. As the C_{STOR} charges from 2.4 V in main converter mode, it's potential is compared with a reference voltage of 1.2 V after being scaled by Resistors designed in such a way that, when V_{CSTOR} reaches 4 V, UV_{THR} node reaches 1.2 V. Once V_{CSTOR} crosses 4 V UV_{SIG} goes low which turns ON the PMOS connecting V_{BAT} with C_{STOR} .

For over-voltage, a continuous subthreshold comparator is used without any clocks.This can be implemented by the same comparator used for generating UV_{SIG} by connecting CLK pin of comparator to signal high (V_{CSTOR}) always.

Load is connected to C_{STOR} so that when V_{BAT} is less than UV_{THR}, battery gets disconnected

from load and C_{STOR} is used as a supply for the load A short-hand explanation of battery management block is as given below:

- $C_{STOR} >= UV_{THR}$: Turn ON the PMOS between C_{STOR} and Battery and start charging the battery.
- $C_{STOR} >= OV_{THR}$: Disconnect the total charger circuitry and hence the whole power train (thereby leaving the V_{SOLAR} to reach its V_{OC})

3.2.8 Auxiliary Circuits

Op amp based reference voltage generator is designed as in Fig. 3.6.

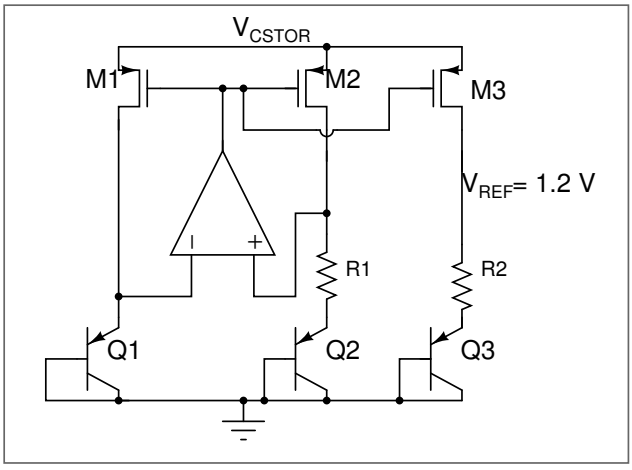

Figure 3.6: Reference voltage generator

I_{bias} for the op-amp is provided by a supply independent (Proportional to Absolute Temperature) PTAT current reference generator shown in Fig. 3.7.

$$IR_1 = V_{BE1} - V_{BE2} = V_T lnn \tag{3.1}$$

$$I = \frac{V_T lnn}{R_1} \tag{3.2}$$

$$V_{REF} = IR_2 + V_{BE3} = \frac{R_2 V_T lnn}{R_1} + V_{BE3} \tag{3.3}$$

The supply and temperature independent voltage Reference generated can be converted to current by using a trans-conductance amplifier. The reference current I_{REF} is current mirrored and

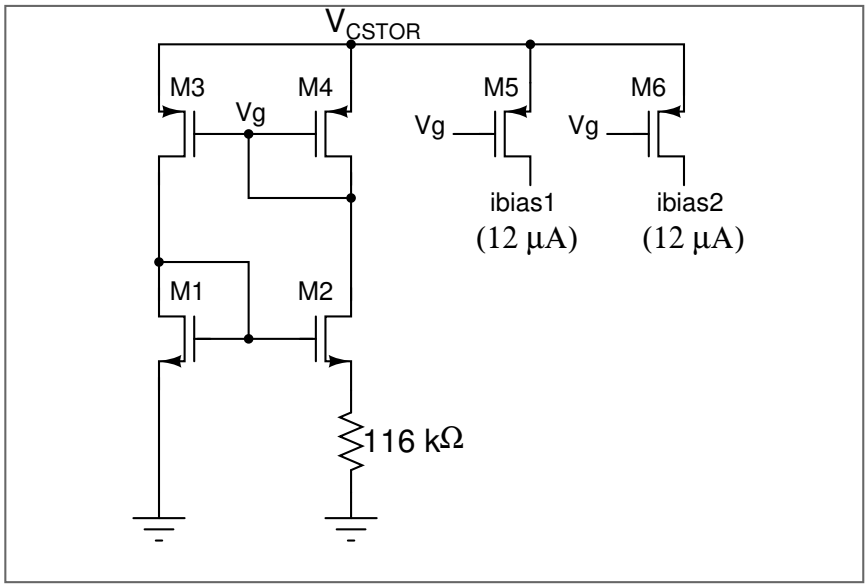

Figure 3.7: Supply independent current reference for op amp

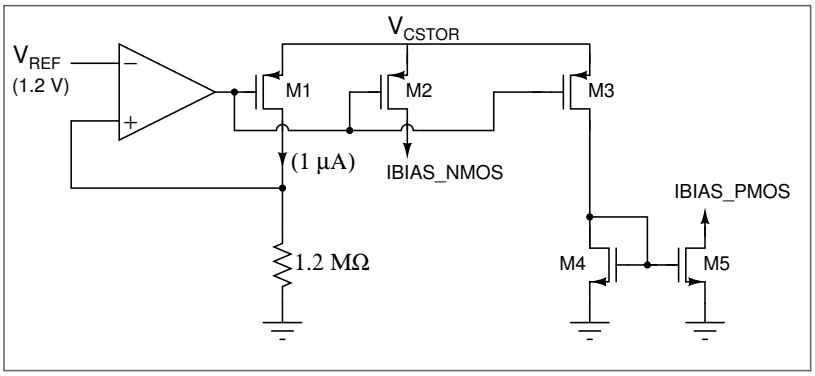

Figure 3.8: Reference current generator

given as bias current for comparators, current sensor and state machine as shown in Fig. 3.8.

Chapter 4

Simulation Results and Verifications

The results for the proposed architecture are simulated and verified.

4.1 Full System at Higher Solar Irradiation

Full system with 50 Ω load is simulated at higher irradiation. As shown in Fig. 4.1 V_{SOLAR} is regulated around V_{MPP} voltage. Until $V_{SOLAR-CSTOR}$ goes low the system is operated in open loop with the help of a free running clock. When UV_{SIG} goes low V_{BAT} is connected to C_{STOR}. As soon as OV_{SIG} become low all the switches are off and the battery stops charging.

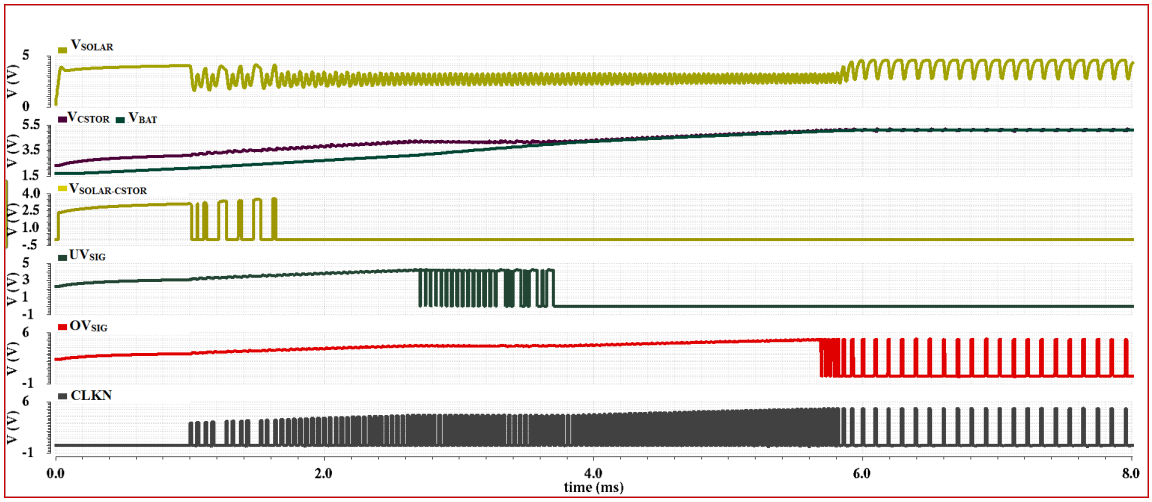

Figure 4.1: Full system results for N_P=8, at 100% solar irradiation for 50 Ω load

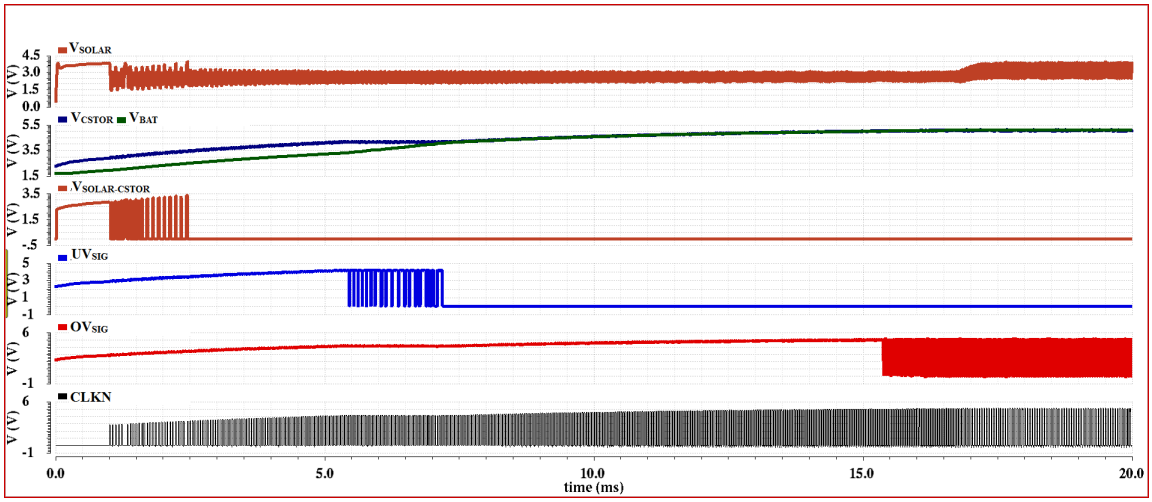

Figure 4.2: Full system results for N_P=8, at 100% solar irradiation for 24 Ω load

The C_{STOR} attains 5 V at 5.6 ms. Efficiency of the system is observed as 88.9% when output is stable at 5 V

The maximum power that the battery can provide is upto 1.25 W. From Fig. 4.2, at maximum load of 24 Ω the system attains 5V at 17 ms. Efficiency of the system is observed as 86.1% when output is stable at 5 V.

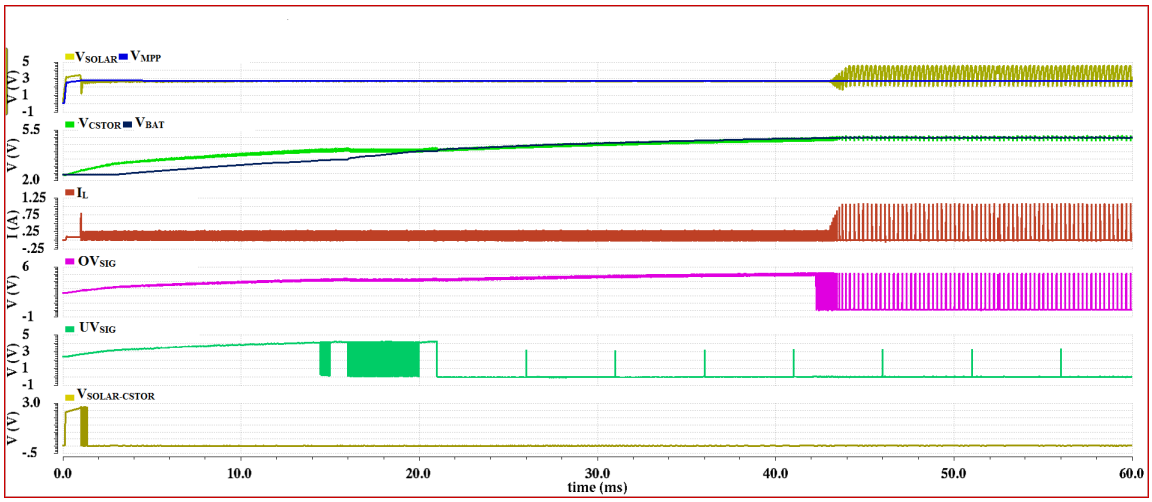

Figure 4.3: Full system results for N_P=8, at 10% solar irradiation for 120 Ω load

4.2 Full system at Lower Solar Irradiation

Input power at 20% of maximum irradiation is 0.25W which is less as required power is 0.5W. Considering 88% efficiency, the maximum load,the system could drive is 113 Ω. Fig. 4.3 shows the

results at 120 Ω load. C_{STOR} takes 44 ms to charge from 2.4 V to 5 V. The efficiency of the system is 88.2%.

4.3 Sub-Blocks Explanation

The sub-blocks functionality can be further understood with the help of following results.

4.3.1 Current Sensor Waveforms

The switch node potential is matched with Drain potential of $V_{SENSE-NODE}$ MOSFET and current is scaled by a factor of 116666 times of I_L. This scaled current is converted to voltage in V_{REF} range by a resistor. V_{IREF} in Fig..4.4 shows the voltage generated corresponding to the sensed inductor current

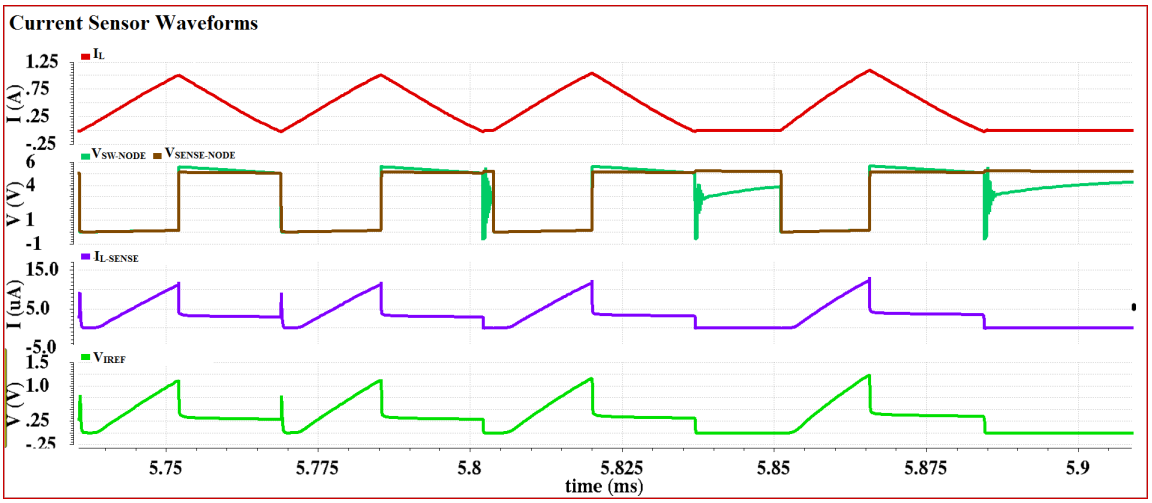

Figure 4.4: Current sensor waveforms

4.3.2 I_{SAT} and I_{ZERO} Waveforms

I_{SAT} and I_{ZERO} comparators are used to limit the peak and minimum inductor currents between 1 A and 0 A respectively.

Resistor in current sensor is adjusted such that V_{IREF} equal to 1.2 V corresponds to 1 A of inductor current. I_{SAT} comparator compares V_{IREF} with V_{REF} and turns on $ISAT_{SIG}$ whenever V_{IREF} crosses vREF as in Fig. 4.5

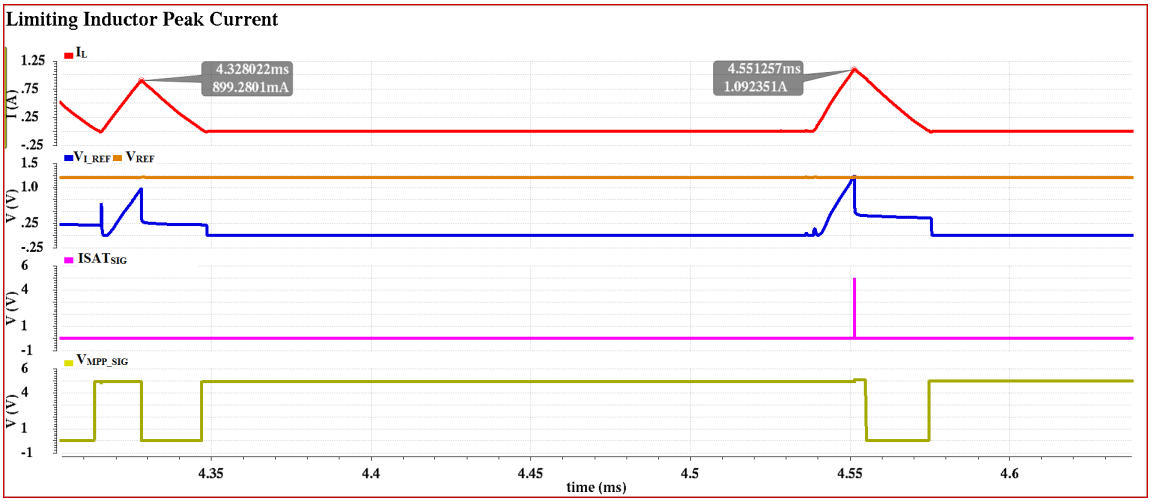

Figure 4.5: I_{SAT} comparator waveforms

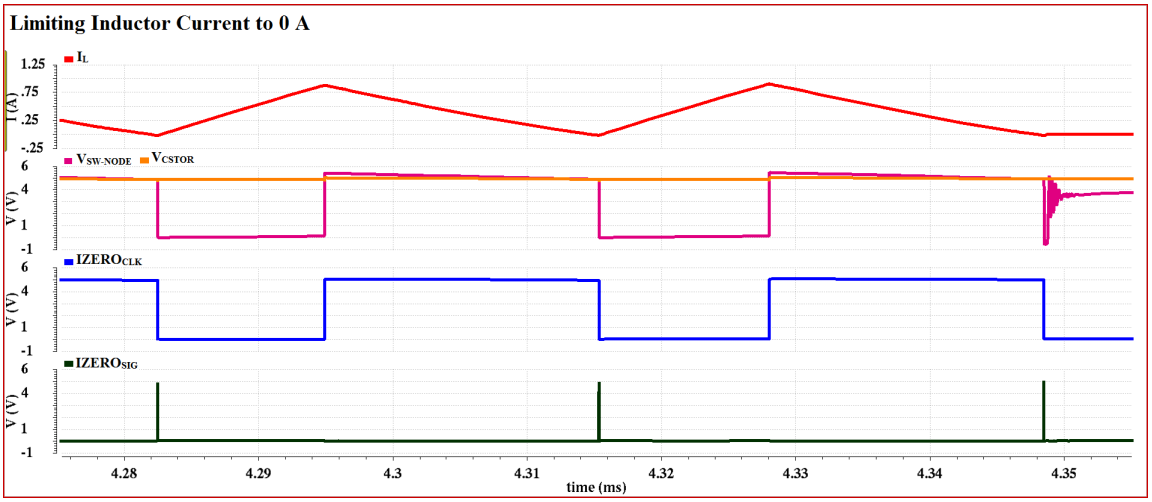

Figure 4.6: I_{ZERO} comparator waveforms

C_{STOR} and switch node potentials are monitored during discharge phase of the inductor.As soon as switch node potential goes below C_{STOR} potential $IZERO_{SIG}$ turns on.$IZERO_{CLK}$ acts as a enable signal for the comparator. Fig. 4.6 shows the waveforms corresponding to izero comparator.

4.3.3 The Digital Controller Waveforms

Fig. 4.7 shows the digital controller waveforms. CLKN is on until $ISAT_{SIG}$ become high. If $V_{MPP-SIG}$ goes low before inductor reaches I_{peak}, high priority is given to $V_{MPP-SIG}$ and CLKN turns off and inductor starts discharging as CLKP goes low immediately. During discharge phase high priority is given to $IZERO_{SIG}$ i.e. CLKP will be low until izero signal is reached irrespective of $V_{MPP-SIG}$ and OV_{SIG}. If OV_{SIG} become low CLKN is turned off immediately and CLKP goes

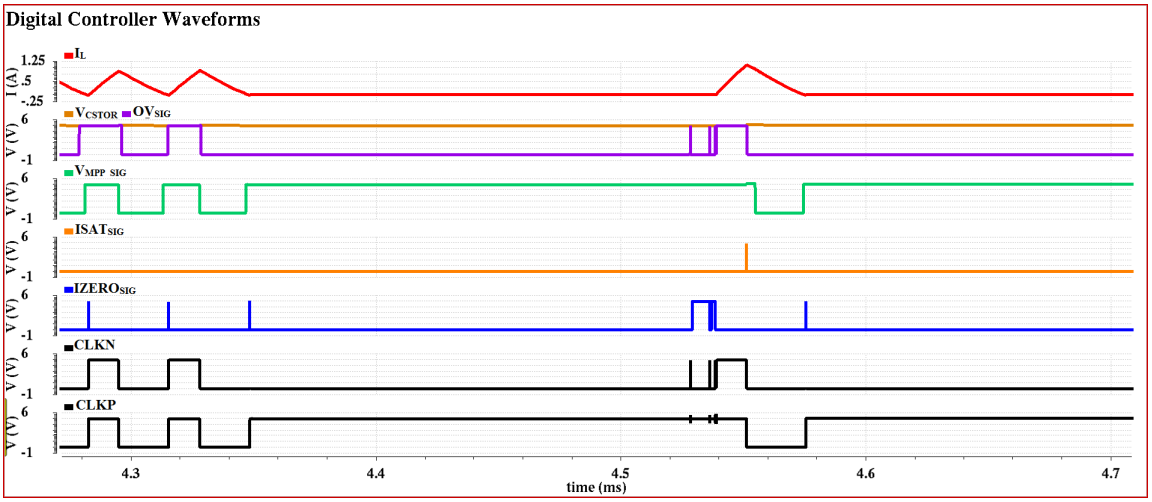

Figure 4.7: Digital controller waveforms

high after inductor current reaches 0A.

4.3.4 Battery Management Waveforms

Battery management waveforms are already explained along with the full system results.

4.3.5 Simulation Results

The table 4.1 gives the input power(P_{IN}), output power(P_{OUT}), power dissipated (P_D)(across the switches(P_{D-SW}), inductor series resistance(P_{D-RL}), main converter(P_{D-CKT})) and efficiency(η) of the energy harvesting system for different sun conditions with the number of solar cells in parallel(N_P) as 4 and 8.

Table 4.1: Simulation results.

N_P	SUN	P_{IN} (mW)	P_{OUT} (mW)	P_D (mW)			η (%)
				P_{D-SW}	P_{D-RL}	P_{D-CKT}	
4	0.1	77.5	72.1	1.4	0.2	4	93.0
	0.5	392	365	10.3	2.9	13	93
	1	721	681	25	5	10	94.5
8	0.1	155.4	145.6	0.3	0.7	8.7	94.3
	0.5	782	740	32.5	9.7	9.6	93.4
	1	1385	1250	87	26	15	90.7

1 SUN = 4.2 mW/cm^2 for solar cell MP3-37

Chapter 5

Conclusion and Future Work

5.1 Summary

This work deals mainly with the modeling and design of an efficient solar energy harvesting system as a strong assistance to power IoT. A generic solution for wider input voltage/power range harvester(1 V-3 V) is given and output can be regulated to required voltage(3 V-5 V) by varying resistance of resistive ladders in under-voltage and over-voltage protection in battery management.System performance is verified with the simulation results. This system includes the following novelties.

- A robust energy harvesting system is proposed which will work even with wide variations in input voltage(1V-3V) and temperature(-40^0 C to 120^0 C) that can supply a power of 0.5 W to the load.
- The problem of C_{STOR} getting shorted to V_{SOLAR} due to zero inductor slope was solved.

5.2 Future Work

This thesis deal with the design of inductor based solar energy harvester circuits. However, there are many open problems related to this area that can lead to a much improved robust energy harvester circuits.

- The energy harvester is designed only for DC transducers. There can be small modification made in the circuit to make it harvest energy from the multiple sources like TEG, RF, Vibrational energy. For example, with the proper rectifier design we can convert AC RF power to

DC RF power.

- The system can be extended to support multiple loads.
- Peak inductor current can be made variable depending upon the load requirements, so that conduction losses can be further minimized.

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