Metal-alloy Cu surface passivation leads to high quality fine-pitch bump-less Cu-Cu bonding for 3D IC and Heterogeneous Integration applications

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Abstract— **In this paper, we report a low temperature, fine-pitch, bump-less, damascene compatible Cu-Cu thermocompression bonding, using an optimized ultra-thin passivation layer, Constantan, which is an alloy (Copper-Nickel) of 55% Cu and 45% Ni. Surface oxidation and its roughness are the major bottlenecks in achieving high quality, low temperature, and fine-pitch Cu-Cu bonding. In this endeavor, we have used Cu rich alloy (Constantan) for passivation of Cu surface prior to bonding. We have systematically optimized the constantan passivation layer thickness for high quality low temperature, low pressure, bump-less Cu-Cu bonding. Also, we have studied systematically the efficacy of Cu surface passivation with optimized ultra-thin constantan alloy passivation layer. After rigorous trial and optimization, we successfully identified 2 nm passivation layer thickness, at which very high quality Cu-Cu bonding could be accomplished at sub 200 °C with a nominal contact pressure of 0.4 MPa. Post-bonding, electrical and mechanical characterization were validated using four-probe IV measurement and bond strength measurement respectively. Furthermore, Cu-Cu bonding interface was analyzed using IR wafer bonder inspection tool. Very high bond strength of 163 MPa and defect free interface observed by WBI-IR clearly suggests, Cu-Cu fine- pitch bonding with optimized ultra-thin alloy of 2 nm thick constantan, is of very high quality and reliable. Moreover, this novel bonding approach with alloy based interconnect passivation technique is the prime contestant for future heterogeneous integration.**

Keywords-alloy based passivation;Cu-Cu thermocompression bonding; surface passivation; ultra-thin constantan; bum-less bonding.

I. INTRODUCTION

Over the past four decades, improvement in Integrated Circuit (IC) performance was primarily achieved by solely focusing on continuously scaling down the device dimensions as per Moore's law. Consequently, IC scaling technology which have essentially remained a planar platform throughout the period of rigorous scaling, has hit rock bottom. Furthermore, ever-growing demand of user's for smaller and faster devices with more user reliable functionalities day-by-day are really grand challenge for device scaling due to physics limits [1]. Hence focus of semiconductor industries has changed completely from device scaling to innovation in system architecture which in turn enhances IC performance. Another significant challenge has emerged in recent years is that the interconnect performance which is limiting the overall performance of the system. Therefore, in order to ceaselessly enhance the system performance demands, new interconnect materials as well as innovative architectures need to be developed. Even though Cu and low-k dielectric materials offered improvements in system performance by taking care of global interconnect RC delay, their contributions were limited [2]. Hence, the focus has completely shifted from device scaling to developing new integration techniques. Flip chip technology, Low Temperature Co-fired Ceramic (LTCC) technology are some of them which have achieved little success.

Three dimensional (3D IC) integration technology is one of the best technique which not only CMOS compatible but also very reliable to industry adoption. Using 3DIC integration, multiple layers of devices are stacked with high density interconnects between the layers. Apart from this, 3D IC technology has a major advantage of supporting heterogeneous integration. Typically, 3D IC integration can be achieved using several stacking options like Wafer-on-Wafer (WoW) bonding, Wafer-on-Chip (WoC) bonding, and Chip-on-Chip (CoC) bonding [3]. Among all the available bonding approaches Cu-Cu WoW thermocompression bonding is the prime contender in achieving 3D IC integration due to several advantages like excellent mechanical strength, impressive electrical conductivity and superior electromigration resistance [4]-[9]. Cu-Cu thermocompression bonding mechanism involves interdiffusion of Cu atoms and grain growth at the bonding interface due to simultaneous application of temperature and pressure [10]. Pure Cu has high affinity towards oxygen and gets oxidized almost instantaneously upon its exposure to ambience. This native oxide layer then acts as barrier for the interdiffusion of Cu atoms. Hence for enhancing the diffusion process the oxide layer has to be removed prior to Cu-Cu thermocompression bonding. Apart from Cu surface oxidation, rough surface is also a barrier for high quality low temperature, low pressure Cu-Cu bonding. Very high surface roughness reduces the bonding strength due to uneven mating Cu interconnects at the interface. Also, must require

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high temperature and pressure for good quality bonding. But during high pressure application for Cu-Cu thermocompression bonding, there may be great chances of mechanical damage of delicate underneath Cu interconnects between stacked layers. On the other hand, application of high temperature during bonding not only increases thermal stress of overall system but also degrades the performance of underlying ultra-sensitive CMOS devices. Therefore, there is strong need of ultra fine-pitch Cu-Cu interconnect bonding at low temperature, low pressure and CMOS compatible for real multi-layer 3D IC or heterogeneous integration.

Several researchers have proposed various ways to prevent/ protect Cu interconnects from oxidation by passivating the Cu surface prior to Cu pad-to-pad thermocompression bonding. Also, some of the researchers have proposed to modify the Cu surface in order to activate the Cu atoms for interdiffusion at room temperature prior to Cu-Cu bonding. Bonding mechanism basically very simple and based on just surface activation between two similar and dissimilar materials. T.Suga *et.al.* proposed this Surface Activated Bonding (SAB) scheme [11], and primary requirement for successful accomplishment of this bonding mainly depends on cleanness of the Cu surface at atomic level [12], [13]. Another prime requirement of this bonding scheme is Ultra high vacuum (UHV) in the order of 10^{-8} torr. Mainly, Argon (Ar) bombardment on the Cu surface cleans the native oxide and helps in interdiffusion of Cu atoms during mating even at room temperature. But, application of Ar ion bombardment increases the surface roughness. Rough Cu surface can be smoothened by an additional process step of Chemical Mechanical Polishing (CMP) prior to Cu-Cu bonding [14], [15]. Since, stringent requirement of additional process step, atomically smooth Cu surface, and requirement of UHV during bonding makes the process very complex, costlier and not manufacturing worthy.

Furthermore, some of the researchers proposed to remove native oxide layer in order to enhance the interdiffusion of Cu atoms during thermocompression cycle just prior to Cu-Cu bonding. Removal of native oxide layer from Cu surface by pre-bond cleaning step using wet chemistry. Pre-bond cleaning was performed by using various chemicals but not limited to acetic acid [16], [17] citric acid [18], sulfuric acid [19], hydrochloric acid [20], [21] treatments and combinations thereof. But, prolonged immersion of samples inside strong acids may degrade the underneath active devices. Hence removal of native oxide prior to Cu-Cu bonding using pre-bond chemical treatment is not CMOS grade. Then, Tan *et.al.* proposed a non-UHV, non-corrosive method to passivate Cu surface effectively using self assembled monolayer (SAM) of alkane-thiol and its subsequent desorption by ion bombardment just prior to Cu-Cu pad-to-pad bonding [22]-[24]. But, main challenge in SAM based Cu surface passivation is complete removal of same must require higher temperature near to 250 ˚C [25]. To eradicate this recently we have reported a methodology to desorb SAM using electrochemical method and non-thermal plasma (NTP) and subsequent bonding was achieved at 200 ˚C [26]-[28]. However, all SAM based Cu surface passivation mechanism are ex-situ and cannot be easily integrated with in-line CMOS process flow. Alternatively, Chen *et.al.* proposed a novel wafer-level Cu-Cu bonding using Ti as the passivation layer on Cu surface at 180 ˚C and 1.91 MPa pressure by keeping eye on CMOS in-line process flow [29]. However, application of such a high pressure condition during bonding may damage the delicate underneath Cu interconnect and seriously affect the system performance. Also, the same research group proposed a noble metal based Cu surface passivation technique using Pd prior to wafer-level Cu-Cu bonding at low temperature (150 ˚C) and very high pressure of 1.91 MPa with superior electrical performance than Ti based Cu-Cu bonding [30]. But very high bonding pressure deviates from the need of low temperature and low pressure Cu-Cu bonding. Optimizing the deposition condition of passivation layer is the key in this metal based Cu surface passivation technique prior to the bonding. We have reported a low temperature (160 ˚C) and low pressure (0.25 MPa) wafer-level Cu-Cu bonding by systematically optimizing Ti passivation thickness layer of 3 nm is suffice for high quality wafer-level Cu-Cu bonding [31]. Furthermore, we have reported efficacy of Cu surface passivation with optimized Ti passivation layer [32]. However, consistence oxidation of Ti was observed in the literatures [33]. Also, metal Ti is not damascene process compatible. A better choice of surface passivation would be a material that is highly conductive, which is not oxidizable even at higher temperature (<300˚C) and is simultaneously CMOS damascene process compatible. Constantan, a Copper-Nickel alloy is an apt choice in this regards. It is reported that Constantan gets oxidized only at temperatures beyond 350˚C and miniscule oxidation happens at room temperature [34]. In our previous work, we have reported a low temperature and low pressure Cu-Cu Wafer-on-Wafer (WoW) bonding using ultra-thin metal-alloy, Constantan as passivation layer. We have demonstrated that a thickness of 2 nm of Constantan layer on Cu surface not only results in excellent bonding but also leads to a reduction in bonding temperature to 150 ˚C [35].

Blanket Wafer level Cu-Cu bonding has limited application as Cu is a conductive material and it will short circuit the devices fabricated on an active layer. In actual 3D integration, copper pad-to-pad bonding is required along with proper isolation among each active device layer using Inter Metal Dielectric (IMD). All Cu pads present on the wafer have to bond in order to ensure better mechanical strength and electrical connectivity. Therefore there is a strong need of precise alignment (±1 μm) prior to high quality WoW fine pitch bump-less Cu-Cu bonding. Towards this endeavor, in our present work a high quality fine-pitch (20 μm) bump-less Cu pad-to-pad bonding obtained with optimized Constantan passivation layer of 2 nm at sub 200 ˚C with a nominal contact pressure of 0.4 MPa. Fig. 1 shows schematic of bonding methodology. Furthermore, longevity of Cu surface passivation is studied using conventional wettability of the passivated Cu surface using optimized constantan passivation layer up to 600 hrs. In addition, electrical characterization is performed under various conditions.

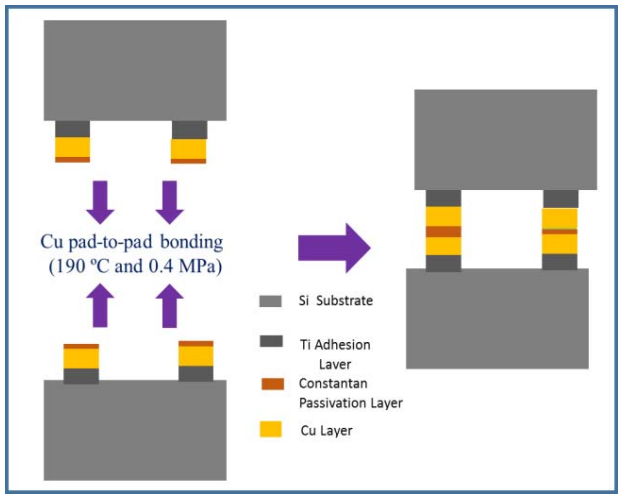

Figure 1. Schematic of Cu pad-to-pad bonding protocol with Optimized Constantan metal-alloy passivation.

II. EXPERIMENTAL

Using the proposed passivation mechanism, fine pitch (20 µm pitch) thermocompression bonding is demonstrated at sub 200 ˚C under mechanical pressure of 0.4 MPa. The following sections describe the methodology of carrying out the same starting from the mark preparation step.

A. Mask design for Cu pad-to-pad bonding

Mask Design was carried out carefully to simplify the task of aligning as much as possible. Symmetry was maintained along the center of the wafers to avoid any mirroring issues as shown Fig. 2. Complete 5 inch mask was sub divided into 16 dies (12 mm × 12 mm) mask design. Standard structures such as daisy chain structure with various pitch size (25 µm, 35 µm, and 55 µm), SEM line structures, grid structures, and mechanical stability structures, shown in Fig. 3, were incorporated in each die.

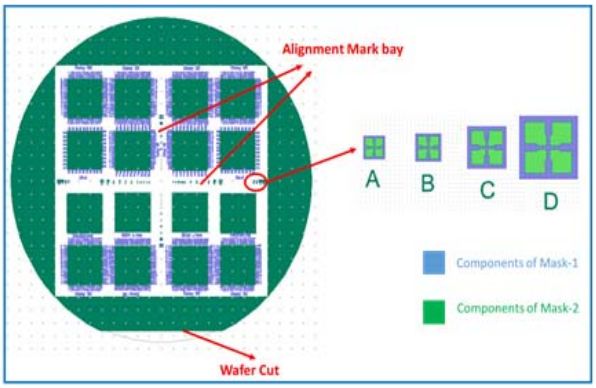

Figure 2. Schematic wafer level design of Mask-1 and 2 after complete alignment.

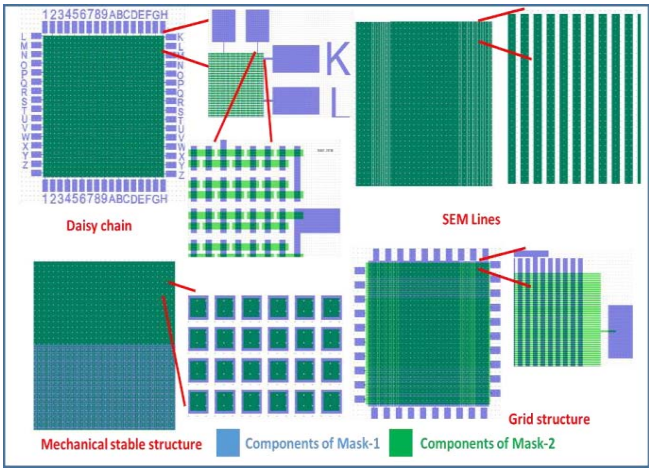

Figure 3. Die level design of major components after proper alignment.

B. Fabrication of fine pitch Cu-Cu bonding with optimized Constantan metal-alloy passivation

4 inch P-type <100> Double Side Polished (DSP) Silicon wafers were used for the whole experiments. The process flow comprises three steps viz., cleaning of wafers, patterning of metal thin film on the wafers and bonding the pair of wafers. Piranha cleaning followed by RCA-1 and RCA-2 was used to clean the wafers in order to remove all the contaminants prior to patterning of photoresist. Liftoff technique was adapted for patterning Cu. Photoresist AZ5214E was used in the image reversal mode. The required patterned were transferred onto silicon. This was followed by sequential deposition 20 nm of Ti film (Cu diffusion barrier/ adhesion layer), 185 nm of Cu film, followed by passivation layer of optimized ultra-thin Constantan of 2 nm thick. The whole wafers were immersed in acetone to complete the lift off process.

Post patterning, AML Wafer Bonder machine was utilized for bonding the wafer pair. Multiple cycles of nitrogen gas purging was carried out to expunge of oxygen from the chamber till a vacuum of 1E-5 mbar was achieved. In-situ wafer alignment was carried out with the help of IR lamp and microscope prior to bonding. After precise alignment of both the wafers, the platens were heated up to 190 °C. Once the desired temperature is achieved, a pressure of 0.4 MPa was applied for 50 mins. Bonded wafer was removed from the vacuum chamber after cooling down to room temperature for further bond interface analysis.

III. Results And Discussions

A. *Post paternning passivated Cu surface analysis prior to bonding*

In our previous work, we have optimized systematically Constantan passivation layer thickness of 2 nm on Cu film improves the surface smoothness and provides flat Cu surface during bonding. As well we have reported same thick constantan passivation layer is preventing Cu surface from oxidation effectively by XPS study. It is now imperious to study the same ultra-thin Constantan passivation layer can able to prevent Cu surface from oxidation or not and in the meantime increase any surface roughness after patterning of Cu interconnects. For this purpose, Post patterning surface analysis was carried out by Secondary ion mass spectroscopy (SIMS) depth profiling and atomic force microscopy to study the surface smoothness.

The wafers with varying passivation thickness (1 nm- 7 nm) of post patterned Cu/constantan pads were subjected to AFM measurements at tapping mode to validate smoothness of the patterned passivated Cu surface. Scan area size of 5×5 μm^2 for performing the AFM studies. Fig. 4 shows the RMS roughness variation of Cu/Constantan patterned surface for various thickness of Constantan alloy passivation. AFM micrograph clearly reveals the patterned Cu surface with 2 nm Constantan alloy is having comparably lower RMS roughness of 0.62 nm than other Cu surface passivated post patterned samples.

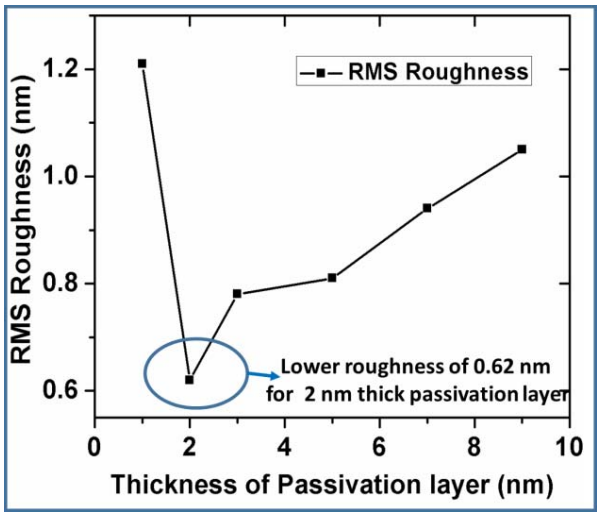

Figure 4. Variation of Post patterning RMS roughness with different constantan passivation thickness.

After figuring out the same passivation thickness can able to provide flat and smoother Cu surface after patterning, now it's really imperious task is to study either the same passivation thickness able to passivate the Cu surface effectively or not. For this purpose, we have performed SIMS depth profiling of post patterned 2 nm passivated Cu sample. There was a week' time delay between sample preparation (patterned sample) and analysis. Fig.5 clearly reveals miniscule oxygen intensity at the surface is indicative of successful Cu surface passivation.

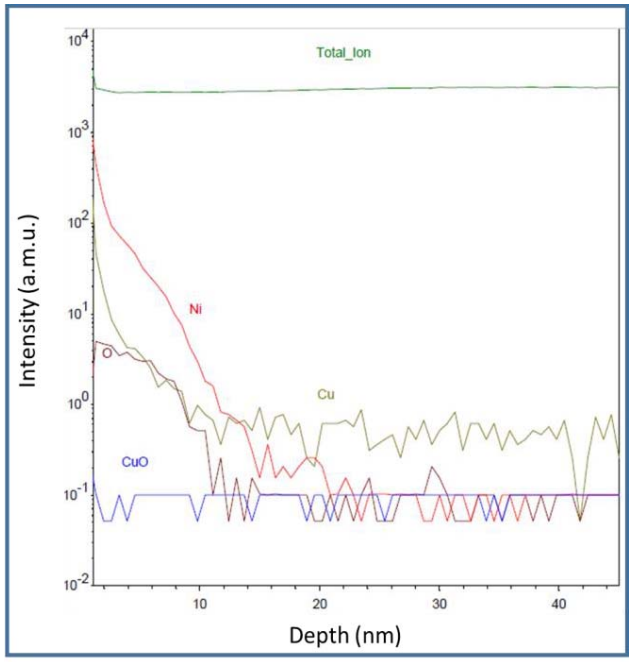

Figure 5. SIMS depth profiling shows negligible oxygen intensity (O_{1S}) at constantan passivation thickness of 2 nm on Cu surface.

B. *Microstructure Imaging of bonded sample*

Infra-red Wafer bonder inspection (IR-WBI) is one of the best qualitative technique to evaluate the interface quality, misalignment, yield of the bonded Cu pads. It is well equipped with infra-red source and adjustable camera. The property of infra-red source easily allows through the Si wafer and blocks through the bonded metal patterns which helps to judge interface quality. If the Cu pad-to-pad bonding is not proper and mechanically unstable then infra-red signal easily pass through. Fig. 6 shows the WBI-IR imaging of 4 ″ bonded sample having 2nm Constantan as passivation layer. Fig. 7 shows highly resolution zoomed version at particular area of the bonded sample. Furthermore, Fig. 8 shows high resolution zoomed version of the die containing 20 µm pitch daisy chain electrical structures. No substantial defects at any particular area of the daisy chain, no breakage at the chain, no twin defects were observed from the WBI-IR images which clearly ratifies that Cu-Cu bonding with ultra-thin optimized Constantan alloy is high quality and reliable.

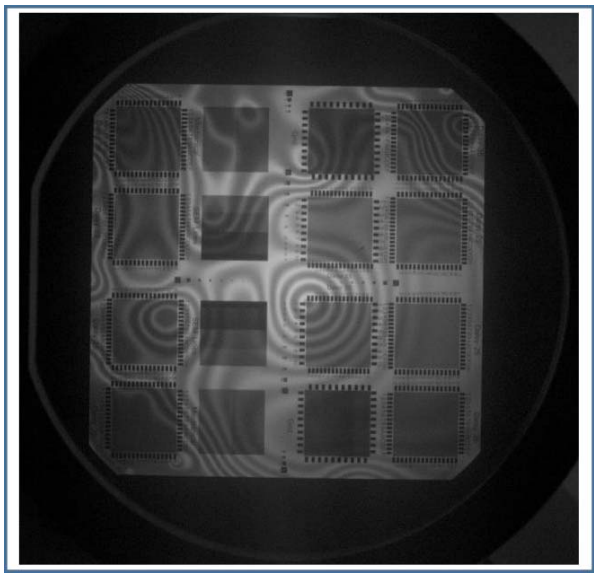

Figure 6. IR-WBI imaging of the complete 4″ fine-pitch bump-less Cu-Cu bonded sample with optimized constantan alloy passivation of 2 nm.

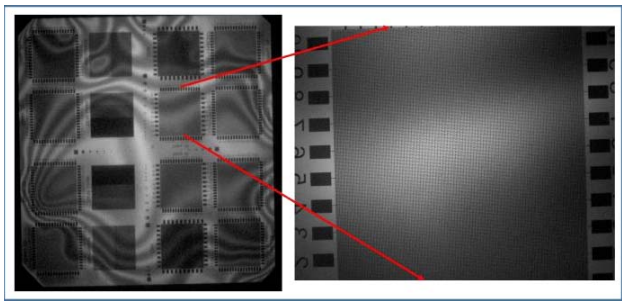

Figure 7. IR-WBI imaging of the high resolution zoomed version of the particular die.

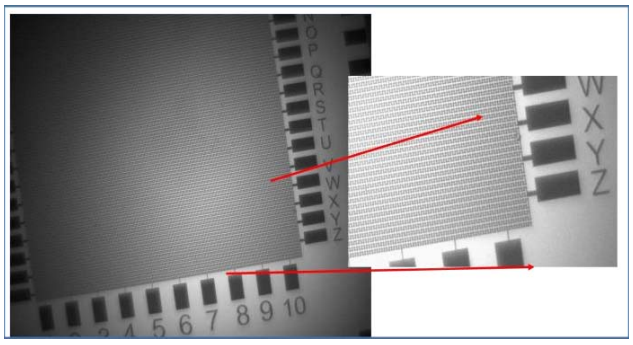

Figure 8 (a). IR imaging of the daisy chain die, (b) high resolution IR imaging of the marked region of figure 8 (a).

C. Bond strength analysis of the Cu pad-to-pad fine-pitch bonded samples

Bond strength plays vital role in order qualitatively analyze the bonding quality. In order to analyze the preliminary bond strength of the constantan passivated Cu-Cu bonded sample razor test was performed. The bonding quality between Cu interconnects were tested primarily using simple razor test and absence of any razor inset at the bonded interface is the initial proof of high quality and reliable bonding.

Furthermore, we have performed bond strength measurement of the 4″ constantan passivated bonded sample using micron tester which is basically shear test. For this purpose, we have diced the 4″ bonded sample into 1 cm^2 pieces using diamond scriber. Also, this is another pre-judgement of high quality bonding even after application of such an uneven high force was not able to separate bonded sample. Then the shear test was performed on those diced samples using micron tester tool. Fig. 9 shows bond strength of 163 MPa (755 N) which is comparably better than the existing reported literatures.

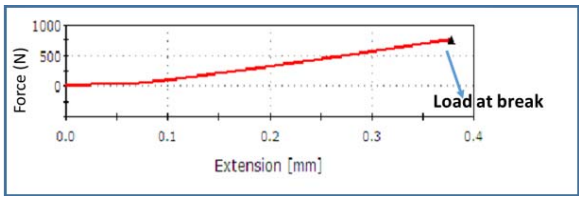

Figure 9. Bond strength qualification.

IV. CONCLUSION

Low temperature (Sub 200 ˚C), low pressure (0.4 MPa), bump-less, ultra fine-pitch, high quality Cu-Cu thermocompression bonding was successfully confirmed using ultra-thin optimized Constantan alloy of 2 nm. Very high bond strength of 163 MPa and defect free interface observed by WBI-IR clearly suggests, Cu-Cu fine- pitch (20 µm) bonding with optimized ultra-thin alloy of 2 nm thick constantan, is of very high quality and reliable.

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