Modeling and Simulation of Negative Capacitance MOSFETs

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Master of Technology

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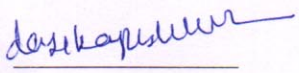

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Approval Sheet

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Dedication

Dedicated to all my teachers and parents who have imparted knowledge to me

Abstract

The current and voltage characteristics of a MOSFET device are maily characterized by the source to channel barrier which is controlled by the gate voltage. The Boltazmann statistics which govern the number of carriers that are able to cross the barrier indicates that to increase the current by a decade, atleast 60 mV of rise in gate voltage is required. As a result of this limitation, the threshold voltage of modern MOSFETs cannot be less than about 0.3 V for an I_{ON} to I_{OFF} ratio of 5 decades. This has put a fundamental bottleneck in voltage downscaling increasing the power consumption in modern IC based chips with billions of transistors.

Sayeef Salahuddin and Supriyo Dutta proposed the idea of including ferroelectric in MOSFET gate stack which allows an internal voltage amplification at the MOSFET channel which can be used to achieve a smaller subthreshold swing which would further reduce the power consumption of the devices. In this thesis we have undertaken a simulation based study of such devices to study how the inclusion of negative capacitance ferroelectrics leads changes in various device characteristics.

Initially we have taken a compact modeling based approach to study device characteristics in latest industry standard FinFET devices. For this purpose we have used the BSIM-CMG Verilog A model and modified the model appropriately to include the effect of negative capacitance ferroelectric in the gate stack. This simulation allowed us to observe that negative capacitance (NC) devices can indeed give a subthreshold swing lesser than 60 mV/dec. Further other interesting properties like negative output resistance and drain induced barrier rising are observed.

Using the compact models developed above, we have analyzed some simple circuits with NC devices. Initially an inverter shows a hysteresis in the transfer characteristics. This can be attributed to negative differential resistance. Ring oscillator analysis shows that RO frequency for NC devices is lesser than that of regular devices due to enhanced gate capacitance and slower response of ferroelectrics.

Scaling analysis has been performed to see the performance of NC devices in future technologies. For this we used TCAD analysis coupled with Landau Khalatnikov equation. This analysis shows that NC devices are more effective in suppressing short channel effects like DIBL and can hence be used for further downscaling of the devices.

Finally we develop models to take into account the multidomain Landau equations for ferroelectric into account. We have performed such an analysis for a ferroelectric resistor series network. A similar analysis is performed for short channel double gate MOSFET without inter layer metal between ferroelectric and the internal MOS device. This analysis showed that coupling factor between ferroelectric domains plays an important role in the device characteristics.

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Chapter 1

Introduction

The power consumed by modern digital circuits is roughly given by $P = fCV_{DD}^2$ where C is the capacitance at the output node, f is the frequency of operation while V_{DD} is the supply voltage. With reduction in device dimensions according to Dennard scaling rules [1], the capacitances of the devices have reduced promising lesser power consumption. However the supply voltage V_{DD} could not be scaled according to the scaling rules, manifesting itself as a bottleneck in achieving high speed low power devices. This is due to the the fact that carriers in source and drain region of the MOSFET are governed by Boltzmann statistics which limits the rate of increase of drain current with respect to voltage to 60 mV/dec. In this report we explore the idea of negative capacitance in gate stack of MOSFETs to overcome the Boltzmann limit ($S_B = 60$ mV/dec) in order to realize high frequency low power devices.

1.1 Subthreshold swing

Subthreshold swing (SS) is defined as inverse slope of the $\log_{10} I_D$ vs V_{GS} curve.

$$SS = \left(\frac{\partial(\log_{10} I_D)}{\partial V_{GS}} \right)^{-1} \tag{1.1}$$

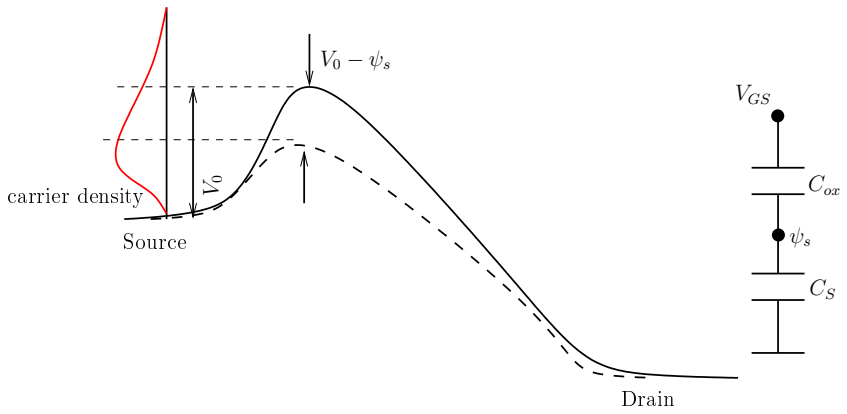
The origin of subthreshold swing is illustrated in Fig. 1.1 [2]. Since only carriers with kinetic energy greater than the barrier can be injected into the channel, the current in this situation can be written in the form of diode current

$$I_D = I_0 \left(e^{q\psi_s / k_B T} - 1 \right) \tag{1.2}$$

From Eq. 1.2 we can write, $n^{-1} = \frac{\partial(\log_{10} I_D)}{\partial \psi_s} = \frac{q \log_{10} e}{k_B T}$. At room temperature n turns out to be 60 mV/dec. The channel potential ψ_s is coupled to V_{GS} by a capacitive network as shown in Fig. 1.1b. By simple series capacitor formula we can write $m^{-1} = \frac{\partial \psi_s}{\partial V_{GS}} = \left(1 + \frac{C_S}{C_{ox}}\right)^{-1}$ where C_{ox} is the oxide capacitance and C_S is the semiconductor channel capacitance. Subthreshold swing is then given by

$$SS = m \times n = 60 \text{ mV/dec} \left(1 + \frac{C_S}{C_{ox}}\right) \tag{1.3}$$

Since capacitances are always positive, $m > 1$ which implies $SS > 60$ mV/dec. In order to



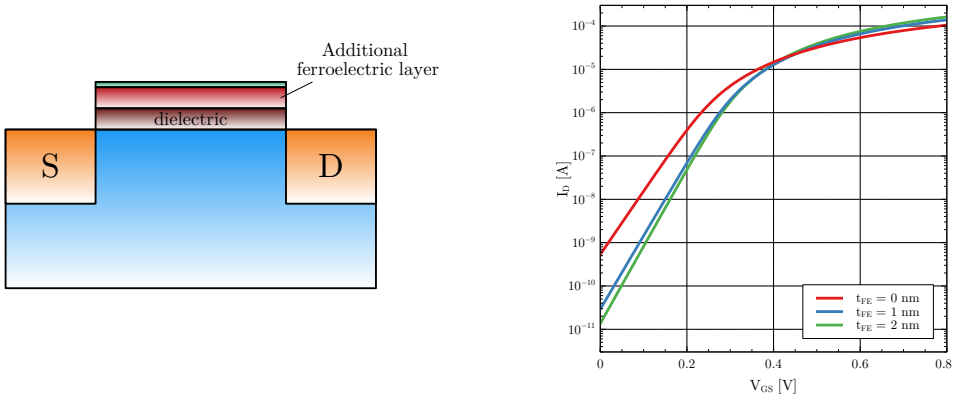
(a) (b)

Figure 1.1: Origin of subthreshold swing (a) Band diagram along the channel of MOSFET. The barrier height is modulated by V_{GS}. Only carriers above the barrier can be injected to channel (b) Gate is coupled to channel potential ψ_s by a capacitive network

maintain I_{ON}/I_{OFF} ratio of more than 10^6 for reasonable noise margins, we need a minimum supply voltage of 360 mV

A lot of effort has been put in optimizing electrostatics to minimize m to unity so as to get SS reasonably close to 60 mV/dec. However in order to push the limits of n, new FETs employing different carrier mechanisms like Tunnel FETs (TFETs) or Impact Ionization FETs (IIFETs) have been proposed.

Datta and Salahuddin [3] however proposed a novel idea, wherein an oxide material is used such that $C_{ox} < 0$. This allows $m < 1$ which can give a subthreshold swing of $SS < 60$ mV/dec. The advantage with this method is that it allows the use of existing fabrication flow with only addition of an additional oxide layer deposition which can provide the negative capacitance effect. Typical structure and characteristics of the device are shown in Fig. 1.2



(a) (b)

Figure 1.2: Ferroelectric based negative capacitance MOSFET (a) Conventional MOSFET with additional ferroelectric layer can can show negative capacitance effect (b) Input characteristics of 14 nm FinFET showing an improvement in subthreshold swing (SS) as well as on current I_{ON} with increasing ferroelectric thickness t_{FE}

1.2 Negative capacitance in ferroelectrics

A capacitor has a negative capacitance (in a differential sense), when $C = \frac{dQ}{dV} < 0$. This means that when charge across it increases, the voltage across it decreases. As a consequence, higher charge in semiconductor would require lesser supply voltage when a negative capacitance device is used with a FET.

Negative capacitance can be achieved using a ferroelectric in series with some other circuit element. The origin of such a negative capacitance lies in an interplay between thermodynamics and electrostatics. This is discussed in following subsections.

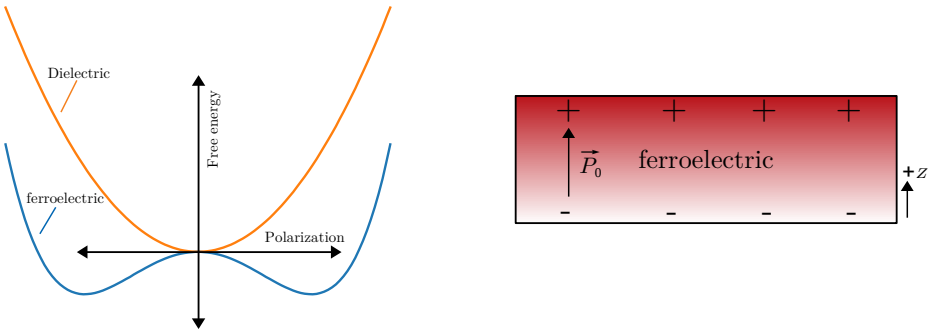
1.2.1 Origin of permanent polarization in ferroelectrics

In an ionic crystal, lattice vibrations can create can create an effective charge separation in a unit cell giving a net dipole moment to the unit cell. For long wavelength phonon modes ($k \to 0$) such an effective separation, u would be nearly same in all unit cells. In such a case the polarization of the material is given by $P = Nq^*u$ where q^* is the effective charge involved in the charge separation and N is the number of unit cells per unit volume. Such polarization would create a local electric field $E_{loc} = \frac{\gamma P}{3\epsilon_0}$ even in in the absence of external electric field. Here γ is called the Lorentz correction factor and is equal to 1 for isotropic cubic systems. Electrostatic potential energy of the crystal is then given by $F_{ES} = -E_{loc} \cdot P = -\frac{\gamma P^2}{3\epsilon_0}$.

The elastic energy is $F_{EL} = ku^2 + k_1u^4$. Using $u = P/Nq^*$, total potential energy would be given by [4]

$$F = \left(\frac{k}{N^2q^{*2}} - \frac{\gamma}{3\epsilon_0}\right)P^2 + \frac{k_1}{N^4q^{*4}}P^4 \equiv \alpha P^2 + \beta P^4 \tag{1.4}$$

In dielectrics elastic energy is dominant giving $\alpha > 0$, while in a ferroelectric, the electrostatic component is dominant giving $\alpha < 0$. This results in a double well potential profile in ferroelectrics with a stable state corresponding to non zero permanent polarization, in contrast with dielectrics as shown in Fig. 1.3



(a) (b)

Figure 1.3: Dielectrics and ferroelectrics (a) Free energy of ferroelectrics have a double well profile in contrast to dielectrics (b) Ferroelectric with open surface and finite polarization

1.2.2 Origin of negative capacitance effect

Continuing from the previous discussion, the free energy of a ferroelectric is given by

$$\mathcal{F} = \alpha P^2 + \beta P^4 + \beta P^6 - E_z P_z \tag{1.5}$$

where the last term indicates the dipole energy due to electric field. The dynamics of ferroelectrics in diffusive limit are given by Landau - Ginzburg equation

$$\rho \frac{\partial P_z}{\partial t} = -(\alpha P_z + \beta P_z^3 + \gamma P_z^5 - E_z \cdot P_z) \tag{1.6}$$

where we have considered only the z component of the polarization. Under steady state $\frac{dP_z}{dt} = 0$ and we can write

$$E_z = \alpha P_z + \beta P_z^3 + \gamma P_z^5 \tag{1.7}$$

Hysteresis characteristics and free energy profile are shown in Fig. 1.4

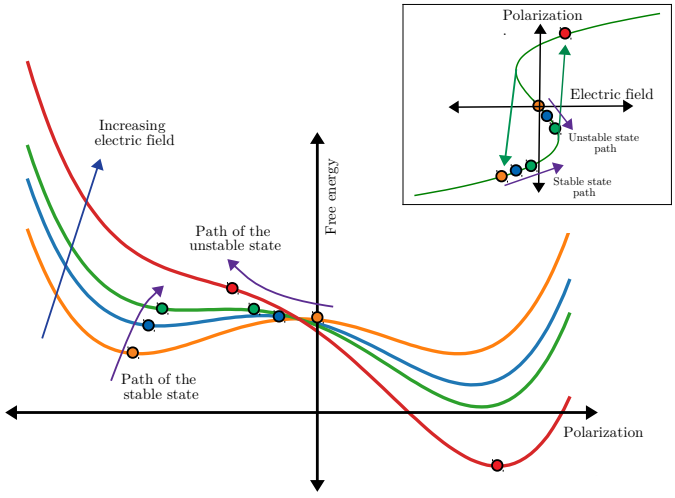


Figure 1.4: Ferroelectric energy profile with respect to polarization. The inset shows the hysteresis curves as obtained from Landau - Ginzburg theory

Negative capacitance in ferroelectrics arises due to high depolarizing fields, especially in situations where the surface polarization charge is not compensated by external charges. Consider for example an open circuited ferroelectric shown in Fig. 1.3b. In such a situation under no external electric field, saturation polarization is not stable since an uncompensated surface charge would create a large depolarizing field which would tend to realign the dipoles to the opposite direction. Once reoriented the same problem occurs again as depolarizing field always acts opposite to that of crystal polarization. The only stable state for which this problem does not occur is $P_z = 0$. However in presence of say short circuited ferroelectric the metal electrodes can quickly provide a compensation charge so that the net electric field is zero inside the ferroelectric.

Now consider the case when a small positive electric field is applied to the crystal. In usual dielectrics, dipoles are then oriented along the electric fields. Although the depolarizing fields tends to re orient the dielectric polarization, the stronger elastic forces hold them together. In ferroelectrics

however any small polarization would enhance the local electric field E_{loc} further increasing the depolarizing field which again gives rise to an instability. However if dipoles are oriented in negative direction, the local electric field at a dipole can be made smaller as $E_{loc} = E_{ext} - \frac{P}{\epsilon_0} + \frac{\gamma P}{3\epsilon_0}$. Since $\gamma \approx 10$ [5] in ferroelectrics, a negative polarization along the surface would stabilize the system by reducing the local electric field. Hence application of a positive electric field can lead to negative surface charges, which indicates a negative capacitance.

The origin of negative capacitance has also been often discussed in relation to thermodynamic system. Capacitance of a system can be written in terms of energy as

$$C^{-1} = \frac{d^2U}{dQ^2} \tag{1.8}$$

As can be seen from Fig. 1.3, ferroelectrics have a concave down curvature at $P = 0$ which can be inferred as negative capacitance.

1.3 Thesis objective

In this thesis, we study and analyse the ferroelectric based negative capacitance MOSFETs at device level and circuit level. Our main objective is to model and simulate the ferroelectric negative capacitance devices using physics based models. Using these models, our objective is to predict and analyse the characteristics of the state of the art devices with the additional negative capacitance ferroelectric in the gate stack.

1.4 Organization of the thesis

This thesis is organized as follows. Chapter 2 gives a brief review of the latest findings in the negative capacitance devices. Chapter 3 describes the performance of modern logic devices with negative capacitance effect. Chapters 4 describes the performance and scalability of NC devices while Chapter 5 describes the phase field modeling and device performance taking into account multidomain nature of ferroelectrics. Chapter 6 provides conclusion and future scope for work.

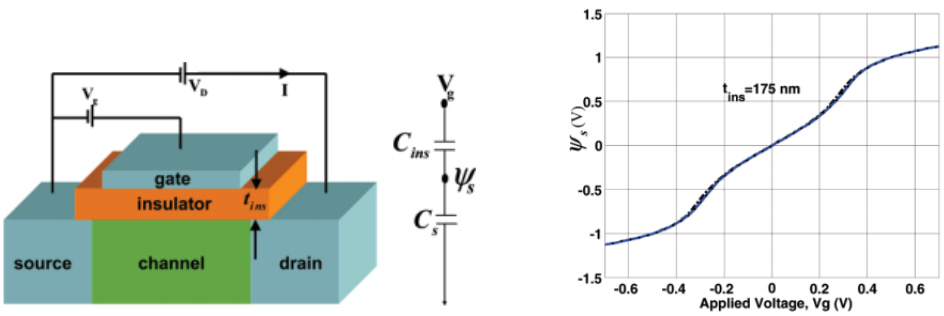
Chapter 2

Literature Review

In this chapter we review the latest findings in the domain of negative capacitance FETs. We begin with a review of development of the idea of the NC MOSFETs, and their future prospects in a theoretical perspective. Then we look at various experimental realizations of negative capacitance MOSFETs. Finally we review the latest developments in modeling of NCFETs with additional physical effects like multi domain nature of ferroelectrics and leakage in ferroelectrics.

2.1 Development and prospects of NCFETs

Datta and Salahuddin [3] proposed the idea of negative capacitance MOSFETs to achieve $SS <$ 60 mV/dec, wherein a ferroelectric insuator is used as gate oxide and provides step up voltage transformation. Further they argued that for the system to stable in its totality the capacitance of



(a) (b)

Figure 2.1: Idea of negative capacitance devices proposed by (a) Ideal device structure employing ferroelectric insulator (b) Amplification of surface potential observed with a $BaTiO_3$ of thickness 175 nm [3]

the system should be positive. This poses a fundamental limit on the maximum thickness of the ferroelectric for hysteresis free operation given by

$$t_{fe} < \frac{1}{2|\alpha|C_S} \tag{2.1}$$

where α is the material property of the ferroelectric and C_S is the semiconductor capacitance.

In [6] design guidelines for designing NC-MOSFETs are given. They showed that for stable operation, the total capacitance of the system should be positive, and hence $C_S^{-1}(Q) > C_{ins}^{-1}(Q)$ throughout the region of operation of the device. Further for minimum coupling factor m, C_S and ferroelectric capacitance $-C_{ins}$ should be as close as possible, since $m = \frac{C_S^{-1}+C_{ins}^{-}1}{C_S^{-1}}$. For ferroelectric FET operating in stable region, they showed that the minimum subthreshold swing is given by

$$SS_{min} = \frac{2.3k_BT}{q}\left(1 + \frac{M}{y_0}\right) \tag{2.2}$$

where $M = (2\phi_t(\alpha Q_{C1} + \beta Q_{C1}^3 + \gamma Q_{C1}^5)/(2\alpha^2 Q_{C1}^2)$, $y_0 = \sqrt{\frac{4\phi_f\phi_t}{\alpha^2 Q_{C1}^2}}$ and Q_{C1} is the solution of the equation $5\gamma Q_C^4 + 3\beta Q_C^2 + \alpha = 0$.

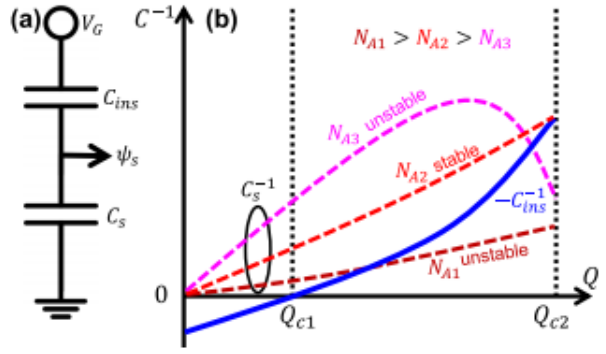
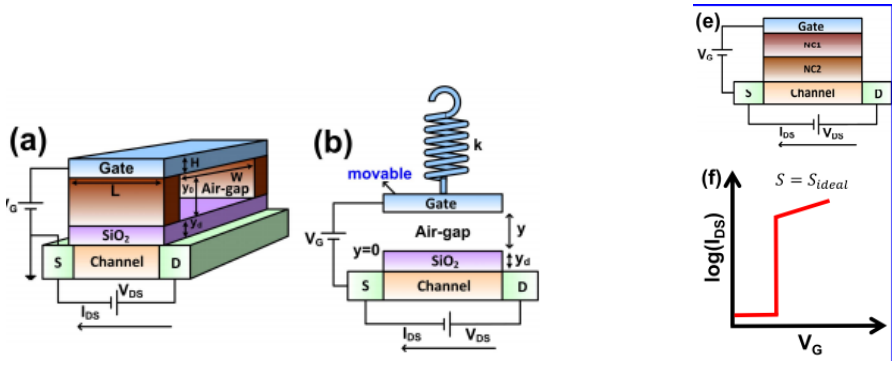


Figure 2.2: Stable operation of NCFETs requires $C_S^{-1}(Q) > C_{ins}^{-1}(Q)$. This is satisfied only for the doping concentration of N_{A2} and hence it would be operating in hysterisis free mode [6]

Other implementations of NCFETs have been discussed in [7, 8]. In particular the nano electro mechanical switch (NEMS) with suspended gate can also provide the negative capacitance effect. As the suspended gate is charged, it is attracted towards the MOSFET and consequently the voltage across it decreases. The NEMS switch can be then used in series with the ferroelectric capacitor to provide an ideal logic switch with $SS = 0$ mV/dec

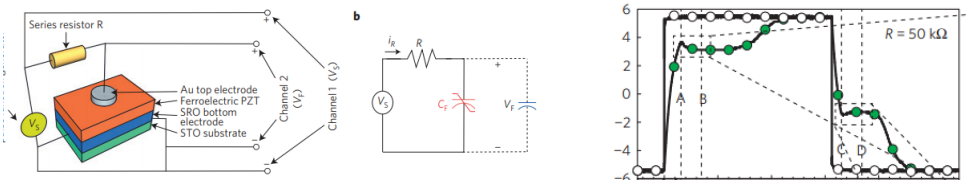


(a) (b)

Figure 2.3: Suspended gate and ideal logic switch (a) A suspended gate NCMOS with an nano mechanical spring (b) SG technology can be used in series with ferroelectric insulator to provide an ideal logic switch by providing a dual energy landscape [7, 8]

2.2 Experimental evidence of NCFETs

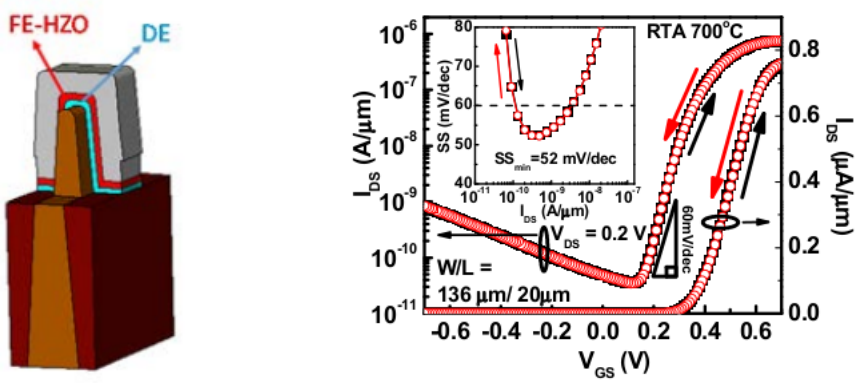
Experimental evidence of NC mechanism has been first provided by A.I.Khan and Salahuddin [9]. In this experiment they connected a ferroelectric capacitor in series with a high resistor. The flow of screening charges from battery is then hindered by the resistance and a transient negative capacitance is observed, where in the charge across the ferroelectric decreases even though the voltage across it increases.



(a) (b)

Figure 2.4: Verification of negative capacitance (a) Ferroelectric capacitor connected in series with a resistor to demostrate NC effect (b) Resistance hinders the flow of screening charges which results in a transient NC effectbetween points A and B [9]

Experimental evidence of FE-FinFETs have been discussed in [10]. In particular in 1.5 nm thickness HZO (Halfnium Zincronium Oxide) was used to achieve a subthreshold swing of about 52 mV/dec.



(a) (b)

Figure 2.5: Experimental evidence of FE-FinFETs (a) Device structure showing a thin 1.5 nm layer of HZO as ferroelectric (b) A minimum subthreshold swing of 52 mV/dec is observed without hysterisis [10]

2.3 Modeling NCFETs

The basic methodology to model the performance of NCFETs has been including an additional insulating layer governed by Landau Khaltnikov equation,

$$V_{FE} = 2\alpha Q + 4\beta Q^3 + 6\gamma Q^5 \tag{2.3}$$

and then solve the MOS equation

$$V_G = V_{FE} + \psi_s + \psi_{ox} + V_{FB} \tag{2.4}$$

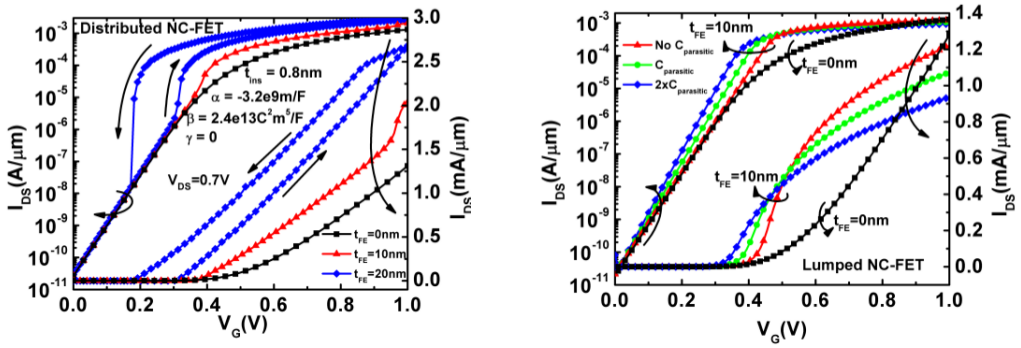
self consistently. If the ferroelectric is connected through a metal, Eq. 2.3 is homogeneous throughout the length of the ferroelectric and can be solved easily. However if the ferroelectric is connected directly to the dielectric insulator, Eq. 2.3 has to be solved at each point along the length of the ferroelectric self consistently as is done in [11].

A compact model compatible with BSIM-CMG model has been proposed in [12]. In this work the core BSIM-CMG model is extended by an additional term $v_{FE} = -(a_0 q_{ch} + b_0 q_{ch}^3 + c_0 q_{ch}^5)$ so that it becomes

$$v_G - v_0 - v_{FE} = -q_m - ln(q_m) - ln\left(\frac{e^{q_t}}{e^{q_t} - q_t - 1}\right) \tag{2.5}$$

where q_m and q_t are normalized mobile and total charges which are specified for different geometries of multi gate FETs. This model can also be used without lumped metal by solving the equation self consistently at n points along the channel so that

$$i_{DS} = \sum_{i=1}^{i=n} q_{ch} dv_{ch} \tag{2.6}$$



(a) (b)

Figure 2.6: Performance of different NCFETs (a) In lumped NCFET the ferroelectric capacitor can be considered a separate series element (b) In distributed model, KVL and LK equations need to be solved self consistently at each point along ferroelectric and in general shows better characteristics due sustained NC effect at different regions of the ferroelectric [12]

The non ideal phenomena of leakage through the ferroelectric has been studied in [13]. The leakage is modeled as resistor parallel to ferroelectric capacitor. The resistor provides an additional path to provide screening charges to ferroelectric degrading its performance. A solution is also provided by changing the metal work functions appropriately. With appropriate work function selection, the point where ferroelectrics go into negative capacitance regime is decreased. This also reduces the leakage, as leakage has been modeled as a resistance ($I = V/R$)

Multidomain nature of ferroelectrics is taken into account in [14] where NEGF formalism has been used to get the device characteristics. An additional term of $\kappa\left(\frac{dP_z}{dx}\right)^2$ has to be added to Eq.

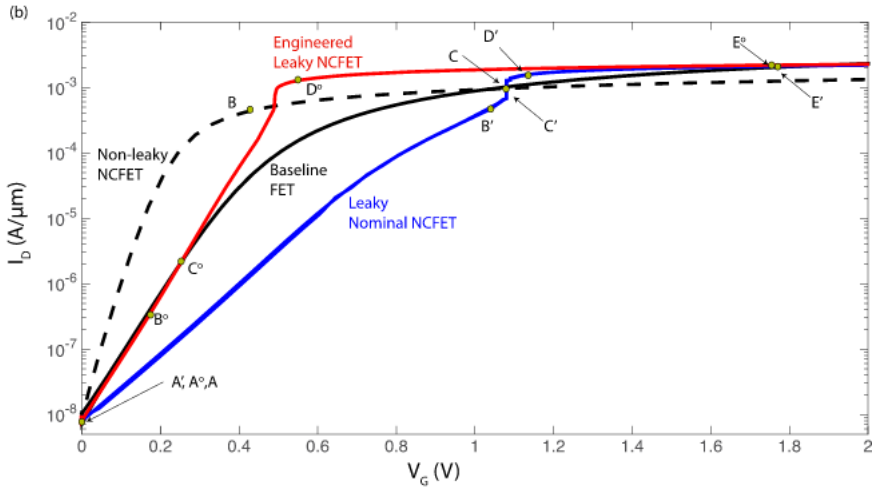
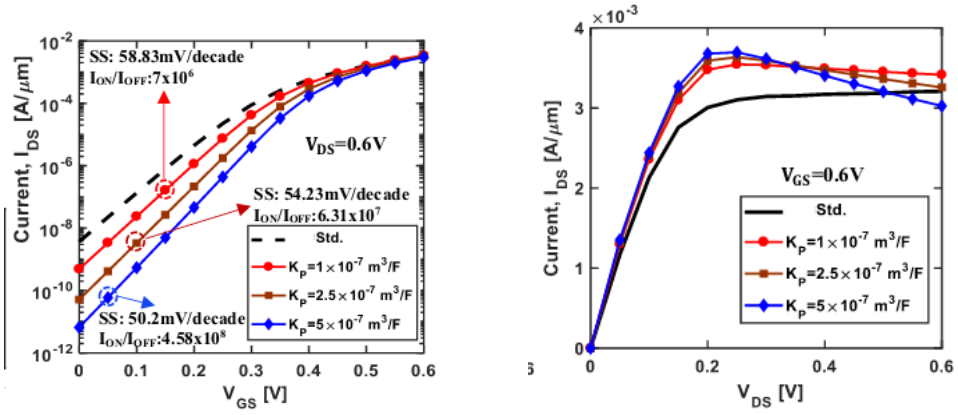


Figure 2.7: Leaky ferroelectrics can degrade the performance of NCFETs. Appropriate workfunction is required to restore the performance of the device [13]

1.5 to account for variation in polarization in ferroelectric. This gives us an equation of state

$$E_z = \alpha P + \beta P^3 + \gamma P^5 - \kappa \frac{\partial^2 P_z}{\partial x^2} \tag{2.7}$$

The κ factor is shown to provide a coupling between the polarization in different regions of ferroelectric. Higher values of κ are shown to make the ferroelectric polarization more uniform and even the MFIS structure tends to become MFMIS structure.



(a) (b)

Figure 2.8: Multidomain behavior of NCFETs (a) Increasing coupling factor κ makes the MFIS structure more towards MFMIS structure and increases SS (b) Negative output capacitance is observed in NCFETs [14]

Chapter 3

DC modeling of NCFETs

In this chapter we discuss the quasistationary performance of NCFET devices. First we present a compact model which we integrate with the industry standard BSIM-CMG model to study negative capacitance based FinFETs. We observe a subthreshold swing of less than 60 mV/dec and a negative output conductance in this study. Then we present an analytical DC compact model for double gate ferroelectric based FET.

3.1 NCFET analysis using compact models

Using NCFETs in future technology nodes for circuit design would require the need for efficient compact models which can capture the accurate device physics as well as the terminal characteristics efficiently.

In this study we use the mono domain Landau - Khalatnikov equation to model the ferroelectric. This equation is given by

$$\rho \frac{dP}{dt} = -\frac{dU}{dP} \tag{3.1}$$

Here P is the polarization of the ferroelectric, U is the Gibb's free energy and ρ is the diffusion constant which depends on the ferroelectric chosen. The Gibb's free energy is usually expanded in Taylor series as

$$U = \alpha P^2 + \beta P^4 + \gamma P^6 - E_{FE} P \tag{3.2}$$

Here E_{FE} is the electric field across the ferroelectric. Substituting the above equation in Eq. (3.1).we get

$$\rho \frac{dP}{dt} = -(2\alpha P + 4\beta P^3 + 6\gamma P^5 - E_{FE}) \tag{3.3}$$

Under steady state conditions, $\frac{dP}{dt} \approx 0$. Using the fact that $E_{FE} = V_{FE}/t_{FE}$, we finally get

$$V_{FE} = t_{FE}(2\alpha P + 4\beta P^3 + 6\gamma P^5) \tag{3.4}$$

In the above equation, P is the polarization and is given by $P = Q - \epsilon_0 E_{FE}$, where Q is the electrode

charge per unit area. However in the present case we assume an ideal metal ferroelectric contact, so that there are negligible depolarization fields, which allows us to approximate $P \approx Q$. Using this we can finally write the DC equation for ferroelectric capacitor as

$$V_{FE} = t_{FE}(2\alpha Q + 4\beta Q^3 + 6\gamma Q^5) \tag{3.5}$$

This equation infact corresponds to a non linear capacitor. When connected in series with another capacitive device (such as a MOSFET), the total charge across the both devices should be same, i.e

$$Q_{MOS} = Q_{FE} \tag{3.6}$$

The equivalent circuit for the ferroelectric MOSFET combination is shown in Fig. 3.1 The presence

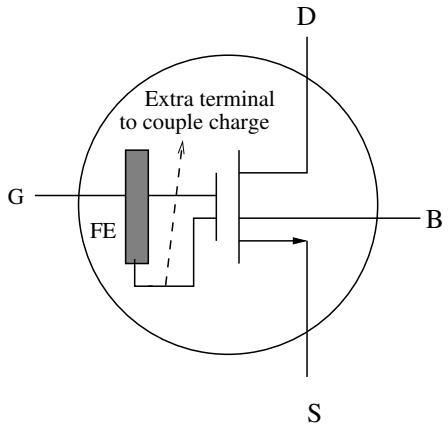


Figure 3.1: Equivalent circuit model for a metal-ferroelectric-metal semiconductor MOSFET

of an intermediate metallic layer is crucial for this model as the intermediate metallic layer brings the bottom surface of the ferroelectric to same potential and charge. Hence the Eq. 3.5 can be used directly. Otherwise since under bias the potential drop accross the MOSFET is not uniform across the channel, Eq. 3.5 has to be solved at each point in the channel self consistently. Also the present model does not take into account the 3D effects of the ferroelectric gate stack. Rather we model the ferroelectric gate stack as a 1D device that is coupled to the underlying FinFET. The equivalent physical structure and the simulated structure are shown in Fig. 3.2. This structure although is not completely physical it has also been investigated in experimental works, where a FinFET is externally connected to a ferroelectric capacitor without physical integration [15].

The underlying MOSFET has been simulated using the industry standard BSIM - CMG model [16]. Simulation has been done using Cadence Verilog A simulator. The ferroelectric model has also been implemented in Verlog A to integrate it with the BSIM model.

For the FinFET parameters from ASU predictive technology models for 14 nm technology [17]. Halfnium Zincronium Oxide (HZO) has been used as ferroelectric material and parameters are chosen as given in [18]. These values are tabulated in Table. 3.1

3.1.1 Results and analysis

Input characteristics of the device for various ferroelectric thickness are shown in Fig. 3.3

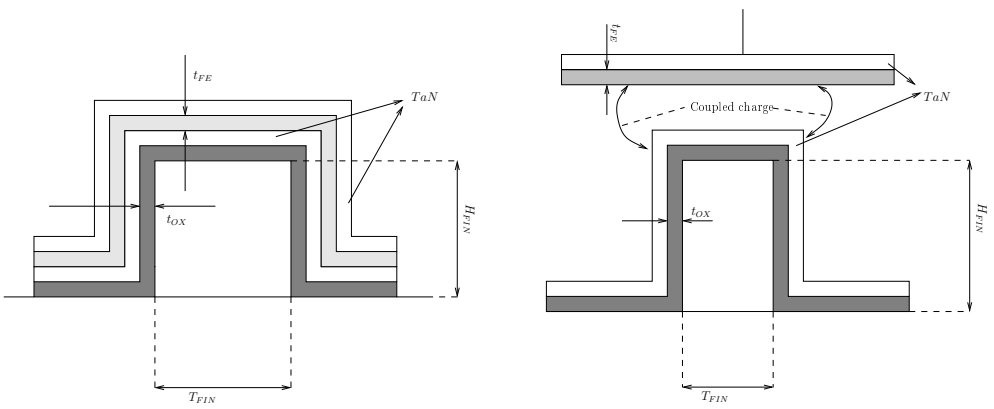


Figure 3.2: Structure of negative capacitance MOSFETs. (a) Actual FinFET structure with an intermediate metal layer (b) Simulated structure which uses a 1D model for the ferroelectric capacitor with charge coupling between the devices.

Table 3.1: Parameters considered for simulation

Parameter	Value
α	$-6.8 \times 10^{10}\ cm/F$
β	$-6.8 \times 10^{20}\ cm^5/F \cdot C^2$
γ	$85 \times 10^{29}\ cm^9/F \cdot C^4$
ρ	$100\ cm \cdot s/F$
t_{FIN}	10 nm
H_{FIN}	23 nm
L_G	30 nm
t_{ox}	0.61 nm

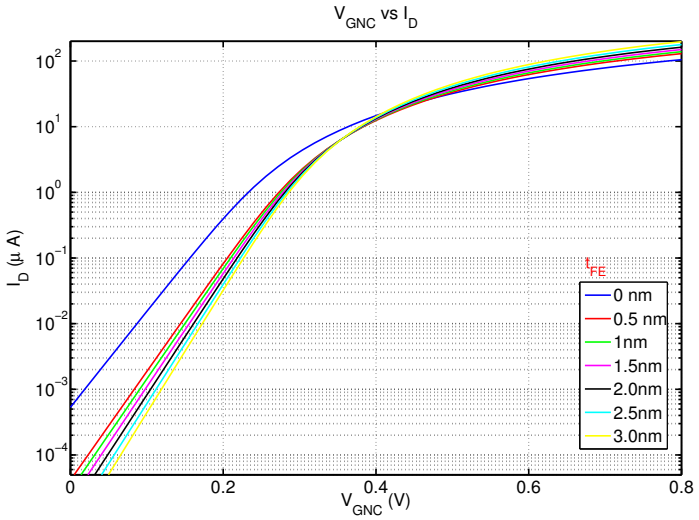


Figure 3.3: Input characteristics of the device for various ferroelectric thickness. Increasing ferroelectric thickness leads to smaller subthreshold swing

The effect of increasing the ferroelectric thickness can be explained as follows. For small Q (in subthreshold) from Eq. 3.5, $dV_{FE} \approx 2t_{FE}\alpha\ dQ$. Since $\alpha < 0$, this implies that for larger ferroelectric

thickness, a small change in MOS charge would lead to larger decrement in ferroelectric voltage. Since voltage follows KVL, this should lead to larger drop across the MOS device giving better subthreshold characteristics.

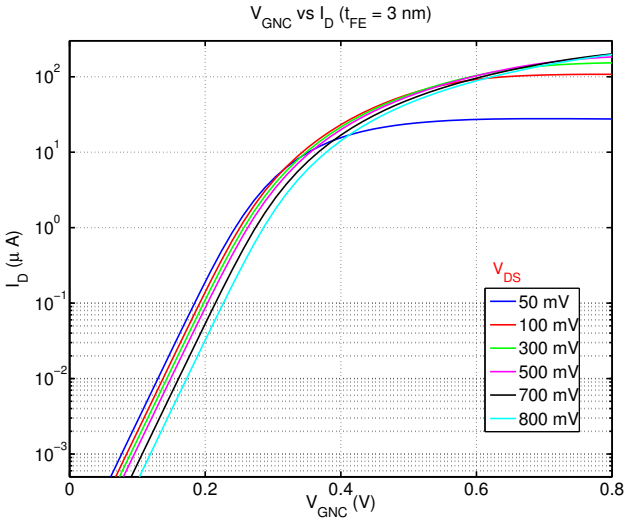


Figure 3.4: Input characteristics of the device for various drain voltages. Negative drain induced barrier lowering can be observed from the characteristics

The input characteristic variation with various drain voltages is presented in Fig. 3.4. A negative drain induced barrier loweing is observed in this plot. As opposed to usual case, wherein the threshold voltage decreases with increasing drain voltage, here the threshold voltage decreases with decreasing drain voltage. A DIBL of -42 mV/V has been observed.

A negative drain induced barrier can be explained as follows. An increase in the drain voltage V_{DS} leads to decrement of the total gate charge due to drain to channel coupling modeled by the capacitor C_D. This reduction in gate charge the in turn leads to increment in ferroelectric voltage since it is operating in negative capacitance. An increase in ferroelectric voltage naturally leads to decrement in the internal gate voltage decreasing the channel current. As a result, a lower drain voltage gives better more current in the subthreshold region especially for larger ferroelectric thickness. Large ferroelectric thickness leads to more negative capacitance effect.

Capacitance matching is another important aspect of ferroelectric FET design. This can be seen from the following equation of voltage gain using capacitance network formula

$$A_V = \frac{\partial V_{int}}{dV_G} = \frac{|C_{FE}|}{|C_{FE}| - C_{int}} \tag{3.7}$$

A closer matching between $|C_{FE}|$ and C_{int} where C_{int} is the internal gate capacitance gives highest voltage gain A_V. Ideally the capacitance matching should be achieved throughout the region of operation. However, due to non linear nature of both C_{int} and C_{FE}, this is not possible.

The output characteristics of NCFETs and normal FinFETs are shown in Fig. 3.7. An interesting observation is the presence of negative output conductance in the output characteristics. The negative output conductance can also be explained similar to negative DIBL. When V_D increases, the charge on the metal intermediate metal layer decreases, as a result of which the voltage across the ferroelectric increases. This further decreases the internal gate voltage suppressing the drain

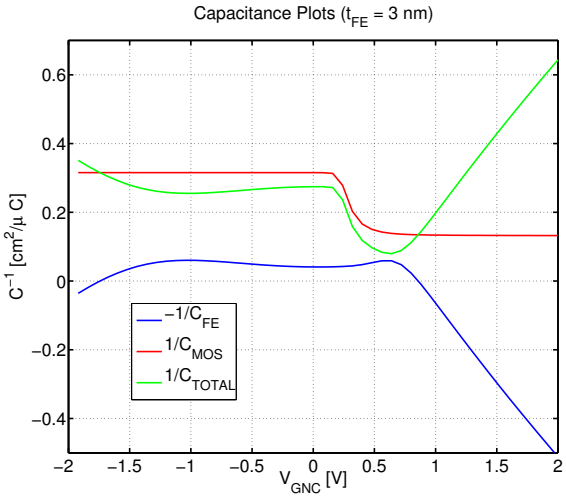
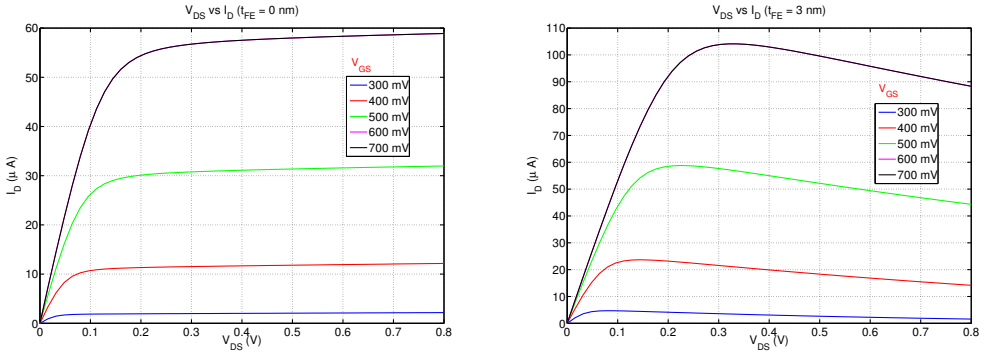


Figure 3.5: Capacitance matching helps in providing better voltage gain. For stable operation total capacitance $C_{MOS} > 0$

current. A positive feedback mechanism is thus setup which is finally terminated by the non linearities of the ferroelectric and the internal MOSFET. Such a behaviour is also observed experimentally for example in [19]

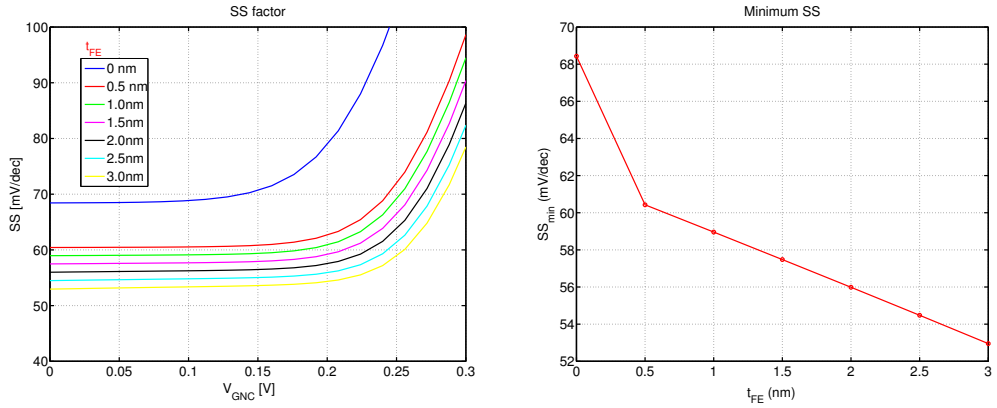


(a) (b)

Figure 3.6: Output characteristics of the FET device. (a) Without ferroelectric, the output shows positive output conductance (b) with ferroelectric, the device shows negative output conductance

Finally we look at the subthresold swing of the device. Subthreshold swing decreases with increasing ferroelectric thickness. This can be attributed to enhanced negative capacitance at higher thickness. A minimum sub threshold swing of 52.4 mV/dec is observed which is consistent with the experimentally reported data [10].

In summary we have seen that adding a ferroelectric can enhance the subthreshold swing of the device. Increasing ferroelectric thickness can lead to better performance, however increasing the thickness might lead to occurrence of hysterisis, which can lead to difficulties in circuit design. Negative DIBL and output conductance are also seen, which are also observed experimentally in other works.



(a) (b)

Figure 3.7: Subthreshold swing of the deices. (a) Variation with gate voltage (b) minimum subthreshold swing reduces with increasing t_{FE} due enhanced negative capacitance

3.2 Modeling double gate ferroelectric MOSFETs

In this section we develop and analyse a model for double gate MOSFET with intrinsic channel. This model, as opposed to previous model does not need an internal metal gate.

3.2.1 Basic model for double gate MOSFETs

An analytical model has been proposed in [20]. For an intrinsic MOSFET the Poisson equation will be

$$\frac{d^2\psi}{dy^2} = \frac{q}{\varepsilon_{\rm si}} n_i e^{q\psi/kT} \tag{3.8}$$

Assuming a symmetric MOSFET, with electric field at $E_y(y = \frac{t_{si}}{2}) = 0$ we have a solution for the equation given by

$$\frac{q(\psi - \psi_0)}{2kT} = -\ln\left[\cos\left(\sqrt{\frac{q^2 n_i}{2\varepsilon_{\rm si} kT}} e^{q\psi_0/2kT} x\right)\right] \tag{3.9}$$

where ψ_0 is the potential at the mid of the channel.

In presence of a channel potential we can write

$$\psi(x,y) = V(x) - \frac{2kT}{q} ln\left[\frac{t_{Si}}{2\beta L_D} cos\left(\frac{2\beta y}{t_{Si}}\right)\right] \tag{3.10}$$

where β is unknown. In this gradual channel approximation, channel quaasi fermi level is assumed to vary only along the channel from source to drain. L_D is the Debye length.

The surface potential is given by

$$\psi_s(x,y) = V(y) - 2\phi_t ln\left(\frac{t_{Si}}{2L_D}\right) + 2\phi_t ln(\beta) - 2\phi_t ln(cos\,\beta) \tag{3.11}$$

Using voltage law, $V_G = \psi_s + \psi_{ox} + V_{FB}$ and $\psi_{ox} = QC_{ox}$ where Q can be found out from Gauss' law as $Q = \epsilon_{Si}\frac{\partial\psi(x)}{\partial x}\Big|_{x=\frac{t_{Si}}{2}}$

$$Q = \frac{4\phi_t\epsilon_{Si}}{t_{Si}}\beta\, tan\,\beta \tag{3.12}$$

Adding a ferroelectric term $\psi_{fe} = 2\alpha Q + 4\beta Q^3$ we have

$$V_G - V(x) + 2\phi_t ln\left(\frac{t_{Si}}{2L_D}\right) = 2\phi_t ln(\beta) - 2\phi_t ln(cos\,\beta) + \left(\frac{t_{ox}}{\epsilon_{ox}} + \alpha t_{fe}\right)\frac{4\phi_t\epsilon_{Si}}{t_{si}}\beta\, tan\,\beta + \gamma t_{fe}\left(\frac{4\phi_t\epsilon_{Si}}{t_{Si}}\beta\, tan\,\beta\right)^3 \tag{3.13}$$

Current is next calculated by Pao Sah Integral:

$$I_{DS} = \mu\frac{W}{L}\int_0^{V_{DS}} Q_{inv}(V)dV = \mu\frac{W}{L}\int_{\beta_s}^{\beta_d} Q_{inv}(\beta)\frac{dV}{d\beta}d\beta \tag{3.14}$$

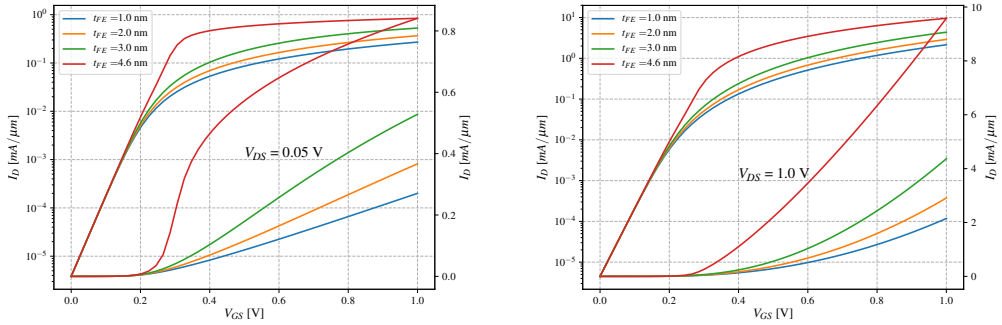
where β_s and β_d are solutions to 3.13 at source where $V = 0$ and drain where $V = V_{DS}$. Evaluation of the above integral leads to

$$g_r(\beta) = \mu\frac{W}{L}\frac{16\epsilon_{Si}\phi_t^2}{t_{Si}}\left[\beta\, tan\,\beta - \frac{\beta^2}{2} + \frac{\epsilon_{Si}}{t_{Si}}\left(\frac{t_{ox}}{\epsilon_{ox}} + \alpha t_{fe}\right)\beta^2 tan^2\beta\right] + \mu\frac{W}{L}\frac{6\epsilon_{Si}\phi_t\gamma t_{fe}}{t_{Si}}\left(\frac{4\phi_t\epsilon_{Si}}{t_{Si}}\right)^3\beta^4 tan^4\beta \tag{3.15}$$

Current is then given by

$$I_{DS} = g_r(\beta_s) - g_r(\beta_d) \tag{3.16}$$

The performance characteristics of the device with $t_{si} = 5\ nm$ and $L = 1\ \mu m$ are shown in Fig. for various ferroelectric thickness



(a) (b)

Figure 3.8: Double gate MOSFET device performance. (a) Linear regime (b) Saturation regime I_{ON} increases with increasing ferroelectric thickness

In this chapter hence we have first analyzed the DC characteristics of NC devices. LK equations in their quasi stationary limit have been used to get FinFET characteristics at 14 nm technology node. Sub 60 mV/dec subthreshold swing is observed and negative DIBL and output conductance are observed which have interesting circuit implications.

An analytical model for MFIS structure is derived for a double gate MOSFET structure. The model outcome shows that as expected the device on current increases with increase of ferroelectric thickness.

Chapter 4

Transient analysis and performance of NC devices

In this chapter we will look at the performance of the NC devices, especially the inverter and ring oscillator. Then we will analyse the scalability of NC devices to future technologies. Finally we will look at the transient performance of the NC devices using TCAD analysis.

4.1 Circuit performance of NC devices

In this section we review the transient performance of NC devices by first analysing the performance with Ring oscillator and then inverter.

4.1.1 Ring oscillator performance

Ring oscillator is an important logic device useful in predicting the speed and response of a transistor. A large time period implies a larger delay for the signal to propagate through the device, while smaller time period of the ring oscillator implies a smaller delay.

The landau Khalatnikov equation described in previous chapter is used here to model the FinFET device with ferroelectric gate stack.

$$\rho \frac{dP}{dt} = -(2\alpha P + 4\beta P^3 + 6\gamma P^5 - E_{FE}) \tag{4.1}$$

The compact model described in the previous chapter is again used for this analysis. A 13 stage inverter is designed and used to simulate the characteristics of the RO. Two cases have been simulated and analyzed in case of a ring oscillator.

- Assuming that polarization can switch infinitely fast. This corresponds to the case of $\rho = 0$.
- Uing $\rho \neq 0$. This is the diffusive limit which is modeled by LK equation as described by Eq. 4.3. This limit however does not completely capture the polarization switching of the NCFET and is discussed later.

The results for first case are shown in Fig. 4.1. Even though the polarization can switch infinitely fast in this case, we see that the time period of the NC RO is greater than that without ferroelectric.

The increment in time period is attributed purely to increase in parasitic capacitance at the output node of an inverter.

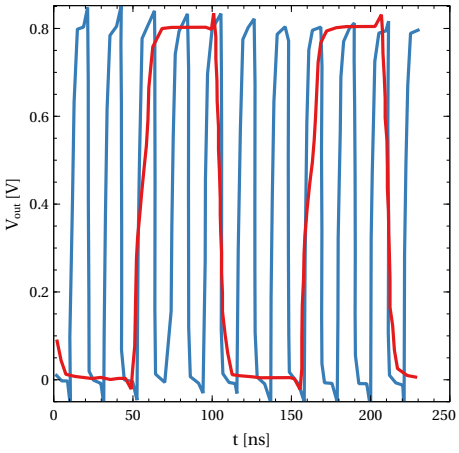


Figure 4.1: Infinitely fast switching ferroelectric ($\rho = 0$). Blue waveform indicates the waveform without ferroelectric, while the red waveform shows the RO characteristics with ferroelectric

Due to addition of a ferroelectric in the gate stack f the ring oscillator, the effective capacitance seen by the previous inverter is

$$\frac{1}{C_{eff}} = \frac{1}{C_G} + \frac{1}{C_{FE}} \tag{4.2}$$

Since $C_{FE} < 0$ for certain bias conditions, C_{eff} infact is more that C_G increasing the delay of the inverter. This explains the higher time period of the NC RO.

In case $\rho \neq 0$, performance is shown in Fig

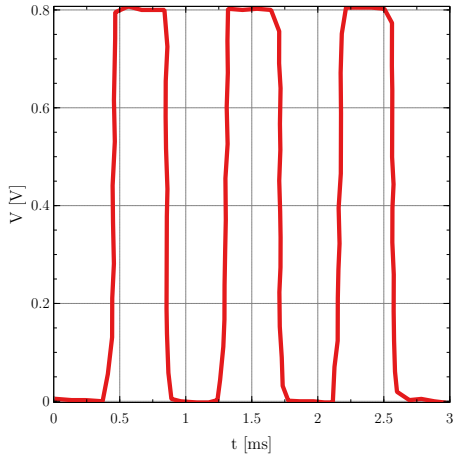


Figure 4.2: Finitely switching ferroelectric ($\rho = 4\ cm \cdot s/F$). Due to large value of ρ, it takes finite amount for the polarization to switch

In this case, in addition to increase in load capacitance, the polarization itself takes time to change its value.

However it has been observed experimentally [21] that the ring oscillator performance of the NCFET is on par with normal FinFET. This dilemma has been resolved in [22] where it has been

shown that LK equation is only a diffusive limit of more general polarization switching phenomena governed by the equation

$$\kappa \frac{d^2P}{dt^2} + \rho \frac{dP}{dt} = -(2\alpha P + 4\beta P^3 + 6\gamma P^5 - E_{FE}) \tag{4.3}$$

In the limit when $\frac{dP}{dt}$ is small, the first term can be neglected. Hence the LK equation in the form of Eq. 4.3 is mostly suitable for transient based quasi stationary analysis wherein we allow the system to relax to a steady state to get quasi static results. It should not be used for a full transient analysis. A particular use of transient analysis is shown to calculate hysteresis phenomena in ferroelectric.

4.1.2 Inverter performance

An inverter is a building block for all digital circuits. The inverter characteristics of the NCFET using model previously described is shown in Fig.

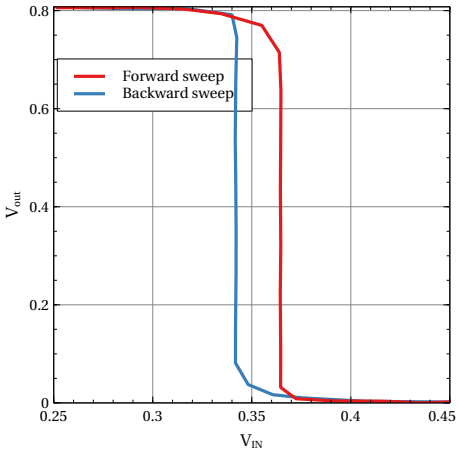


Figure 4.3: Inverter VTC with $t_{FE} = 3\ nm$. Hysteresis is observed due to negative output conductance.

An interesting phenomena is the observation of hysteresis in the VTC even though the $I_D - V_G$ characteristics do not show any hysteresis.

To account for the same we note that under normal conditions, for given input voltage V_{in} the output curves for NMOS and PMOS only intersect at one point, which decides the operating point. However in presence of NDR, the curves can intersect at multiple points which leads to a hysteresis. Also compared to the usual MOSFET we observe a steeper transition. This is due to lower subthreshold swing compared to usual FinFET. As a result of lower subthreshold swing, the MOSFETs can switch to on state with a lower requirement for voltage.

4.2 Scalability of NCFETs

To further study the advantages of the NCFET devices we perform a scalability analysis on the NC devices with shrinking dimensions. Inorder to do the same we use TCAD analysis to enhance our understanding as compact models are usually designed and calibrated only for a particular technology node and cannot be used to perform the device analysis for future technologies.

Three technology nodes have been analysed, particularly the 10 nm, 7 nm and the 5 nm. The dimensions used are specified in ITRS [23] are given in the following table

Table 4.1: Device dimensions for various technology nodes

Dimension	5 nm	7 nm	10 nm
L_G	11.9 nm	14 nm	18 nm
H_{FIN}	42 nm	42 nm	42 nm
W_{FIN}	6 nm	6 nm	6 nm
t_{ox}	0.61 nm	0.61 nm	0.61 nm

Source and drain have been doped with doping of $N_{SD} = 10^{20}\ cm^{-3}$ while channel doping has been taken to be $N_{ch} = 10^{18}\ cm^{-3}$. The device structure and the doping concentration have been shown in Fig. 4.4

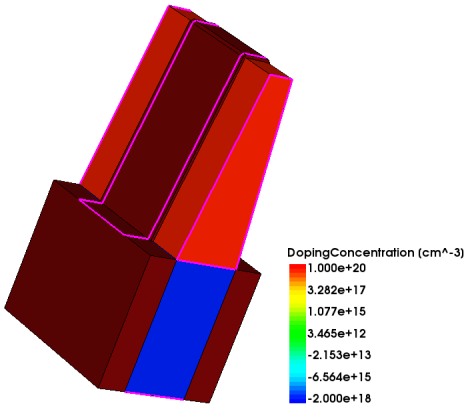
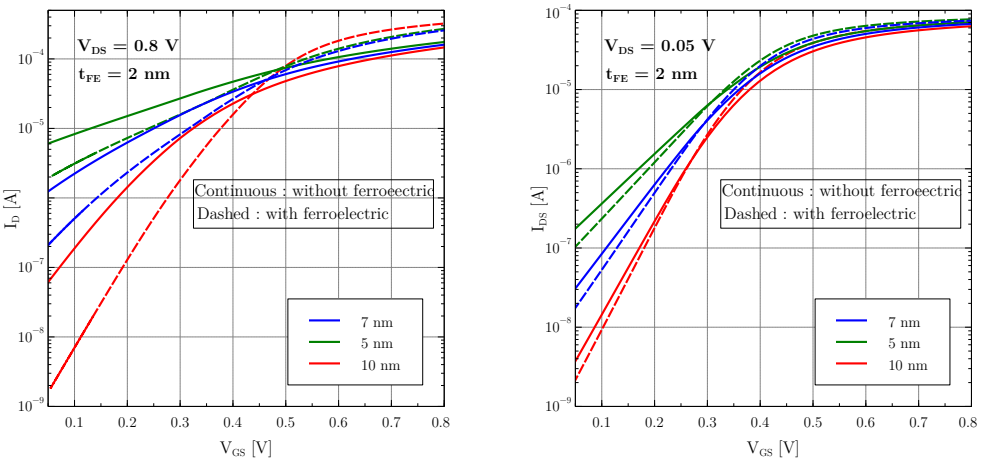


Figure 4.4: FinFET device structure used for present analysis
s

Ferroelectric has been considered 1D and has been externally coupled to the device mentioned in the previous chapter using 1D LK equations. As a result an intermediate metal layer has been assumed. Models to take into account phenomena like high field saturation, doping dependence of mobility, band gap narrowing due to high concentration and mobility degradation ue to ormal electric fields have been taken into account.

Input characteristics are shown in Fig. 4.5. As can be seen from the characteristics, the subthreshold swing of the 5 nm technology is almost equal to that of 7 nm technology, while the subthreshold swing of 7 nm technology with FE is on par with that of 10 nm technology. This clearly indicates that the device scaling can be continued using FE technology to lower device device dimensions in accordance with the Moores law without having significant short channel effects. A similar plot is also shown for input characteristics in the linear regime where we observe that subthreshold swing of the FE devices has greatly reduced due to voltage amplification by the negative capacitance ferroelectric. The usefulness of NC devices is especially visible in saturation region. Due to high V_{DS}, the off current in this situation is very high. However as discussed previously, NC dielectric provides a negative DIBL effect which effectively tends to reduce the threshold voltage at higher drain voltages and hence reduces the off current and at the same time enhancing the on current.



(a) (b)

Figure 4.5: Input characteristics at various technology nodes (a) Saturation regime. Effectiveness of NCFETs is especially visible here (b) Linear regime

The DIBL characteristics of the device are shown in Fig. 4.5. where saturation and linear characteristics of 7 nm technology device have been compared.

Table 4.2: DIBL and SS performance for various technology nodes with ferroelectric gate stack

Technology →	5 nm		7 nm		10 nm	
Parameter	Std	Fe	Std	Fe	Std	Fe
SS (mV/dec)	376	282	218	157	116	92
DIBL (mV/V)	278	120	155	56	77.6	19.2

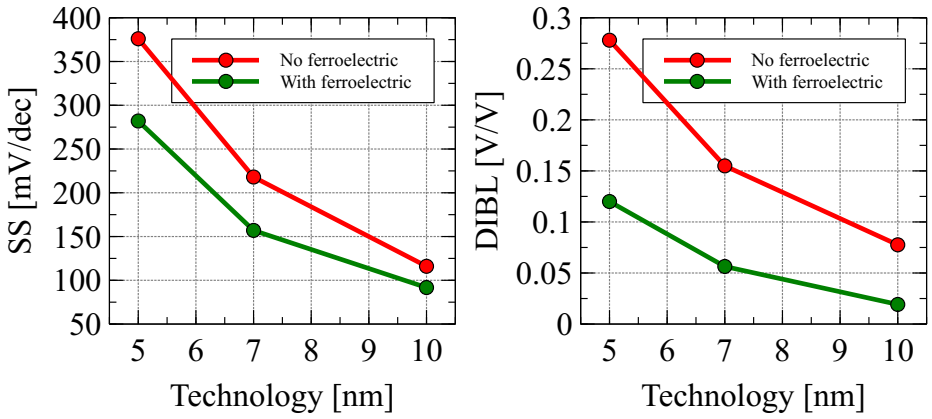


Figure 4.6: Ferroelectrics in gate stack can be used to achieve a performance enhancement of one technology ahead

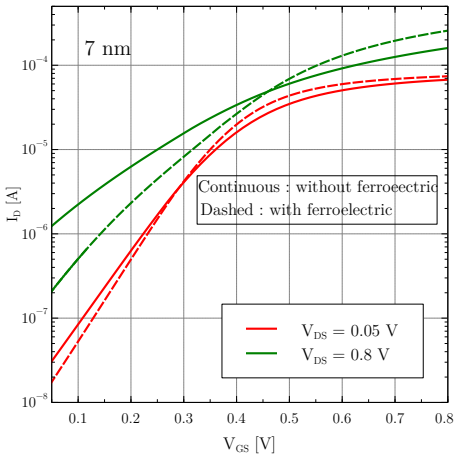


Figure 4.7: 7 nm technology saturated and linear region input characteristics showing a reduction in DIBL due to negative DIBL effect

4.3 Quasistationary anlysis using time domain LK equation

While the stationary LK equation can be used to get the characteristics of the device when the system is stable ($C_{total} > 0$), it cannot be used get the system characteristics when there is hysteresis in the device and the negative capacitance becomes unstable.

Such an analysis uses the LK equation in its diffusive limit. This use is justified as we finally need the quasi stationary behaviour and really not worried abut the actual transient solution of the device. The following algorithm is used to get the characteristics

- Provide initial guess to the system
- Allow the system to relax to steady state
- Record the values

This algorithm is shown schematically in Fig.

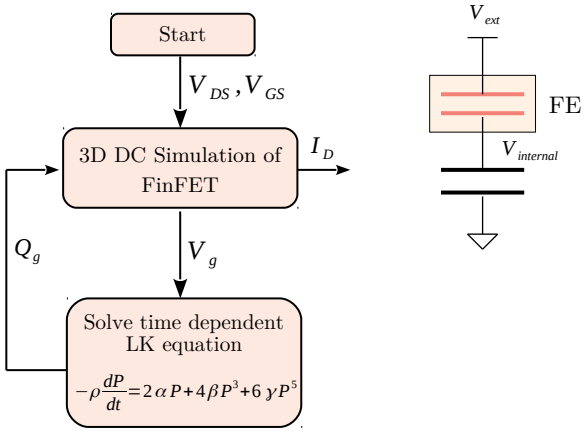


Figure 4.8: Algorithm for quasistationary analysis using time dependent LK equations

Following figure shows the hysteresis characterization of the ferroelectric device when a $t_{FE} = 5\ nm$ is used. The ferroelectric is unstable in this regime and hence shows a hysteresis.

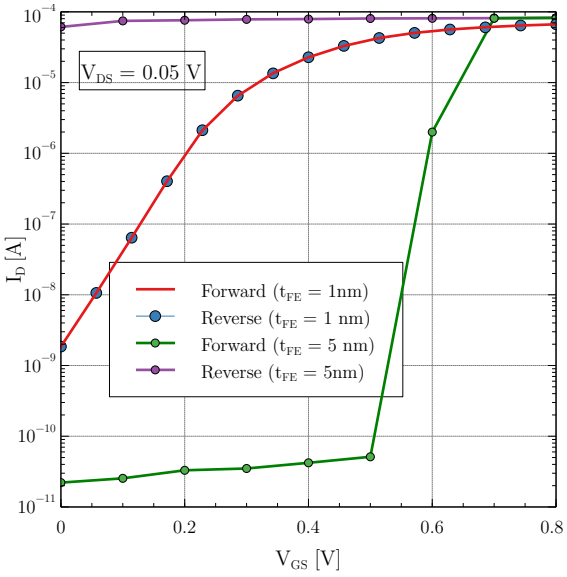


Figure 4.9: Hysteresis due to large t_{FE}

In conclusion we have seen in this chapter the circuit performance of NC devices. The invereter and the ring oscillator although can be operated at a lower voltage due to enhanced subthreshold swing but have significant disadvantage of operating at a lower speed due to added capacitances at the output node.

Also the circuit performance of the NCFETs at various future technologies has been observed. We see that NC effect indeed provides an immunity to short channel effects and allows further scaling of the devices.

Finally a model is developed where in time dependent LK equations are used to get quasi stationary response of the the 3D FinFET for 7 nm technology node.

Chapter 5

Phase field modeling of NCFETs

In this chapter we develop and study some models which take into account the multidomain nature of the ferroelectrics. This is important as most of the times ferroelectrics are observed to split to domains so as to minimize the electrostatic energy due to depolarization fields. Initially we consider a phase field model with ferroelectric capacitor in series with a resistor which resembles the experiment described in [9]. We then investigate the performance of short channel double gate MOSFET taking into account domain interactions.

5.1 Time dependent Landau Ginzburg theory with multi domain ferroelectrics

In presence of multiple domains, Landau Ginzburg theory can be described by [24]

$$\frac{dP_z}{dt} = -\rho\big(2\alpha P + 4\beta P^3 + 6\gamma P^5 - E_z - \frac{1}{2}\kappa_p \nabla^2 P_z\big) \tag{5.1}$$

which has an additional gradient term as compared to traditional LK equation described in previous chapters. This term indicates that whenever there is a gradient in polarization, the polarized domains move in such a way so as to minimize the gradient in polarization. This in in particular important in case of a ferroelectric in series with a MOSFET as the electric field along the MOSFET varies with application of drain bias which tends to induce different polarization along the length of the ferroelectric.

To apply this model, we initially consider the circuit shown in Fig. 5.1. Since we are considering 2D structure, the electrode of the capacitor has a total charge of

$$Q_F = \int_S P_z dS \tag{5.2}$$

where integral is taken over entire surface.

Total current in the circuit would then be given by

$$i = \frac{dQ_F}{dt} = \frac{d\Big(\int_S P_z dS\Big)}{dt} = \int_S \frac{dP_z}{dt} dS \tag{5.3}$$

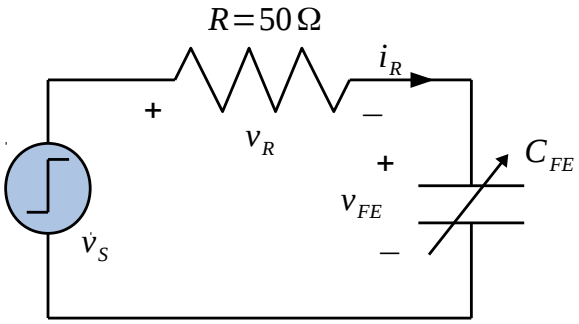


Figure 5.1: A series combination of ferroelectric capacitor and a resistor.The capacitor is considered to have a 2D structure

Substituting Eq. 5.1 in the above equation we have

$$\frac{dQ_F}{dt} = i_R = \int_S -\rho\big(2\alpha P + 4\beta P^3 + 6\gamma P^5 - v_{FE}/t_{FE} - \kappa\nabla^2 P_z\big)dS \tag{5.4}$$

Next we assume that electric field ($E_z = v_{FE}/t_{FE}$) in the ferroelectric is independent of spatial location and is given by $v_{FE} = v_S - i_R R$. This when back substituted in the previous equation we have an equation for current

$$i_R = \frac{1}{1 + \frac{A\rho R}{t_{FE}}}\left(\frac{A\rho v_S}{t_{FE}} + \int_S -\rho\big(2\alpha P + 4\beta P^3 + 6\gamma P^5 - \kappa\nabla^2 P_z\big)dS\right) \tag{5.5}$$

where v_S is dependent on time. We solve this equation using finite difference discretization for a ferroelectric of dimensions $50\mu m \times 50\mu m$.

The total charge on the ferroelectric always increases as $Q_F = \int i_R dt$ and the current in the circuit is always positive as otherwise this would violate the law of conservation of energy.Hence the charge on the ferroelectric capacitor always increases. However since there is a series resistor, the supply of the charge to the ferroelectric capacitor is slowed down from the external source. During some period of time, the polarization of the ferroelectric is not compensated by the external supply and the effective voltage across it becomes negative.

In this study effect of ferroelectric coupling factor κ_p on characteristics of Fig. 5.1.

5.1.1 Analysis with different coupling coefficients

In this case the TDGL equation reduces to the one dimensional case. The simulated characteristics are shown in Fig 5.2. Parameters are considered from Table 3.1 and $t_{FE} = 10nm$. Since the entire capacitor is assumed to have a uniform polarization, the entire polarization needs to switch, which gives rise to sharp dip in ferroelectric voltage. However experimentally a much smoother negative capacitance switching is observed, although it is qualitatively similar to the one considered here [9]

Next we consider the case with $\kappa_p = 1.0 \times 10^{-7}$. To get the initial state of the capacitor, we initially assume a random state of polarization and the allow the Landau Ginzburg free energy to minimize. Next we perform the analysis as described previously. The initial state of the ferroelectric capacitor is shown in Fig. 5.3

The characteristics of the switching process are shown in Fig. 5.4. Here the transition is much

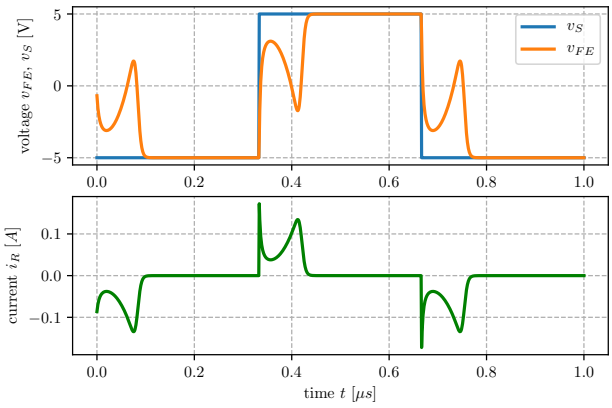


Figure 5.2: Ferroelectric in series with resistor. Homogeneous ferroelectric is assumed. Observe the sharp fall in v_{FE} as the entire ferroelectric has to switch transiting from negative capacitance regime.

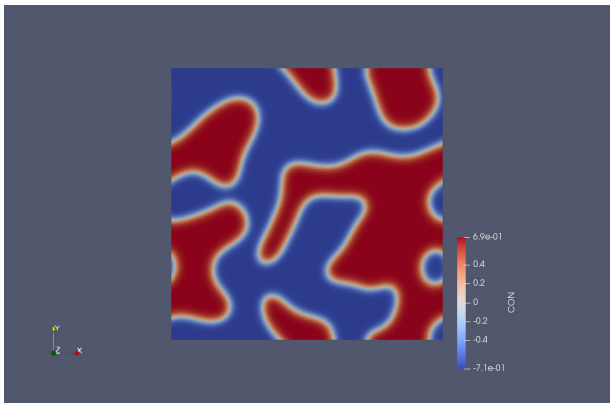


Figure 5.3: Initial state of the ferroelectric capacitor considered for simulation

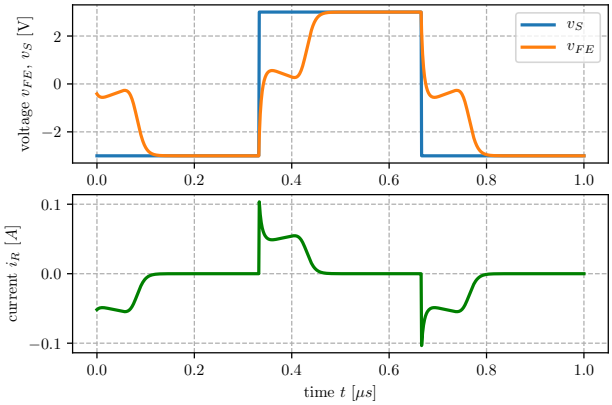


Figure 5.4: Ferroelectric in series with resistor. $\kappa_p = 1.0 \times 10^{-7}$. In this case fall in v_{FE} is more smooth as entire ferroelectric need to switch during the process.

smoother as the entire ferroelectric does not have to switch during the switch process. However there is an additional charge that needs to be supplied by the battery for the domain wall motion. In addition to switching from positive to negative domains, the domain walls move so as to minimize free energy, which requires some amount of charge. This can be seen from observing the characteristics

of ferroelectric in Fig 5.5 with $\kappa_p = 1.0 \times 10^{-8}$ where in since the energy associated with domain walls is small, the domains move at a much smaller rate. As a result, the battery needs to provide even lesser charge further decreasing the negative capacitance effect.

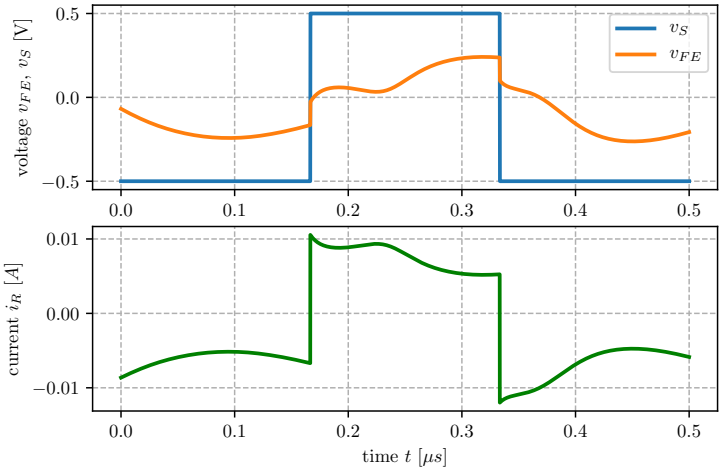


Figure 5.5: Ferroelectric in series with resistor.$\kappa_p = 1.0 \times 10^{-8}$. Lesser negative capacitance is observed as a smaller fraction of the ferroelectric needs to switch.The charge associated with domain wall motion is also small

5.2 Double gate MOSFET model with multi domain ferroelectric

Next we develop and study a TCAD based model to study the effects of ferroelectric in double gate MOSFET gate stack. The model we consider here is similar on that described in [14], however instead of using NEGF formalism we use TCAD based drift - diffusion model for the core MOSFET simulation. This has the potential advantage of extending the simulation to other device structures like SOI MOSFETs.

The simulated structures for MOSFETs are shown in Fig. 5.6.

5.2.1 Simulation methodology

In this study, we divide the gate electrode into $N = 12$ smaller electrodes. This enables us toextract the charges from all the electrodes, which in general case would be different owing the presence of the channel potential. A domain of ferroelectric is placed on each electrode and the LK equation for each electrode separately

$$E_{FE,i} = \alpha Q_i + \beta Q_i^3 + \gamma Q_i^5 - \frac{1}{2}\kappa_p \frac{Q_{i-1} - 2Q_i + Q_{i+1}}{\Delta x^2} \tag{5.6}$$

Where the last term is central difference approximation of gradient and $\Delta x = L_g/N$. This is then solved self consistently by $V_{Gi} = V_G - V_{FE,i}$ where V_{Gi} is the voltage on i^{th} internal electrode.

This entire process is automated using Python Jinja templating engine. Algorithm is depected in flow chart in Fig. 5.7

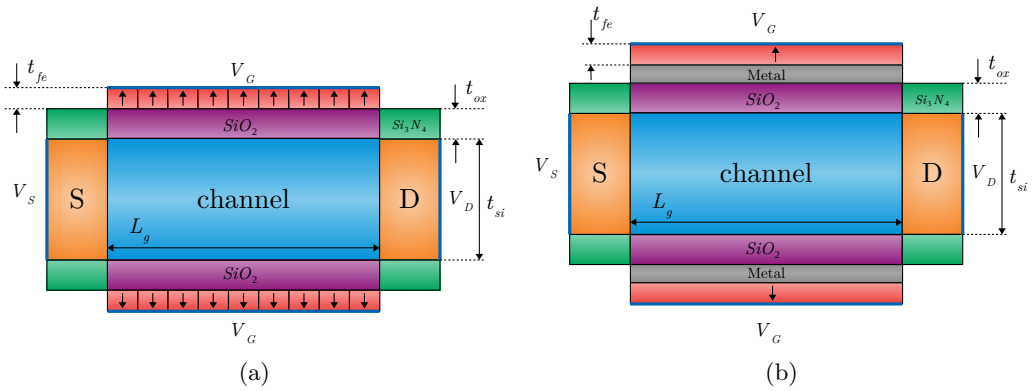


Figure 5.6: Double gate MOSFETs used for simulation (a) Structure without inter layer metal (b) Structure with interlayer metal

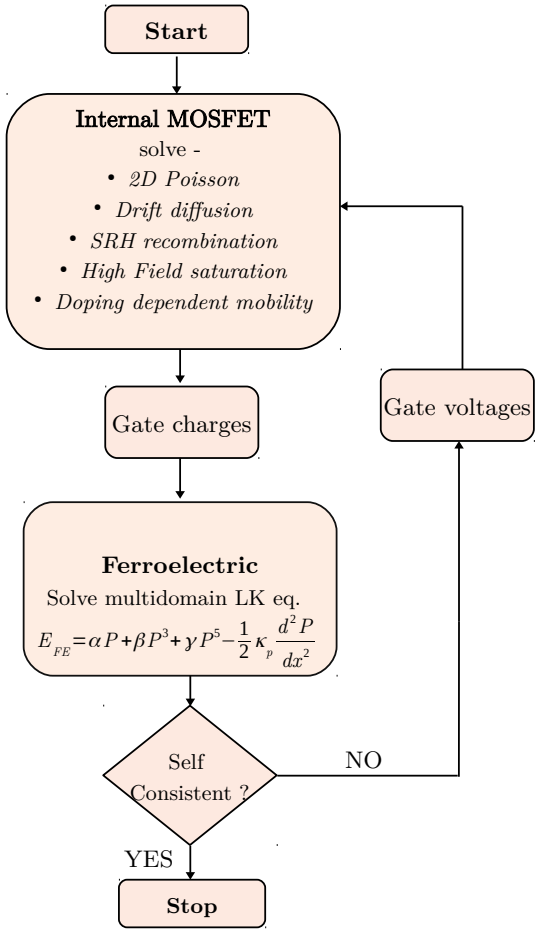


Figure 5.7: Flow chart depecting flow of simulation

Parameters cosidered for simulation are tabulated in Table. 5.1

Table 5.1: Parameters used for simulation

Parameter	Value
N_{SD}	$10^{20} cm^{-3}$
$N_c h$	$10^{15} cm^{-3}$
t_{ox}	0.5 nm
t_{Si}	5 nm
L_g	12 nm
α	$-5.1 \times 10^9\ m/F$
β	$2 \times 10^{11}\ m^5/F/C^2$
γ	$1 \times 10^7\ m^9/F/C^4$

5.3 Results and discussion

For inter layer metal case all electrodes are at same voltage and $Q_{avg} = \frac{1}{N}\sum_i Q_i$ We first consider the performance for different thickness of ferroelectric as shown in Fig. 5.8. This case of ILM corresponds to $\kappa_p \to \infty$ as there is no variation in polarization along the ferroelectric. As κ_p gets largerthe variation in polarization must decrease

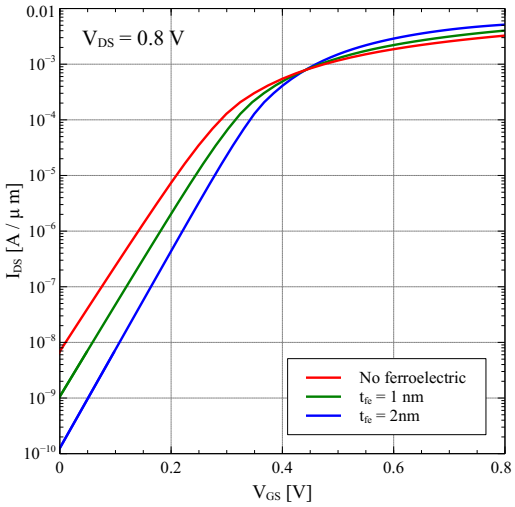


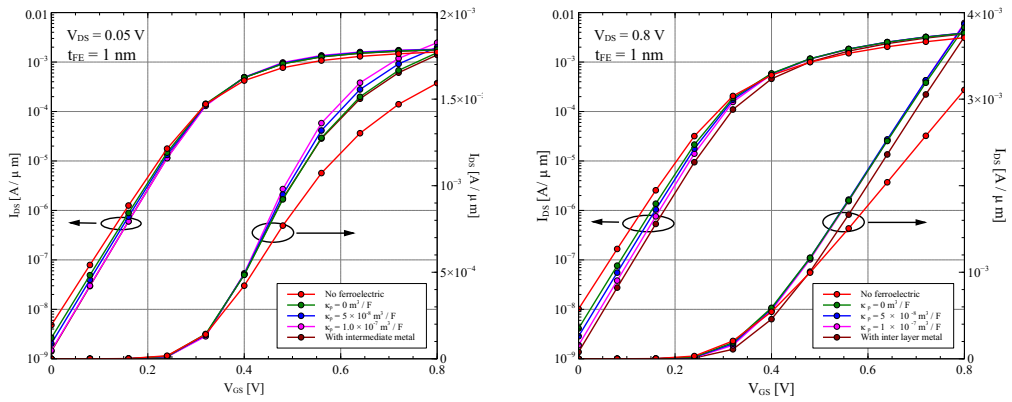
Figure 5.8: Input characteristics for various ferroelectric thickness with interlayer metal

Table 5.2: Subthreshold swing with interlayer metal

t_{FE}	SS
0 nm	66.1 mV/dec
1 nm	59.8 mV/dec
2 nm	51.8 mV/dec

As can be seen evidently, SS increases with decresing in κ_p. This is because at low gate voltage polarization along x has a concave down curvature leading to $\frac{d^2Q}{dx^2} < 0$. Hence with decrease in κ_p especially at lower gate voltages, electric field in ferroelectric decreases leading to lower NC effect. On the same account, DIBL decreases with increase in κ_p as shown in Fig. 5.10

Next we consider the analysis with different values of κ_p. The input characteristics asre shown in Fig. 5.9



(a) (b)

Figure 5.9: Input characteristics for various κ_p (a) Linear regime (b) Saturation regime

Table 5.3: Subthreshold swing for various κ_p

κ_p	SS
No ferroelectric	66.1 mV/dec
$\kappa_p = 0.0m^3/F$	64.2 mV/dec
$\kappa_p = 5.0 \times 10^{-8}m^3/F$	62.3 mV/dec
$\kappa_p = 1.0 \times 10^{-9}m^3/F$	60.4 mV/dec
ILM	59.8 mV/dec

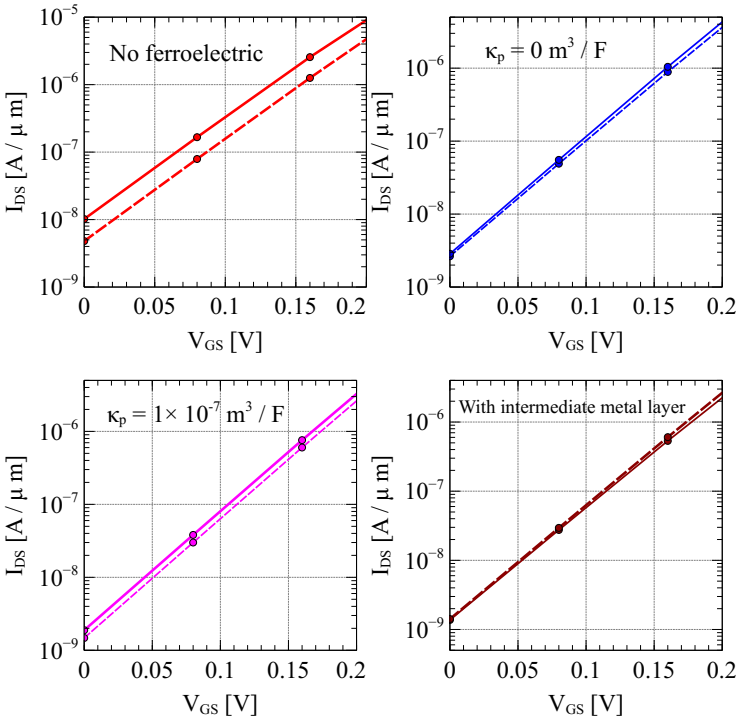
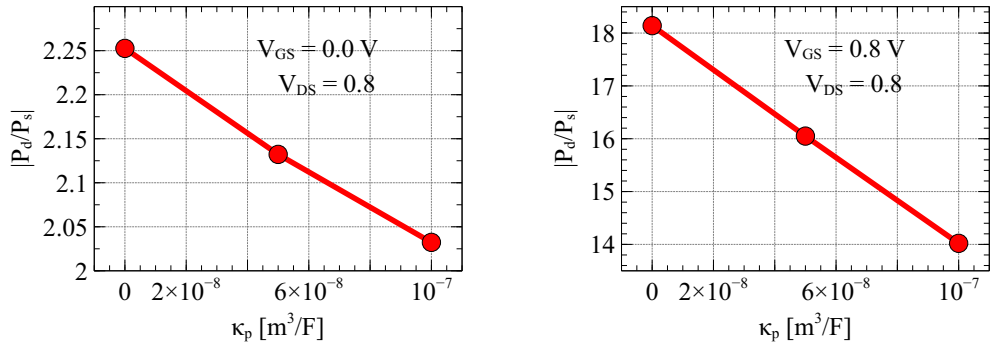


Figure 5.10: DIBL in various configurations. Dashed curves are for linear regime while solid are for saturation . In case of ILM there is a small negative DIBL observed.

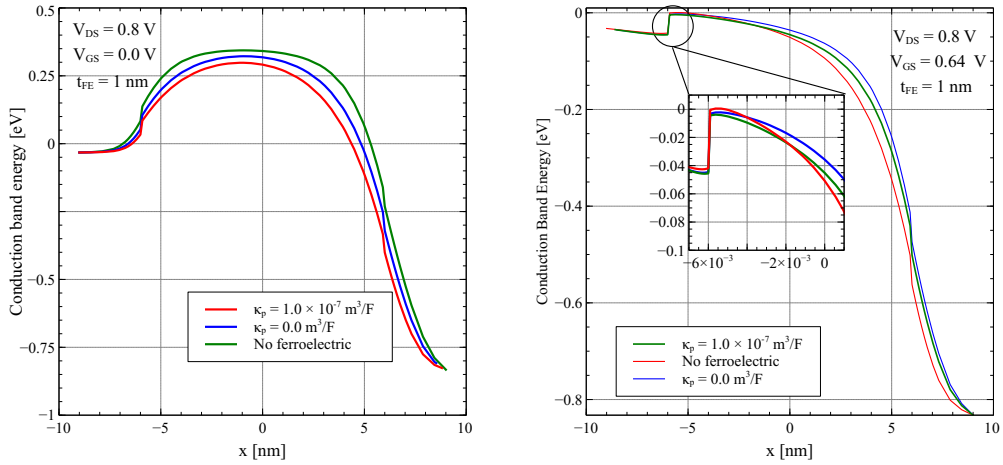
The decrease in off current and subsequent subthreshold swing can be justified due to influence of drain side polarization on source side polarization. Since the drain side polarization is negative, this reduces the polarization at source side increasing the source side barrier, decreasing the off current. This is shown in Fig. 5.11 where as can be seen the ratio of source side and drain side polarization falls as κ_p increases.



(a) (b)

Figure 5.11: Influence of drain polarization on source polarization (a) Off situation (b) On situation

The effect of such a coupling on source side barrier is shown in Fig. 5.12. With increase in κ_p, as source polarization decreases, the depolarization field increases which further increases the source side barrier.



(a) (b)

Figure 5.12: Influence of drain polarization on source barrier (a) In off state the source barrier increases with increasing κ_p (b) In On state with increase in κ_p, source side barrier decreases.

A study with varying thickness of ferroelectric is also shown in Fig. 5.13 where it is evident that with increase in ferroelectric thickness, due to more negative capacitance effect, the subthreshold swing drops.

The output characteristics of the device are shown in Fig. 5.14

As can be seen from the characteristics higher κ_p leads to lower output conductance and a negative output conductance in case of ILM. With increase in κ_p, the drain side polarization starts

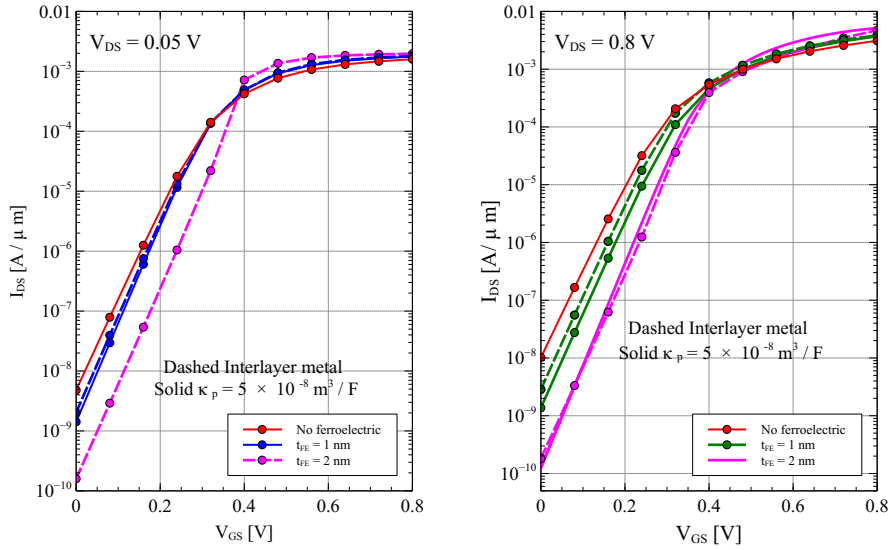
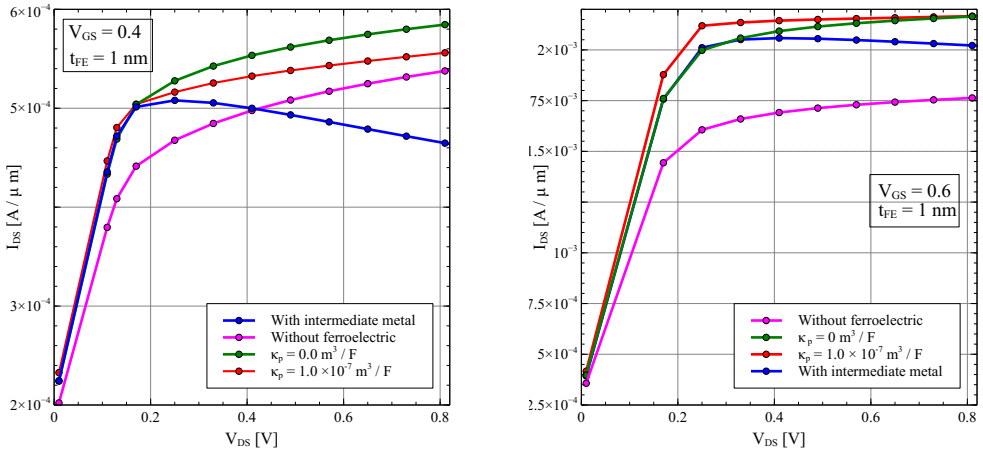


Figure 5.13: With increasing thickness the subthreshold swing of the device falls



(a) (b)

Figure 5.14: Output characteristics for various κ_p (a) $V_G = 0.4$ V (b) $V_G = 0.6$ V

affecting the source side polarization more. As a result with increase in drain voltage source side polarization decreases as drain side polarization also decreases. This leads to steady voltage drop near the source side making the barrier almost constant.

In this chapter hence we have seen the phase field modeling of NCFETs. Initially we have considered a 2D analysis of ferroelectric capacitor with series resistances and then we have developed a TCAD based model using which we have analyzed the impact of domain interactions on NCFET performance.

Chapter 6

Conclusion and future work

In this chapter we provide conclusion and future scope of work

6.1 Conclusion

DC Modeling of NCFETs In this chapter we have developed compact models for NCFETs both analytical and numerical. The compact model so developed is compatible with various present generation industry standard compact models like BSIM-CMG. The use of negative capacitance in gate stack can give sub 60 mV/dec subthreshold swing which is greatly helpful in reducing transistor threshold voltage and hence power consumption. Also the inclusion of negative capacitance in gate stack leads to an additional barrier rising due to decrement in internal gate voltage with increasing drain voltage. This phenomena when dominates the barrier lowering due to drain side electric field leads to NDR and drain induced barrier rising in NCFETs . Hence in addition to standard logic devices, NCFETs can be used for creation of other useful circuits like oscillators. However this has a potential disadvantage that this would make circuit design difficult (for example in such a case, an inverter would show hysteresis.

An analytical model for long channel undoped double gate MOSFET with negative capacitance gate stack without inter layer metal has been derived and indicates decrement in subthreshold swing. However this model does not take into account short channel effects and hence can be mainly used as a core model for more advanced compact models.

Transient analysis and performance of NC devices In this chapter we have analyzed important circuits like inverter and ring oscillator using NC devices. Also we have analyzed the performance of future technology nodes for NC FET devices. The circuits designed with ferroelectric in gate stack exhibit negative output conductance. Due to negative output conductance the inverter exhibits hysteresis in the transfer characteristics. This could lead to challenges in circuit design. However this could also be used as advantage in designing oscillator circuits. We next investigated the ring oscillator circuit using NC devices. The frequency of the ring oscillator is observed to be lesser compared to that using normal FinFET. This can be attributed to additional capacitance in the gate stack. In the diffusive limit, the performance is even poorer, however the diffusive limit is itself useful only in slow transients.

Having evaluated the performance of some elementary circuits with negative capacitance devices, we have undertaken a study on to future technology nodes. We have observed using TCAD simulations that NC effect can be used to downscale the devices to future generations (upto 5 nm technology). NCFETs give lower subthreshold swing as well as lower DIBL which indicates better suppression of short channel effects. Subthreshold swing is reduced due to voltage amplification, while DIBL decrement is due to another phenomena of barrier rising due to inclusion of negative capacitance in gate stack which compensates for lowering of barrier due to drain electric field.

Phase field modeling of NCFETs In this chapter we have mainly analyzed the effects of interdomain coupling of ferroelectrics on electronic device performance. Intially We developed a model based on Allan Cahn equations to simulate a ferroelectric capacitor in series with a resistor. We analyzed the effect of coupling factor on NC effect of a series resistor ferroelectric capacitor circuit and observed that decreasing coupling factor leads to decrement in negative capacitance due to lower domain wall velocity. We have continued this study of the effect of coupling coefficient to device analysis where in we have developed a TCAD based model for simulating NCFETs in various configurations like with inter layer metal and without inter layer metal with different coupling coefficients. We see that with increase in coupling coefficient, the sub-threshold swing decreases. Also in case of NCFET with interlayer metal, a negative output conductance is observed.

6.2 Future work

A lot of modeling and physical effects have been left out in this theses and can be carried out in future. Most of the work doen herein is either 1D or 2D. However for more accurate analysis of 3D short channel effects in negative capacitance MOSFETs, a full 3D analysis of ferroelectrics needs to be performed. This should properly take into account all the effects of crystallographic directions of permanent polarization in the ferroelectric materials.Stress and strain influence the ferroelectric properties heavily. A proper evaluation of effects of stress and strain on NCFETs needs to be done since in modern fabrication process, lattice mismatch between two materials can induce large mechanical strain in the material. As a result Landau parameters depend on many external parameters like stress, temperature, etc.A variability and reliability analysis needs to be performed to evaluate the device performance in various process corners. Such an analysis should also take into account the polycrystalline nature of ferroelectric when deposited on 3D FinFET gate stack.

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