

Trade-off and Design optimization of the Notch filter for ultralow power ECG application

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This thesis entitled "TRADE-OFF AND DESIGN OPTIMIZATION OF THE NOTCH FILTER FOR ULTRA-LOW POWER ECG APPLICATION" by AMIT KUMAR (EE16MTECH11015) is approved for the degree of Master of Technology from IIT Hyderabad.

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Dedicated to

My Parents and Pravanjan Patra Sir

Abstract

ECG acquisition, several leads combined with signals from different body parts (i.e., from the right wrist and the left ankle) are utilized to trace the electric activity of the heart. ECG acquisition board translates the body signal to six leads and processes the signal using a low-pass filter (LPF) and SAR ADC. The acquisition board is composed of: an instrumentation amplifier, a high-pass filter, a 60-Hz notch filter, and a common-level adjuster. But miniaturization or need of portable devices for measuring Bio-Potential parameters has led to design of IC's for biomedical application with ultra-low power. Because of miniaturization i.e. use of lower technology nodes has led to non-idealities which reduces the attenuation of Common Mode to differential component i.e. not CMRR. Because of this demerit the power line interference signal can't be assumed as a common mode signal. Hence we need to design a power line interference filter to avoid the contamination of the signal.

Contents

Declaration	2
Approval Sheet.....	3
Acknowledgements	4
Abstract	6
1 Introduction	9
1.1 Motivation.....	9
2 Characterization of Notch Filter	11
2.1 Requirement for designing a Notch Filter.....	11
2.2 Design of Passive Notch Filter	11
2.3 Why do we need Active Notch Filter?.....	12
2.4 Active Notch Filter	12
2.4.1 Tow-Thomas Architecture.....	12
2.4.1.1 Notch Frequency	12
2.4.1.2 Notch Depth.....	13
2.4.1.3 Quality Factor.....	13
2.4.2 Modelling of each block.....	14
2.4.3 Operation of circuit at lower frequencies	18
2.4.4 Operation of circuit at higher frequencies.....	20
2.5 Optimizing R and C Values.....	21
3 Background of OTAs.....	24
3.1 OTA Terminology	24
3.2 Different OTA Configuration.....	27
3.3 Recycling folded cascode OTA.....	36
3.4 Improved Recycling folded cascode OTA.....	42
3.5 Comparison of all the OTA.....	48
3.6 Application of OTA.....	49

4 G_m/I_D Methodology	47
4.1 Introduction	47
4.2 Different regions of operation.....	48
4.3 Performance Comparison among Different regions of operation	54
4.4 Different types of Model.....	54
5 OTA Design and Analysis	
5.1 The Conventional Folded Cascode Amplifier	57
5.2 Recycling Folded Cascode Amplifier	58
5.3 Two Stage Recycling Folded Cascode Amplifier.....	60
5.4 OTA Design requirements	61
5.4.1 OTA Design Parameter	61
5.4.2 Power Consumption of First Stage OTA	61
5.4.3 2 nd Stage OTA	61
5.5 Recycling Folded Cascode	62
5.5.1 Design of RFC.....	62
6 Simulation and Results	65
7 References	81

Chapter 1

INTRODUCTION

1.1 Motivation

In the last Decade, there has been a growing demand for the design of wireless sensing device for biomedical applications. These devices are utilized for monitoring and recording bio-potential signals such as electrocardiogram (ECG), electroencephalography (EEG), and electromyography (EMG), to name a few.

Wearable monitoring systems provide tremendous benefits but they have many design challenges e.g. low power consumption, self-sustainability, light weight, affordability. Most crucial among previously mentioned issues are low power and self-sustainability. A typical biomedical wearable sensor consists of AFE, ADC and power module as shown in fig 1. To make the system self-sustainable an energy harvesting module has to be incorporated. For example, fig presents an ECG acquisition and processing system on chip (SoC) with energy harvesting module to make it self-sustainable. Although the above system fulfils the processing requirement but it suffers from a major drawback of high AFE power consumption ($4.8\mu\text{W}$) which leads to fast drainage of battery.

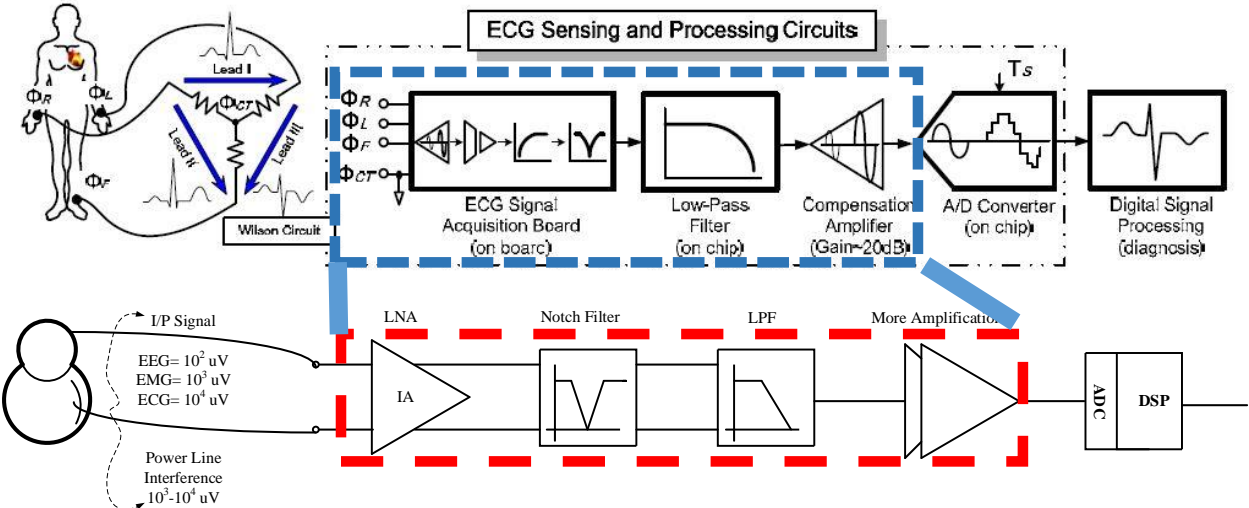


Figure 1. Bio-medical sensor interface

A detailed system level architecture of ECG acquisition unit is shown in fig 1. It consists of AFE which includes Instrumentation amplifier followed by two PGA, a mixed signal AGC and a 10-bit SAR ADC. The system is powered by RF energy harvesting circuit. The AFE combined with ADC consumes a total power of 343nW.

ECG acquisition, several leads combined with signals from different body parts (i.e., from the right wrist and the left ankle) are utilized to trace the electric activity of the heart. ECG acquisition board translates the body signal to six leads and processes the signal using a low-pass filter (LPF) and SAR ADC. The acquisition board is composed of: an instrumentation amplifier, a high-pass filter, a 60-Hz notch filter, and a common-level adjuster.

Chapter 2

Characterization of Notch Filter

2.1 Requirement for designing a notch filter

- ECG acquisition, several leads combined with signals from different body parts (i.e., from the right wrist and the left ankle) are utilized to trace the electric activity of the heart. ECG acquisition board translates the body signal to six leads and processes the signal using a low-pass filter (LPF) and SAR ADC.
- The acquisition board is composed of: an instrumentation amplifier, a high-pass filter, a 60-Hz notch filter, and a common-level adjuster.
- The main function of the acquisition board is to pre-amplify the weak ECG signal whose amplitude is between 100 μ V and 4 mV.
- The range of the ECG signal means that this system requires a signal-to-noise and distortion ratio (SNDR) of at least 32 dB (that is, 6 bits) to detect heart activities precisely.
- The frequency range of the ECG signal is between 0.1 Hz to 250 Hz
- Therefore, an on-chip low-power LPF behind the acquisition board provides a low cut-off frequency (250 Hz) to decrease the out-of-band high-frequency noise.
- On the other hand, the noise under 0.1 Hz will be eliminated by a high-pass filter on the acquisition board

2.2 Design of Passive Notch filter

Transfer Function is given as:

$$T(s) = \frac{R}{R+Z_{eq}}, \quad Z_{eq} = sL \parallel \frac{1}{sC} \quad (2.1)$$

$$T(s) = \frac{V_o}{V_i} = \frac{R}{\left(\frac{L}{C} + R\right)} = \frac{R \left(sL + \frac{1}{sC}\right)}{\left(\frac{L}{C} + R \left(sL + \frac{1}{sC}\right)\right)} = \frac{s^2 + \frac{1}{LC}}{s^2 + \frac{1}{RC}s + \frac{1}{LC}} \quad (2.2)$$

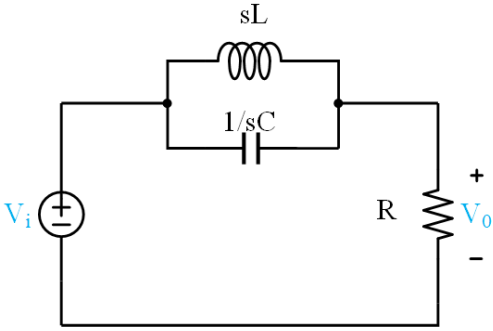


Fig:2.1 Notch Filter Circuit

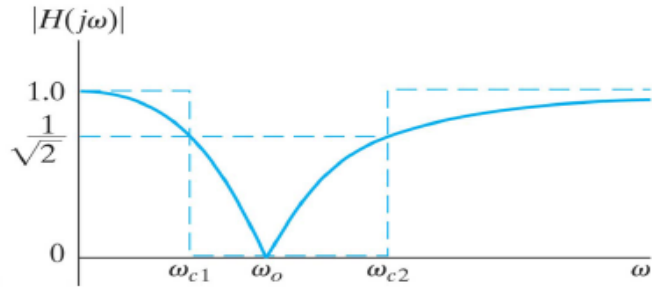


Fig:2.2 Plot Gain Vs frequency

2.3 Why do we need Active Notch filter

PASSIVE	ACTIVE
<ul style="list-style-type: none"> • inductors large for lower frequencies • some inductors (non-toroidal) may require shielding • limited standard sizes, often requiring variable inductors and therefore tuning • low tolerance inductors (1-2%) very expensive • must be designed with consideration to input and output loading • Generally not amenable to miniaturization • no power gain possible • no voltage gain 	<ul style="list-style-type: none"> • no inductors • easier to design • high Zin, low Zout for minimal loading • can produce high gains • generally easier to tune • small in size and weight

2.4 Active Notch filter

2.4.1 Tow-Thomas Architecture

2.4.1.1 Notch Frequency:

$$\omega_0 = \frac{1}{2^n R \sqrt{C C_3}} \quad (2.3)$$

2.4.1.2 Quality Factor:

$$Q = \sqrt{\frac{C}{C_3}} q \quad (2.4)$$

2.4.1.3 Notch Depth (p):

$$\begin{aligned}
 p &= \frac{1}{|T_{(non-ideal)}(j\omega_0)|} \\
 &= 1 + \frac{C_3}{C} \left(\frac{A}{2Q} + 1 \right) \\
 p &= 1 + \sqrt{\frac{C_3}{C}} \left(\frac{A}{2Q} + \sqrt{\frac{C_3}{C}} \right)
 \end{aligned} \tag{2.5}$$

2.4.2 Modelling of Each block:

2.4.2.1 Mathematical Modelling of Closed Loop Architecture:

$$V_{out} = \frac{V_{in} * A}{(1 + A\beta)} \tag{2.6}$$

$$Error = \frac{V_{in}}{(1 + A\beta)} \tag{2.7}$$

$$Feedback\ Path\ Voltage = \frac{V_{in} * A\beta}{(1 + A\beta)} \tag{2.8}$$

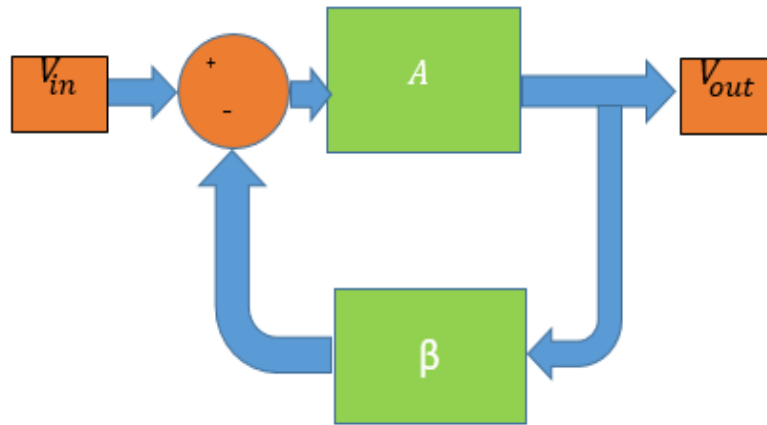


Fig: 2.3 Closed Loop block diagram

2.4.2.2 Mathematical Equivalent of High Pass Filter:

Feedback Path transfer function i.e. β

$$\begin{aligned}
 V_{out} &= \frac{V_{in}}{\left(\frac{1}{G+sC} + \frac{1}{sC} \right)} \times \frac{1}{sC} \\
 &= \frac{V_{in}}{\left(\frac{sC}{G + sC} + 1 \right)}
 \end{aligned} \tag{2.9}$$

$$\frac{V_o}{V_i} = \frac{1}{\left(\frac{sC}{G+sC}+1\right)} = \frac{1}{\left(\frac{sRC}{1+sRC}+1\right)} = \frac{1+sRC}{1+s2RC} \quad (2.10)$$

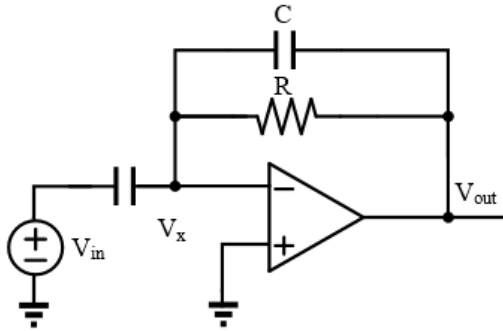


Fig.2.4 High Pass Architecture

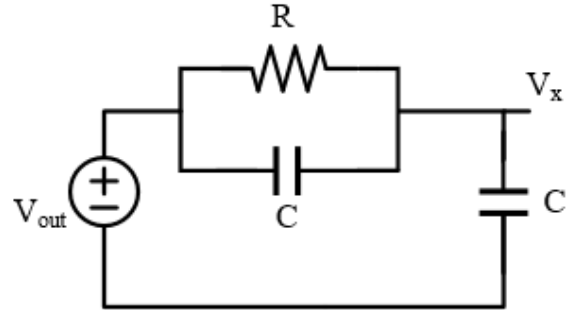
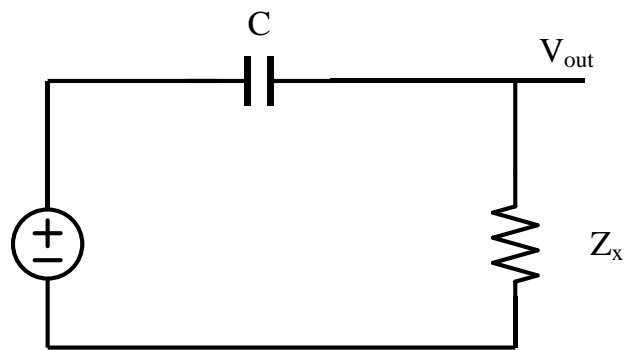
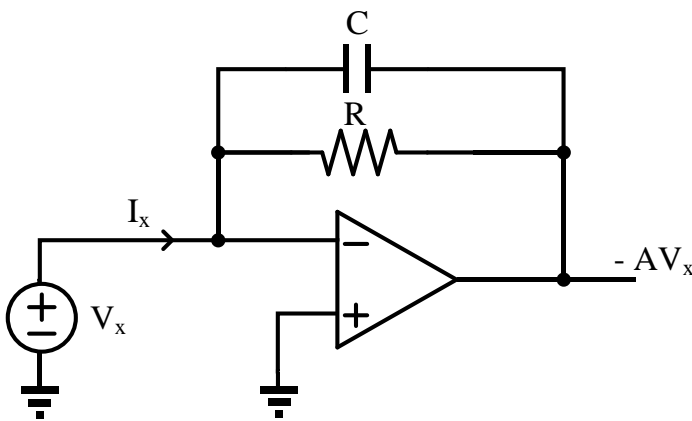


Fig.2.5 Feedback Architecture

2.4.2.3 Problem in error voltage:

Thevenin Equivalent impedance of the high pass filter



$$I_x = V_x (1 + A)(G + sC)$$

$$\frac{V_x}{I_x} = \frac{1}{(1 + A)(G + sC)}$$

$$Z_x = \frac{R}{(1 + A)(1 + sRC)}$$

$$Z_x = \frac{R}{(1 + A)(1 + sRC)}$$

$$(V_{in} - V_{err}) * sC = \frac{V_{err} * (1 + A)(1 + sRC)}{R}$$

$$\frac{V_{err}}{V_{in}} = \frac{sRC}{1 + s2RC + A * (1 + sRC)}$$

$$Error = \frac{V_{in}}{(1 + A\beta)}$$

$$\frac{V_{err}}{V_{in}} = \frac{1 + 2sRC}{1 + s2RC + A * (1 + sRC)} ; \text{which is not correct}$$

The below expression is real expression according to the circuit

$$\frac{V_{err}}{V_{in}} = \frac{sRC}{1 + s2RC + A * (1 + sRC)}$$

Note: This Discrepancy is because of input loading which is not taken care.

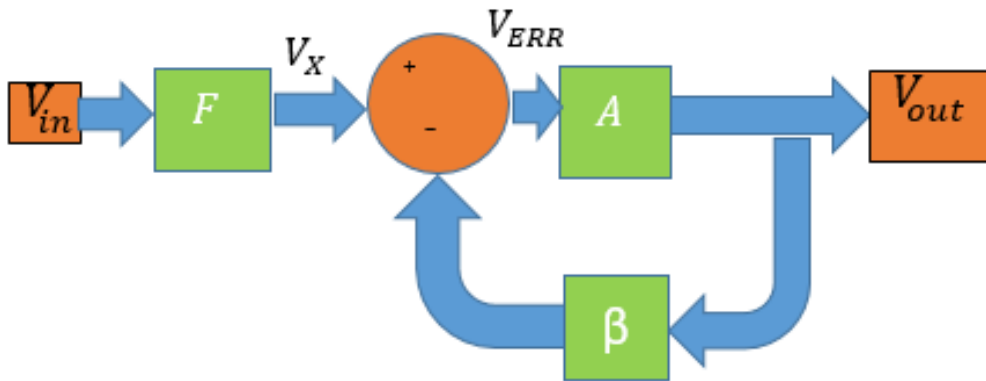


Fig: 2.6

$$V_{err} = \frac{V_x}{(1 + A\beta)}$$

$$\frac{V_{err}}{V_x} = \frac{1 + 2sRC}{1 + s2RC + A * (1 + sRC)}$$

$$\frac{V_{err}}{V_{in}} = \frac{sRC}{1 + s2RC + A * (1 + sRC)}$$

Since, $\frac{V_{err}}{V_{in}} = \frac{V_{err}}{V_x} * \frac{V_x}{V_{in}}$

The Transfer Function, $\frac{V_x}{V_{in}} = \frac{sRC}{(1 + s2RC)}$

2.4.2.4 Complete Model of HPF

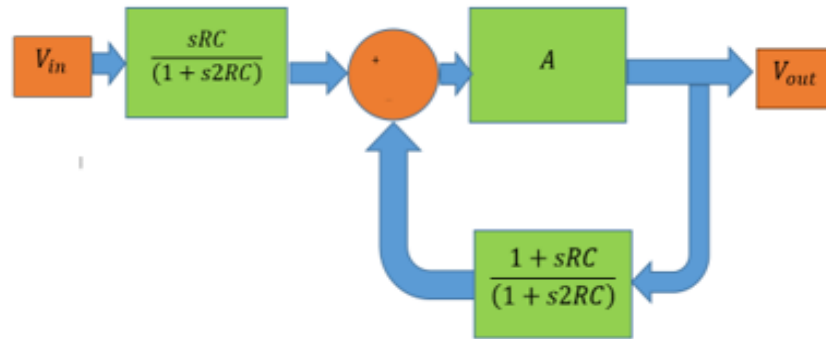


Fig: 2.7

Conclusion:-

- The feedback is unity for lower frequencies.
- Error voltage is zero as the input is blocked by capacitor.
- Feedback goes to 0.5 for frequencies greater than $1/RC$.
- The input is high passed with a gain of 1 after RC .

2.4.2.5 Mathematical modelling of integrater or LPF

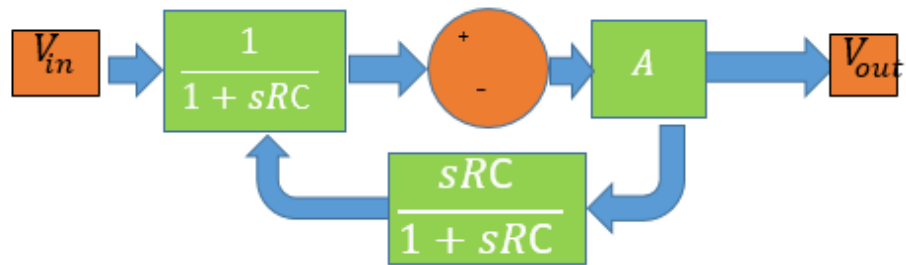


Fig: 2.8

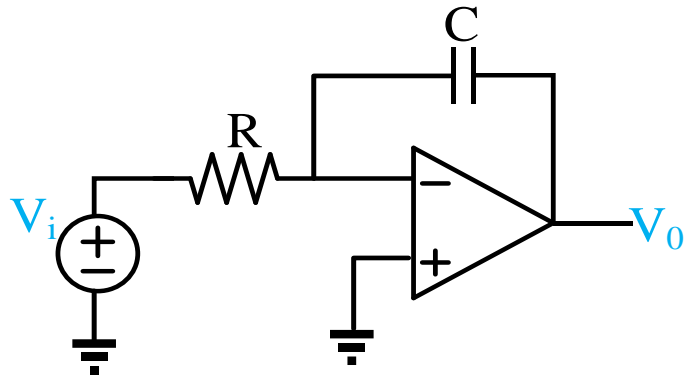


Fig: 2.9

Conclusion

- Here the error voltage is V_{in} for frequencies $< 1/RC(1+A)$.
- The feedback factor goes to unity at $-1/RC$.
- The gain is < 1 after $-1/RC$.

2.4.3 Operation of Circuit at Lower frequencies:

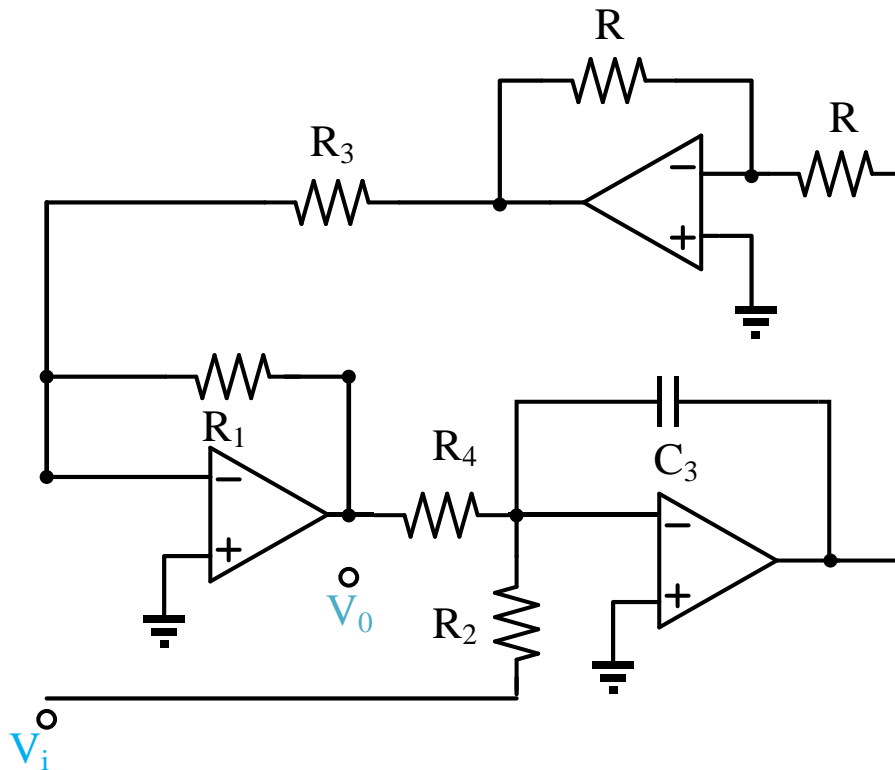


Fig:2.10

- For Lower frequencies, as we saw the input is high pass filtered by 1st amplifier. The cutoff frequency is $1/R_1C$. Which is assumed to be lower than $1/R_2C_3$.
- Hence to have a higher loop gain the R_1/R_3 ratio has to be improved i.e. >1 . As the loop gain increases output voltage exactly follows the input voltage.
- The UGB of the 2nd amplifier i.e. integrator is $-1/R_2C_3$ for the input at lower frequencies.
- The Loop Gain is shown by red loop. Once the loop gain goes to unity it gives -3dB point of the lower cutoff frequency.
- As R_1 is increased the cutoff frequency can be moved but it leads to decrease in peaking as the attenuation decreases.

2.4.3.1 Loop Gain at Low Frequencies:

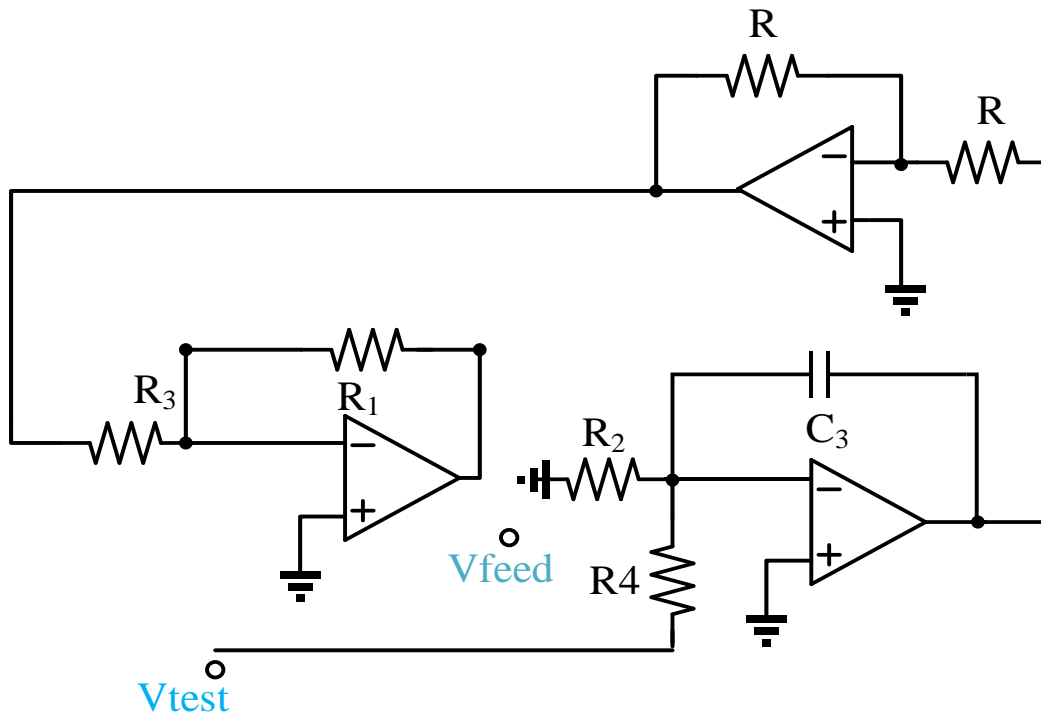


Fig: 2.11

- Here the loop gain is found by applying a V_{test} at the input of R_4 and finding feedback at V_{feed} .
- For proper negative feedback V_{feed} has to be first order. So $R_1 * C_2 < R_4 * C_3$.
- For more notch depth $R_1 * C_2$ should be around one third of $R_4 * C_3$.
- The frequency where $\frac{V_{feed}}{V_{test}} = 1$. It gives the lower cutoff frequency of the notch.

2.4.4 Operation of Circuit at higher frequencies

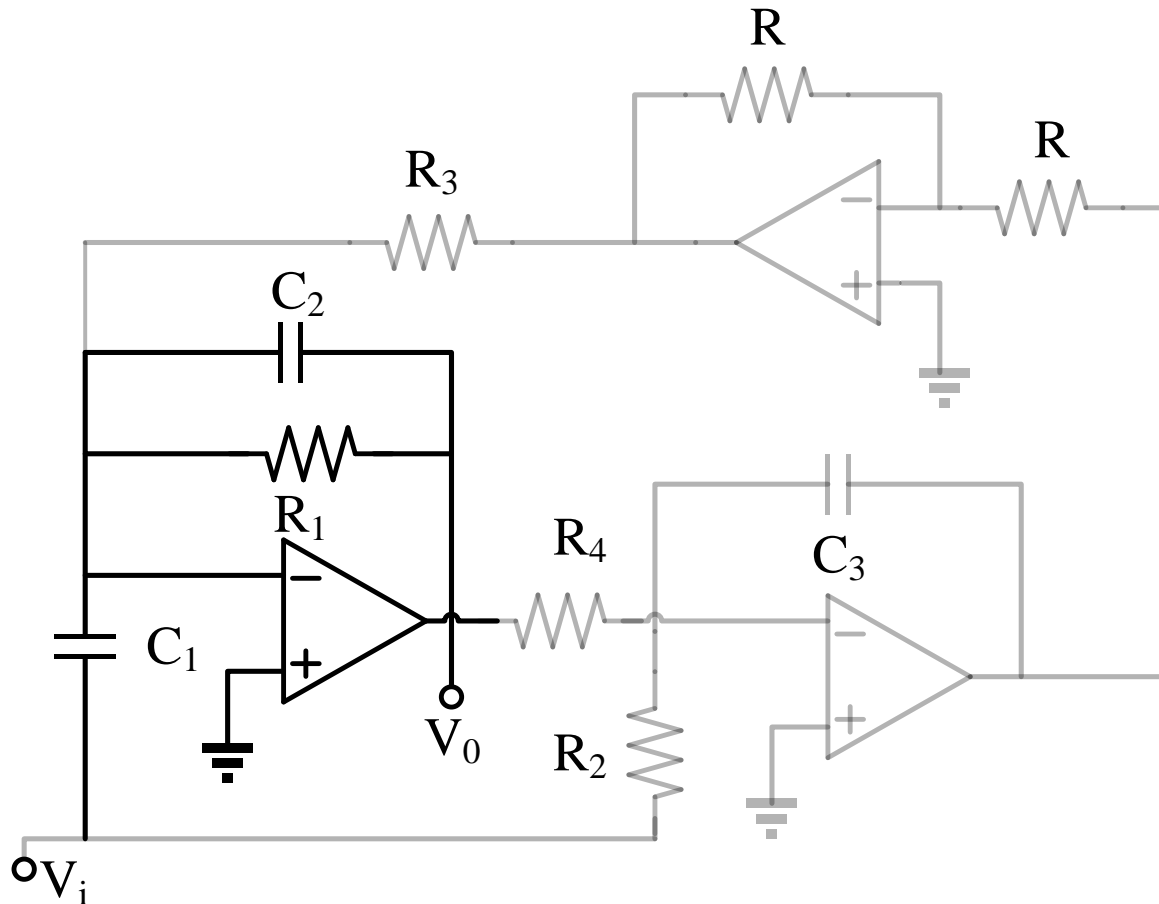


Fig: 12

- At higher frequencies i.e. frequencies greater than $1/R_1C_2$. The part of the active circuit is shown in dark.
- $1/R_1C_2$ provides the -3dB corner frequency in the upper side.
- The output is given by C_1/C_2 ratio which is chosen to be 1 as because of filter.
- The gain continues to be one till the loop gain is greater than one.
- Hence for a operation frequency of 250Hz the UGB of the amplifier has to be 500Hz as $B=0.5$.
- Hence maximum UGB required is 500Hz.
- As this amplifier should give a gain of 1 for higher frequencies compared to other amplifiers. Hence maximum UGB is given by this amplifier.

2.5 Optimizing the R and C values for Higher Notch depth(p)

- For getting higher notch values the quality factor of zeros has to be increased.
- The other way of optimizing is to increase C3/C ratio. Increasing C3 leads to a lower 3dB cutoff frequency again R4 and R2 has to be optimized. The values of R4 and R2 are kept same.
- The values of R2, R4 and C3 offers the lower cutoff frequency. The values for lower cutoff frequency is chosen to be greater than 10Hz. ; $R_2 = R_4 = 2^n R$
- For having higher peaking q has to be less than or equal to 1. $R_1 = qR$
- For A gain of 1 at higher frequencies $C_1 = C_2 = C$
- For higher peaking and lower quality factor $C_3 > C$
- The design starts with fixing $\omega_0 = 2\pi * 55 \text{ rad/sec}$
- Where ω_0 is given by: $\omega_0 = \frac{1}{\sqrt{CC_3 2^{2n} R^2}}$
- Here the C is assumed to be 1p, N=15 and C3 is chosen to be 10p. The values are chosen such that it can be implemented within a low power and lower device area. Here n represents the number of R-2R ladders.

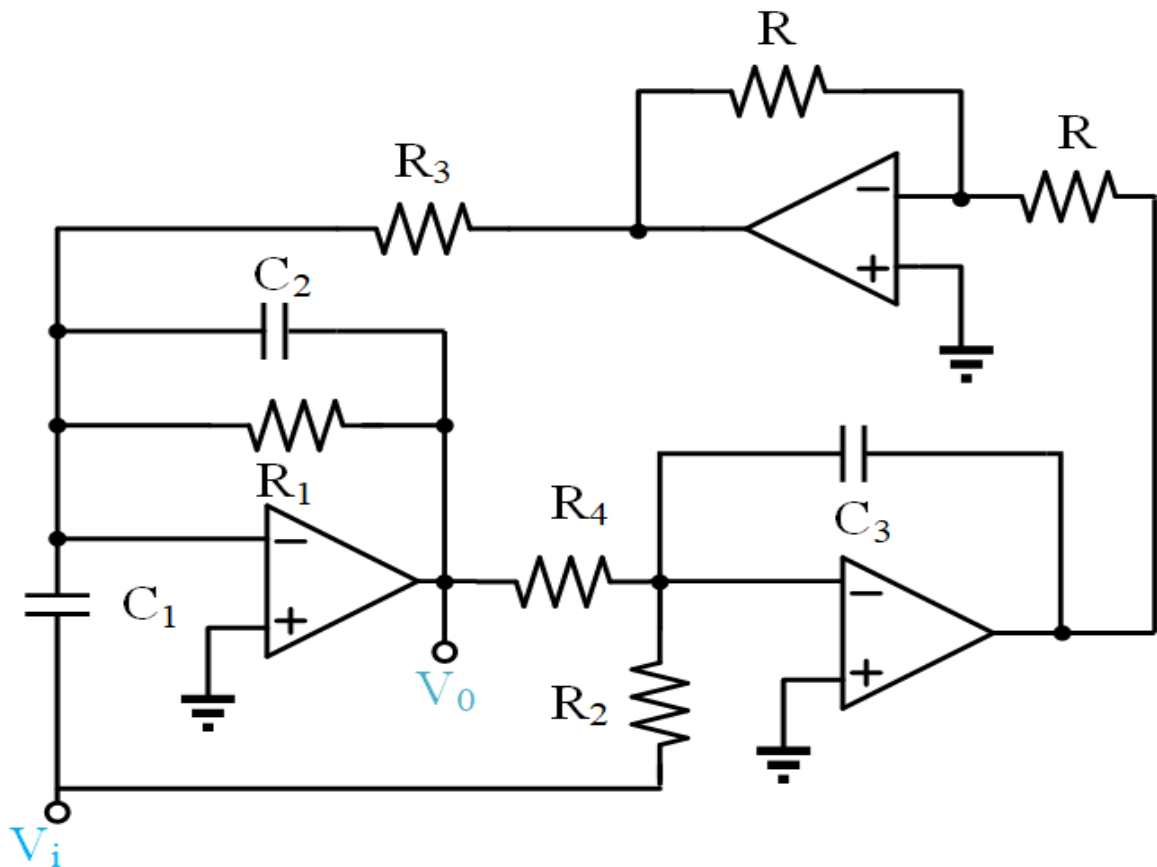


Fig: 13

2.5.1 For High Notch Depth

$$\begin{aligned}
 p &= \frac{1}{|T_{(non-ideal)}(j\omega_0)|} \\
 &= 1 + \frac{C_3}{C} \left(\frac{A}{2q} + 1 \right) \\
 &= 1 + \sqrt{\frac{C_3}{C}} \left(\frac{A}{2Q} + \sqrt{\frac{C_3}{C}} \right)
 \end{aligned}$$

2.5.2 Tabulation of R and C Values:

Parameters	Values
C1, C2	1pF
C3	10pF
N	15
q	1
R	176.5K

2.5.3 Implementing higher resistance:

- For realizing higher value of resistance a R-2R ladder is implemented as shown in figure.

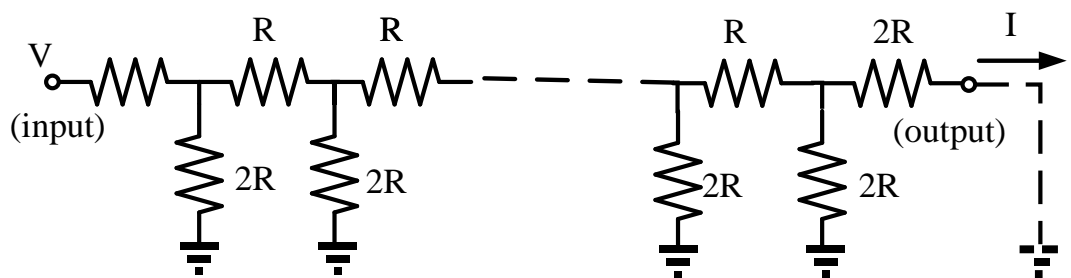


Fig: 14

- The capacitor values are also chosen to be minimum to reduce power consumption.
- As capacitor will act as load.

Chapter 3

Background of OTAs

Operational amplifiers are amplifiers (various forms of controlled sources) with a very large forward gain (gain > 80dB), the closed loop transfer function is independent of the gain of the amplifier. For CMOS on chip designs we conventionally design an Operational Transconductance Amplifier (OTA) as opposed to the discrete operational amplifier.

3.1 OTA Terminology

OPAMP	OTA
High input impedance and low output impedance	High input impedance and output impedance.
Modelled as a voltage controlled voltage source because of the above property.	Modelled as a voltage controlled current source.
Used with external feedback for feedback circuits. Used as an buffer. Contains compensation capacitor in its circuitry between the 2 stages (Miller Compensation).	All nodes are at low impedance except for the input and output nodes.
OpAmp becomes unstable with large load capacitance.	Better Frequency capabilities than Op-Amp. As load capacitance increases the phase margin increases and the OTA is stable.
An OTA with output buffer is an OPAMP.	Generally a single state design.

Gain: For any CMOS topology the gain of the circuit is given by the product of its transconductance and the output resistance of the load structure. The gain is strongly dependent on the frequency of

the input signal. At higher frequencies the inherent parasitic capacitances of the circuit reduce the gain. The gain expression can be given as

$$A_v = g_m * R_{out} \quad (3.1)$$

Where g_m represents the transconductance and R_{out} represents the output resistance of the circuit. *Unity Gain Bandwidth*: This specifies the frequency at which the amplifier gain is unity. The maximal capacitance at the output node gives this specification. There is always a trade-off in achieving high gain and high bandwidth as the high gain-bandwidth for any amplifier is constant for a particular design .

$$f_u = \frac{g_m}{2\pi C_l} \quad (3.2)$$

Where f_u represents the unity gain bandwidth and g_m represents the transconductance of the circuit and C_l represents the load capacitance.

Phase Margin: The phase margin (PM) will determine the stability of an amplifier. Higher values of PM will allow the output signal to achieve steady state without much ringing. Lower values will cause ringing at the output. In our design we require $PM > 60^\circ$.

$$PM = 180 - \arctan\left(\frac{f_u}{f_{dp}}\right) - \arctan\left(\frac{f_u}{f_{ndp}}\right) \quad (3.3)$$

Where f_{dp} is the dominant pole and f_{ndp} are the non-dominant poles in the amplifier transfer function. This equation has ignored the zeros in the amplifier transfer function.

Common Mode Input Range: This is an important parameter at the input of the circuit. The saturation voltage of the bias architecture, the saturation voltage, and V_{GS} voltage headroom of the transconductance structure define the CMIR. An approximate expression can be given as

$$CMIR = V_{DD} - V_{GS} - V_{Dsat} \quad (3.4)$$

Similarly Differential mode input range (DMIR) is the V_{GS} in the circuit. The available supply voltage V_{DD} defines the type of configuration which can be used for obtaining highest CMIR.

Output Swing: This specification relates to the output of the amplifier. The saturation voltage of the load structure mainly defines the output swing of the amplifier. In general the cascode structures results in a low output swing as more number of transistors as stacked under each other and the V_{DSSat} subtracted from the V_{DD} provides the output voltage swing

$$ODR = V_{DD} - \sum V_{DSSat} V_{SSat} \quad (3.5)$$

Static Current Consumption: The product of the current in all the amplifier branches and the supply voltage defines this specification. Careful design needs to be done if the power budget allocated is very low. For decreasing the power consumption, the OTAs can be operated in different regions of operation.

Slew Rate: The output capacitance and the current flowing in the output branch defines this parameter. High Slew rate designs requires high values of current which may affect other specifications in the amplifier design.

$$SR = \frac{I_{out}}{C_{load}} \quad (3.6)$$

The speed of an amplifier is dependent on the equivalent RC constant at the output node. It also depends on the current sourcing/sinking capability at the output. Thus it is a strong function of the internal capacitances and currents in the amplifier branches.

Common Mode Rejection Ratio (CMRR): The common mode gain is given by the gain of the common mode input to the output. The Common mode rejection ratio is the difference of the differential gain from the common mode gain. The CMRR should be very high such that the cancellation of the signals is proper. The common mode gain is given by

$$A_{CM} = g_m * R_{out} \quad (3.7)$$

$$CMRR = A_{DM} - A_{CM} \quad (3.8)$$

The A_{CM} represents the common mode gain, g_m represents the common mode transconductance and R_{out} represents the common mode output resistance. A_{DM} represents the differential mode gain. CMRR is given by the difference of common mode and differential mode gain.

3.2 Different OTA configuration

Cascode circuits are widely used for increasing the gain and output resistance of the OTA. Many positive feedback techniques [1], [2] are used for enhancing the gain by increasing the output resistance. For high UGB and high gain, many architectures has been reported in the literature such as Differential Amplifier, Folded Cascode (FC), Enhanced Fully Differential Folded cascode (EFC), Recycling Folded Cascode (RFC) and Improved Recycling Folded Cascode (IRFC).

3.2.1 Telescopic Differential Amplifier

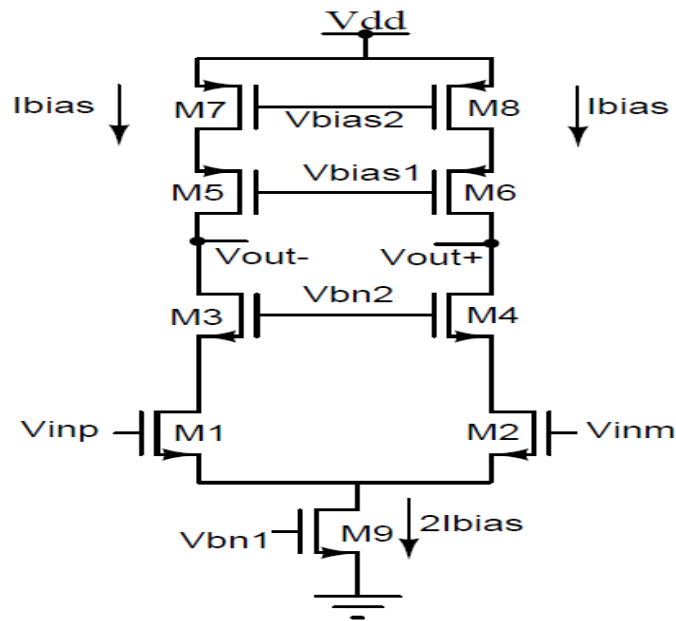


Fig 3.1 Telescopic Differential Amplifier

The NMOS type differential equation is shown in the Fig.2.1. M1 and M2 are the input transistors. M3 and M4 are the Cascode transistors used to increase the resistance of the current source. The half circuit of the differential amplifier is shown in Fig.2.2.

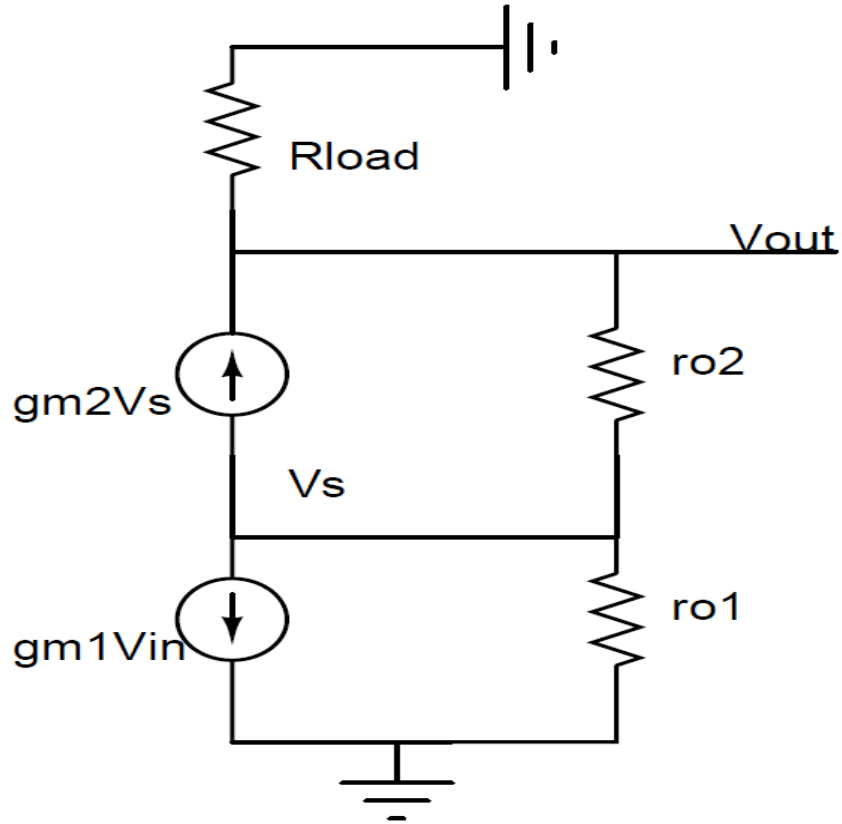


Fig 3.2 Small signal equivalent of Telescopic OTA

DC Gain

The gain is given by

$$A_v = G_m * R_{out} \tag{3.9}$$

where G_m represents the transconductance and R_{out} represents the output resistance of the differential amplifier.

The transconductance of the telescopic differential amplifier is given by

$$I_{out} = g_{m1}V_{in} \tag{3.10}$$

$$G_m = g_{m1} \tag{3.11}$$

Where g_{m1} is the transconductance of the input transistor M1 of the differential amplifier.

The output impedance R_{out} of the telescopic differential amplifier is given by

$$R_{out} = (g_{m3}r_{o3}r_{o1}) || (g_{m5}r_{o5}r_{o7}) \quad (3.12)$$

Frequency Response: There are two poles in the telescopic differential amplifier. One is non dominant and other is the dominant pole.

1. Dominant pole-: The dominant pole exists at the output node as the resistance and the capacitance at the output node is very high. The pole frequency is given by

$$\omega_{p1} = \frac{1}{R_{out} * C_{load}} \quad (3.13)$$

$$C_{load} = C_l + C_{DS4} + C_{DS6} + C_{GD4} + C_{GD6}$$

R_{out} is the output impedance and C_{load} is the output capacitance of the telescopic differential amplifier.

2. Non-dominant Pole-: The non dominant pole exists at the cascode node of the differential amplifier. The non dominant pole frequency is given by

$$\omega_{p2} = \frac{1}{R_c * C_c} \quad (3.14)$$

$$R_c = \frac{1}{g_{m3}}$$

The resistance at the cascode node is given by R_c and capacitance is given by C_c . The ω_{p2} is at a very high frequency which leads to a very high phase margin.

Common Mode Gain-:

The common mode gain is found by sorting the output nodes and input nodes. The half circuit for calculating the common mode gain is shown in Fig.2.3 .

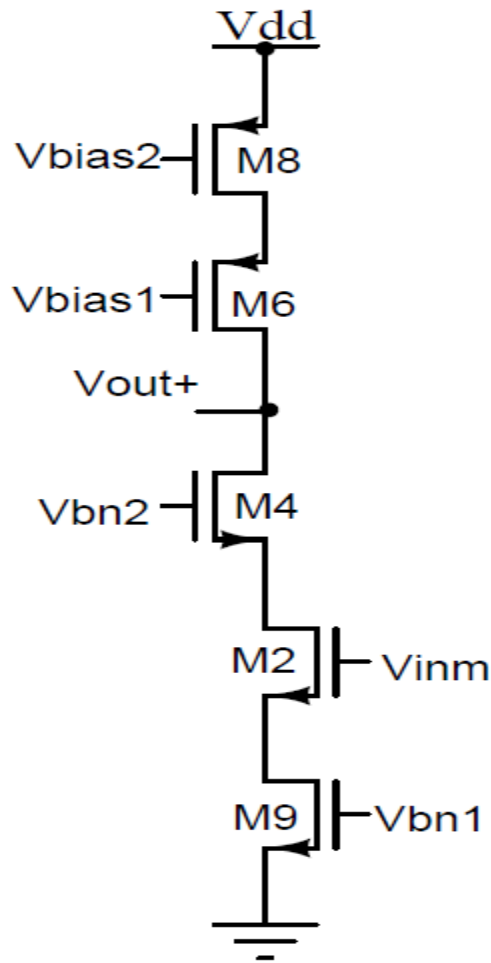


Fig: 3.3 Half circuit for calculation of common mode gain of the Telescopic OTA

In case of differential signal the transistor M9 does not come into effect as its drain node acts as a virtual ground. But in case of common mode signal M9 acts as a source degeneration transistor for M2. Due to which the input transconductance decreases and the common mode gain decreases.

The common mode gain is given by

$$A_{cm} = -\frac{g_{m2}}{(1 + 2 * g_{m2} * r_{09})} * \left(\frac{g_{m4} r_{04} (r_{02} + r_{09})}{2} \right) \parallel \left(\frac{g_{m6} r_{06} r_{08}}{2} \right) \quad (3.15)$$

Where A_{cm} is the common mode gain of the telescopic differential amplifier. The resistance decreases by two because of the two paths are sorted and both are parallel to each other. As the common mode gain decreases the CMRR increases which leads to a better performance.

Limitations of Telescopic Differential Amplifier

In telescopic differential amplifier the swing at the output node decreases due to a large number of transistors are in series which leads to a consumption of large amount of over drive. To improve the gain of the differential amplifier the cascoding of transistors is done which further leads to decrease in the signal swing at the output. This limitation is solved by using folded cascode OTA.

3.2.2 Folded Cascode OTA

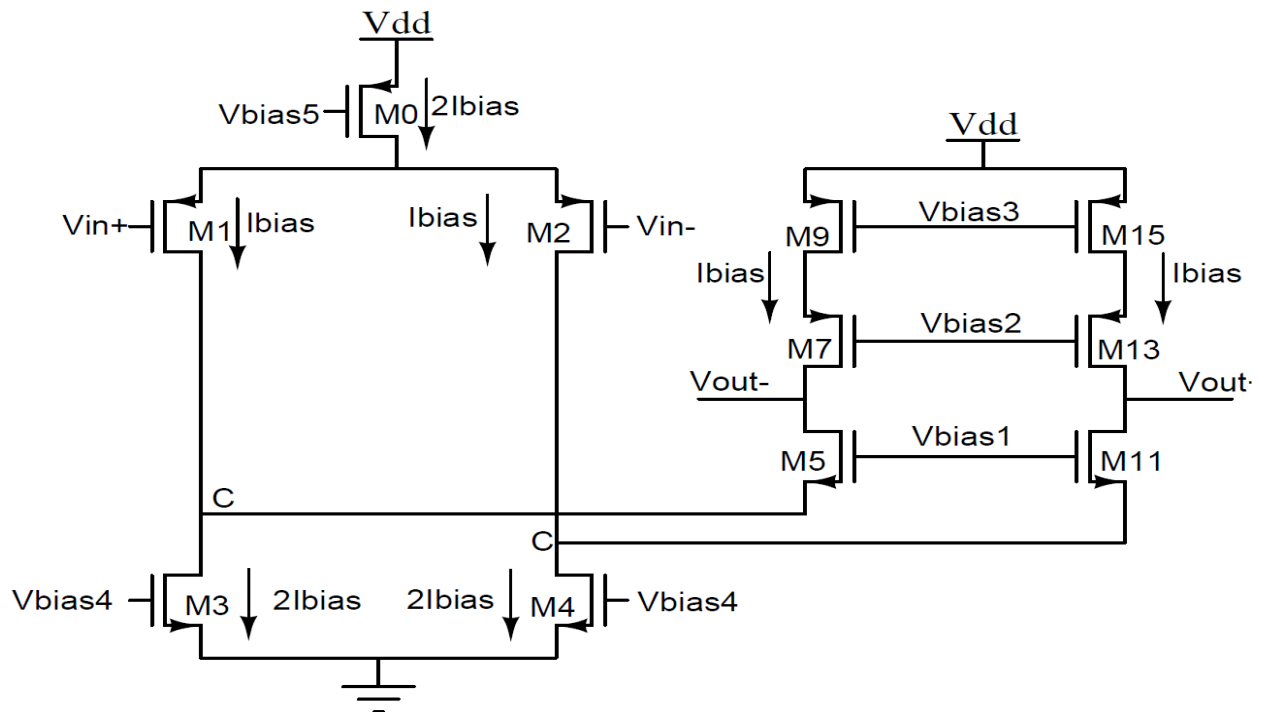


Fig 3.3 Differential ended Folded Cascode OTA

A PMOS type folded cascode OTA is shown in Fig.2.4. In PMOS type folded cascode the input drivers are of P-type M1 and M2. The signal generated by the M1 and M2 are given to the

NMOS cascode transistors M5 and M11. M5 and M11 acts as a common gate stage as no incremental current flows through M3 and M4 as it acts as a folding node denoted by 'C'.

The half circuit of the folded cascode is given in the Fig.2.5 below.

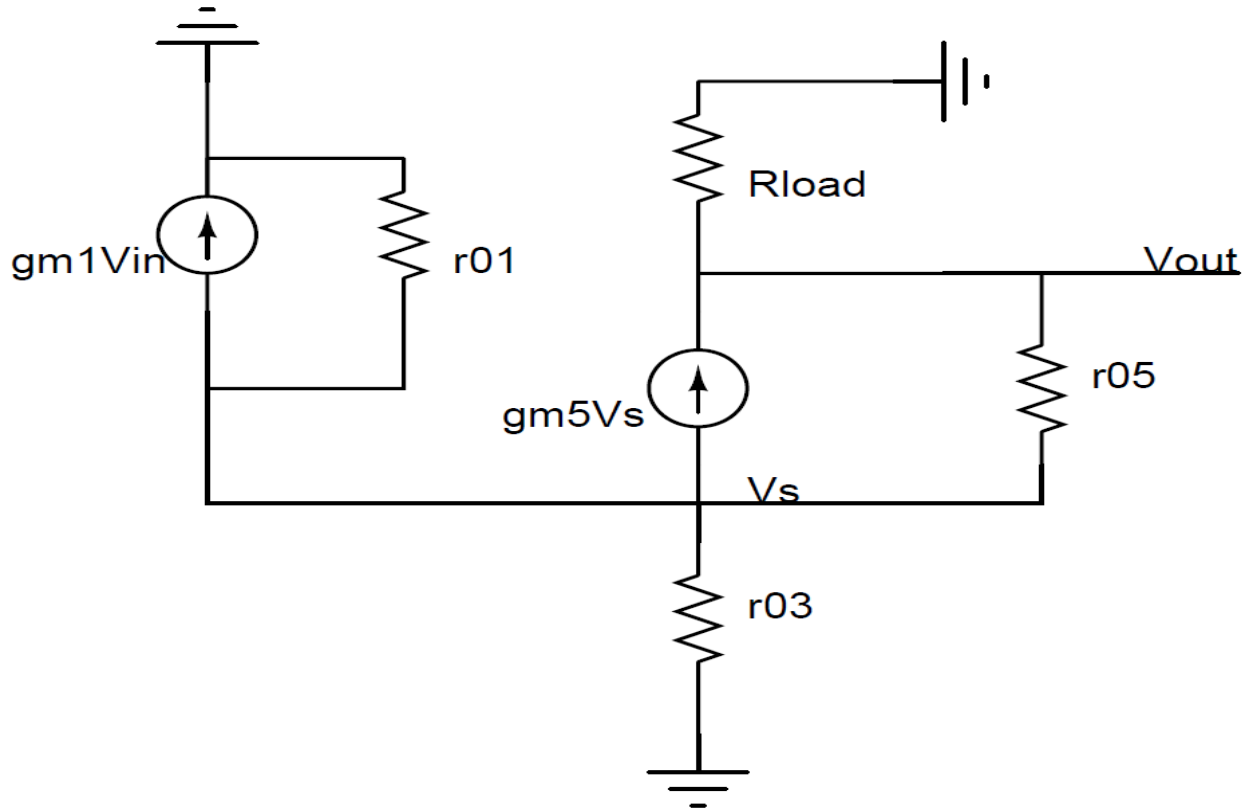


Fig 3.4 Small signal equivalent of Folded cascode OTA

DC GAIN

The DC gain of the folded cascode is given by

$$A_{vfc} = G_{mfc} * R_{outfc} \quad (3.16)$$

The G_{mfc} represents the transconductance and R_{outfc} represents the output impedance of the folded cascode OTA. The transconductance of the folded cascode is given by the input transistor.

$$G_{mfc} = g_{m1a} \quad (3.17)$$

The output resistance of the folded cascode OTA is given by

$$R_{outfc} = g_{m5}r_{o5}(r_{o1a}||r_{o3a})||(g_{m7}r_{o7}r_{o9}) \quad (3.18)$$

Frequency Response

In folded cascode OTA there are two poles. One is dominant pole and other is non dominant pole. The dominant pole is at the output node and the non-dominant pole is at the cascode node of the folded cascode OTA.

1. Dominant Pole

The dominant pole frequency ω_{p1} at the output node is given by

$$\omega_{p1} = \frac{1}{R_{outfc}C_{outfc}} \quad (3.19)$$

$$C_{outfc} = C_l + C_{DS5} + C_{DS7} + C_{GD5} + C_{GD7} \quad (3.20)$$

The capacitance at the output node is given by C_{outfc} . C_l represents the load capacitance of the OTA for which it is designed. The dominant pole frequency is also known as the 3-dB bandwidth of the OTA.

2. Non Dominant Pole

The non dominant pole frequency is given by ω_{p2}

$$\omega_{p2} = \frac{1}{R_c C_c} \quad (3.21)$$

Where R_c represents the cascode resistance and C_c represents the cascode node capacitance at the folding node. The resistance at the cascode node is given by

$$R_{cfc} = \frac{1}{g_{m5}} \quad (3.22)$$

The capacitance at the cascode node is given by

$$C_{cfc} = C_{GS5} + C_{DS3} + C_{DS1} + C_{GD1} + C_{GD3}$$

As the resistance is very low at the cascode node the non dominant pole is at a very high frequency which leads to a higher phase margin. As the phase margin is very high the stability of the system is maintained.

Unity Gain Band Width (UGB)

The UGB is defined as the frequency at which the voltage gain is unity or 0dB. The UGB of the OTA is given by

$$UGB = \frac{g_{m1}}{C_{load}} \quad (3.23)$$

The UGB of the OTA depends upon the input transconductance and the load capacitance. As the load capacitance increases the UGB decreases and the phase margin increases. The UGB increases with the increase in the DC current through the input transistor as the input transconductance increases.

Common Mode Gain of Folded cascode OTA

The common mode gain of the folded cascode OTA is discussed in this section. The transistor M0 for a common mode signal behaves as a resistance r_0 . The output resistance is half for common mode signal compared to the differential signal. The common mode gain equation is given by

$$A_{cm} = G_{mcmfc} * R_{outcmfc} \quad (3.24)$$

$$G_{mcmfc} = -\frac{g_{m1}}{(1 + 2 * g_{m1} * r_0)}$$

$$R_{out} = \left(g_{m5}r_{05} \left(\frac{r_{03}}{2} \parallel \left(\frac{g_{m1}r_{01}r_{00}}{2} \right) \right) \parallel \left(\frac{g_{m7}r_{07}r_{09}}{2} \right) \right)$$

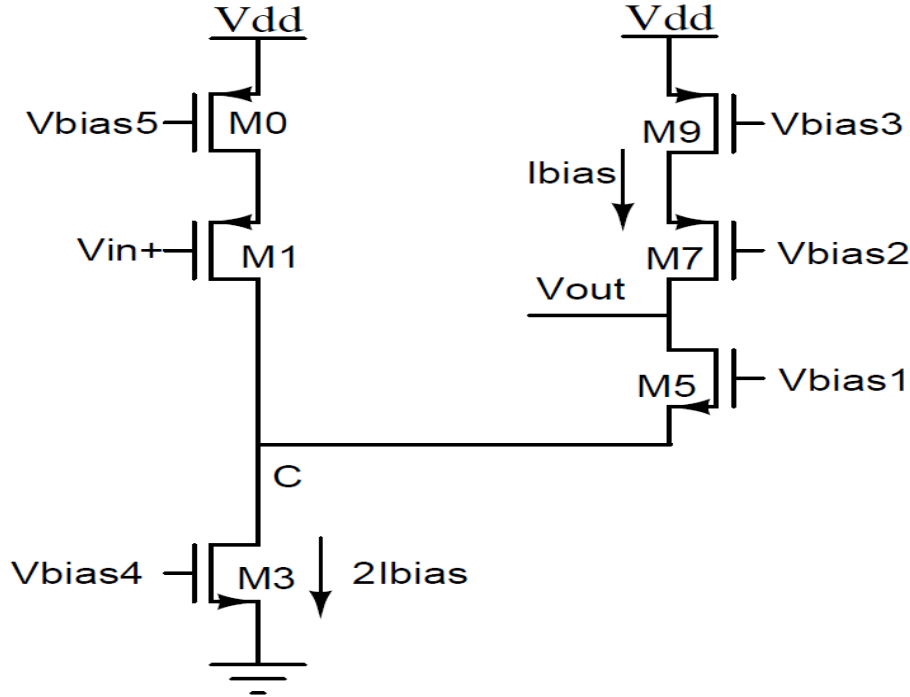


Fig 3.5 Half circuit of Folded Cascode OTA for finding Common Mode gain

3.3 RECYCLIC FOLDED CASCODE OTA

The bias current sources in the conventional FC [3] consume high current, and have large transconductance. However, these current sources don't contribute to the DC gain. In [4], the input transistors of FC are split into two parts (M1a, M1b, M2a, M2b) which conduct fixed and equal currents of $I_b/2$. Next the current source transistor in the FC is replaced by current mirrors M3a:M3b and M4a:M4b at a ratio of K: 1. This architecture is called as the RFC OTA and is shown in Fig.2.7.

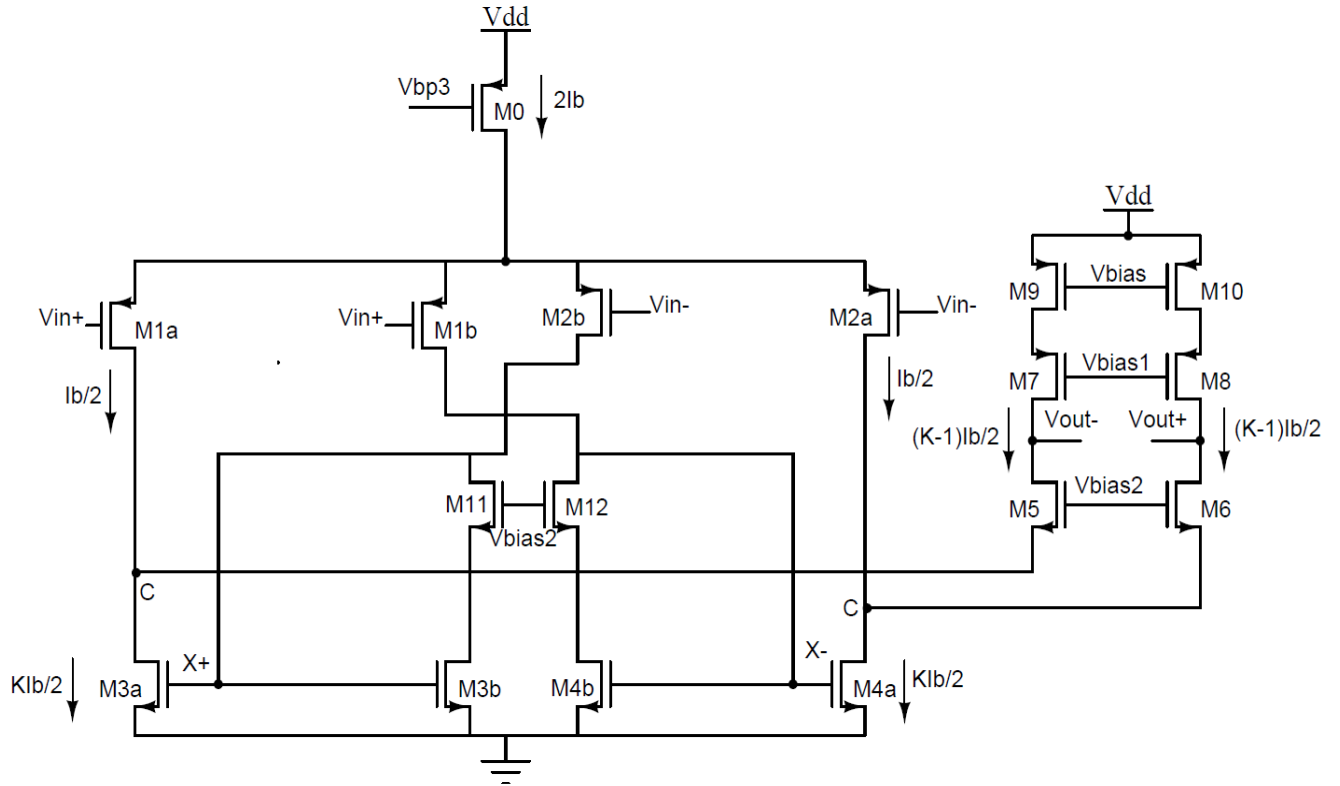


Fig 3.6 Recycling Folded Cascode OTA

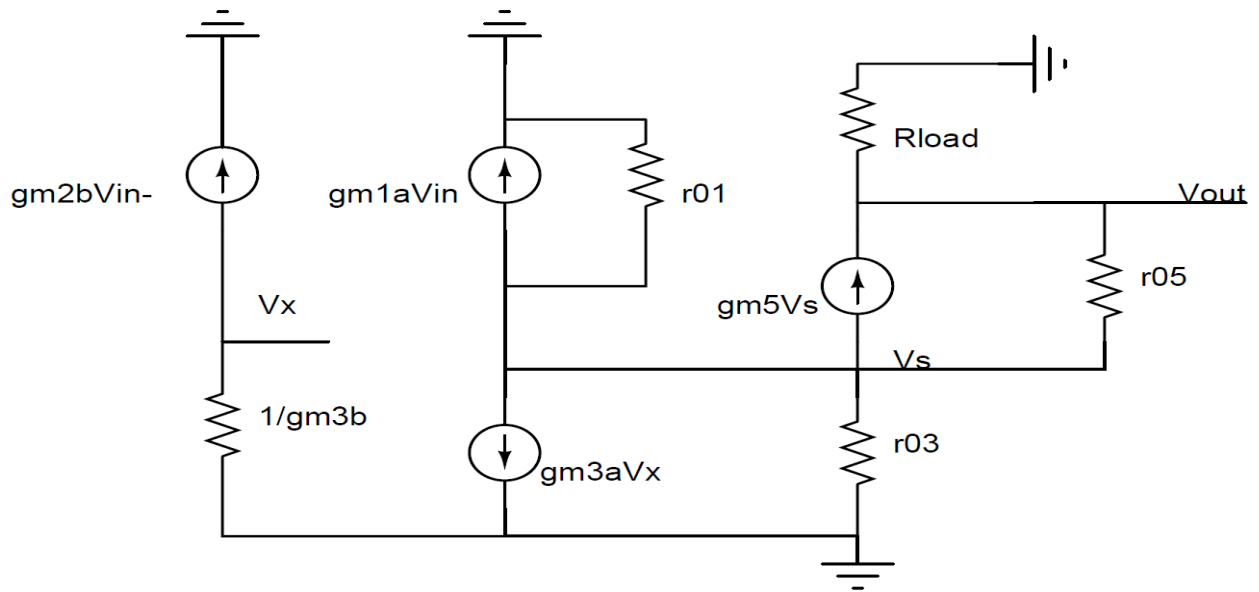


Fig 3.7 Small signal equivalent of Recycling Folded Cascode OTA

DC Gain

The DC gain A_v of the RFC [4] is given by

$$A_v = G_m * R_{out} \quad (3.25)$$

where G_m is the transconductance and R_{out} is the output impedance. The transconductance G_m is given by

$$G_m = I_{out}/V_{i+} \quad (3.26)$$

where the output current I_{out} is given by

$$I_{out} \approx g_{m1a}V_{i+} + g_{m3a}V_{x+} \quad (3.27)$$

From Fig.2.7, it can be seen that transistors M2b and the diode connected transistors M11 and M3b act as a common source amplifier with a voltage gain of approximately -1. Since, the input applied to M2b is in opposite direction, the node X_+ (or X_-) is in the same phase of V_{i+} (or V_{i-})

where

$$V_{x+} \approx -g_{m2b}R_xV_{i-}$$

and

$$R_x = 1/g_{m3b}$$

Hence

$$V_{x+} \approx V_{i+}$$

Substituting V_{x+} in (2.27)

$$I_{out} = g_{m1a}V_{i+} + g_{m3a}V_{i+} \quad (3.28)$$

Substituting (2.28) in (2.26) gives the small signal transconductance G_m .

$$G_m = g_{m1a} + g_{m3a} \quad (3.29)$$

where

$$g_{m3a} \approx K \cdot g_{m1a} \quad (3.30)$$

The output impedance R_{out} of the RFC OTA is given by

$$R_{out} = g_{m5}r_{05}(r_{01a}||r_{03a})||g_{m7}r_{07}r_{09} \quad (3.31)$$

Using (2.30) and (2.31) in (2.25), A_v is given by

$$A_v \approx g_{m1a}(K + 1) \cdot g_{m5}r_{05}(r_{01a}||r_{03a})||g_{m7}r_{07}r_{09} \quad (3.32)$$

Frequency Response Analysis:

From Fig.2.8, it is observed that there are three poles and one zero. For practical purposes, we need to consider only the poles occurring at the output node and cascode node as the other pole and zero lie far away from origin.

1. Dominant Pole:

Because of high impedance (R_{out}) and large capacitance (C_{out}) at the output node, the dominant pole occurs in this node.

The dominant pole frequency ω_{p1} (f_{-3db}) is given by

$$\omega_{p1} = 1/R_{out}C_{out} \quad (3.33)$$

Where

$$R_{out} \approx g_{m5}r_{05}(r_{01a}||r_{03a})||g_{m7}r_{07}r_{09}$$

and

$$C_{out} = C_l + C_{DB8} + C_{GD8} + C_{GD6} + C_{DB6}$$

2. Non-Dominant Pole:

It occurs in the cascode node C at a very high frequency compared to the dominant pole. Since the output capacitance bypasses the effect of output impedance, an equivalent impedance R_C at the cascode node is approximately $1/g_{m5}$. Hence, the non-dominant pole frequency ω_{p2} is given by

$$\omega_{p2} \approx 1/R_C C_C \quad (3.34)$$

Where

$$C_C \approx C_{GD3a} + C_{GS5} + C_{GD1a} + C_{DB3a} + C_{DB1a} + C_{SB5}$$

The UGB of the OTA is given by

$$UGB = A_V * f_{-3db} \quad (3.35)$$

Using (3.30) & (3.35)

$$UGB \approx g_{m1a}(K + 1)/C_{out} \quad (3.36)$$

From (3.30) & (3.35), it is observed that the A_V and UGB are enhanced by a factor of 2 (for $K = 3$ and g_{m1} of FC = $2g_{m1a}$), compared to the FC for the same power and area.

Common Mode Gain

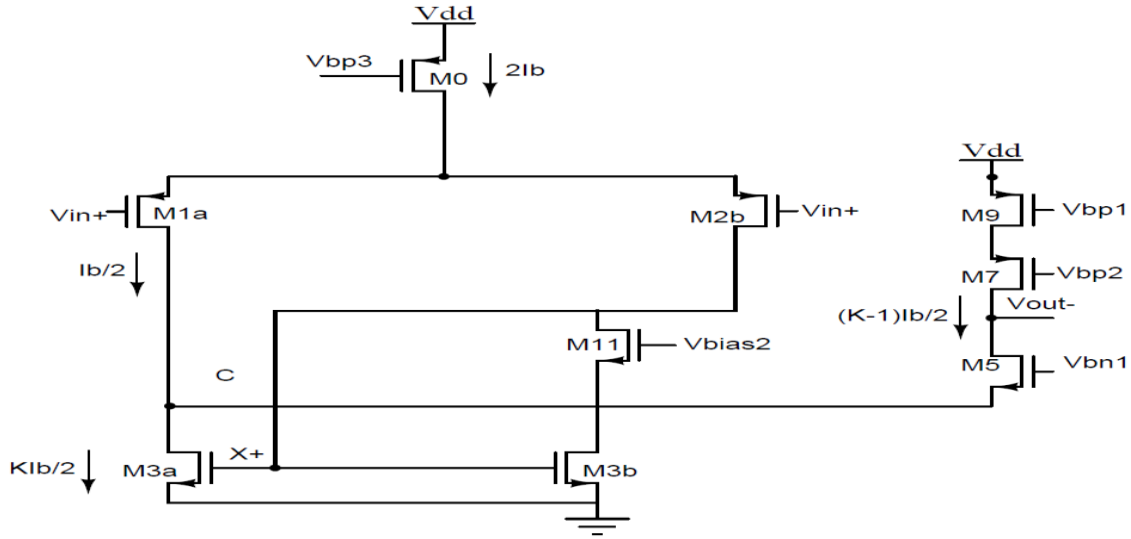


Fig 3.8 Half Circuit equivalent for finding Common Mode Gain

The common mode operation of RFC is described next. For common mode input, the signal at the gate of M1a and M3a are out of phase. So as the common mode input decreases the current in M1a increases and the current in M3a also increases because of out of phase. So, if the small signal current coming from the M1a is ΔI_d then current going through M3a is $K\Delta I_d$. Hence $(K-1)\Delta I_d$ is now coming from the output node to the cascode node. Hence, the transconductance and output resistance may be shown to be given by (3.37) and (3.38).

$$G_m = \frac{I_{out}}{V_{in}} \approx 2g_{m1a}(K-1) \quad (3.37)$$

$$R_{out} = \left(\frac{g_{m9}r_{o9}r_{o13}}{2} \right) || g_{m5}r_{o5}(r_{o1a} || r_{o3a}) \quad (3.38)$$

Hence, the common mode gain is given by (21)

$$A_{cm} = G_m * R_{out}$$

$$A_{cm} = 2g_{m1a}(K - 1)\left(\frac{g_{m9}r_{o9}r_{o13}}{2}\right) || g_{m5}r_{o5}(r_{o1a} || r_{o3a})$$

3.4 Improved Recycling Folded Cascode Amplifier

To improve the signal swing at the current mirror node X+ (or X-), the DC and AC path are separated in IRFC proposed in [5] and is shown in Fig.2.10. To achieve this, the transistors M11, M3b and M12, M4b are divided into two parts M11a, M11b, M3b1, M3b2 and M12a, M12b, M4b1, M4b2 respectively. The paths M11b, M3b2 and M12b, M4b2 have high impedance ($g_{m11b}r_{o11b}r_{o3b2}$). The paths M11a, M3b1 and M12a, M4b1 and have low impedance ($1/g_{m3b1}$). The small signal current flows through the low impedance path. The ratio of DC currents flowing through the high impedance and low impedance paths is a : b and the transconductance of M11a, M3b1 is scaled by ‘a’ where $a < 1$. The signal flowing through the current mirror node becomes larger compared to that of the RFC due to the increase in the resistance of the small signal path.

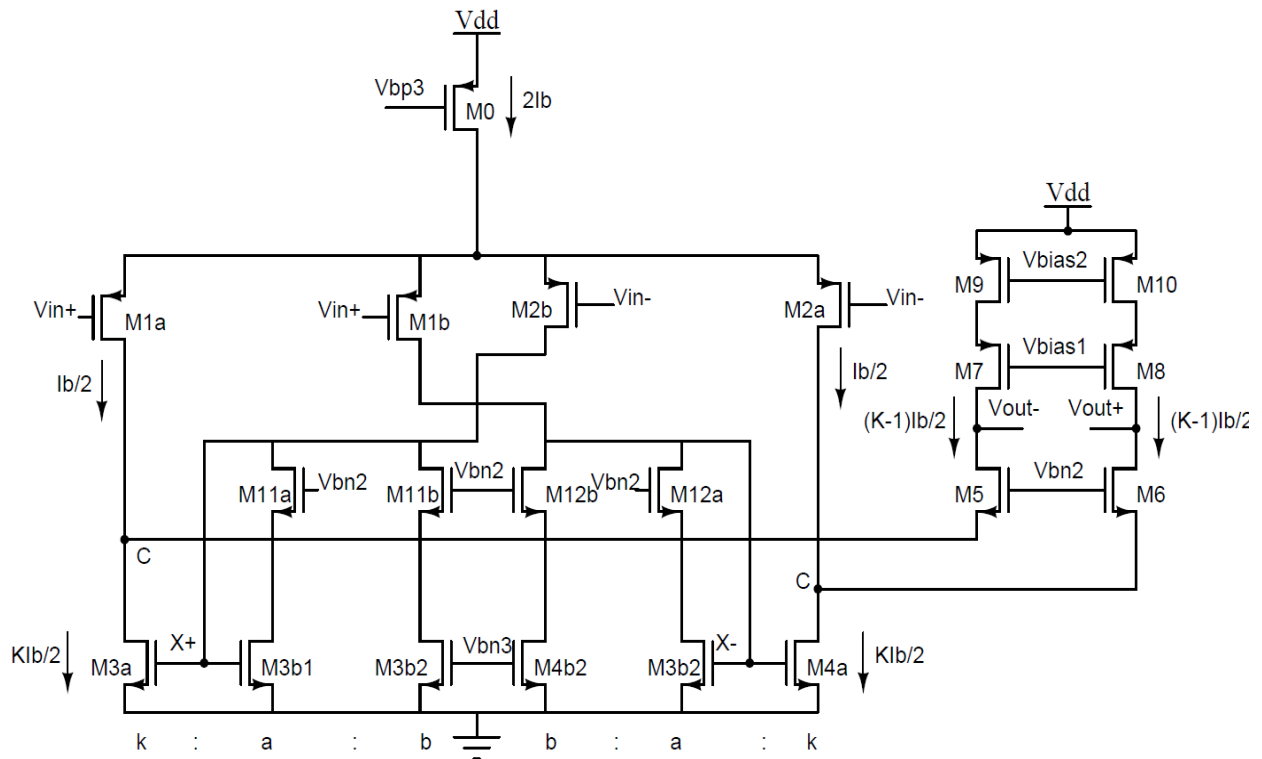


Fig 3.9 Improved Recycling Folded Cascode OTA

DC Gain

Generally the DC gain A_v of the OTA is given by (2.39)

$$A_v = G_m * R_{out} \quad (3.39)$$

where G_m is the transconductance and R_{out} is the output impedance.

The transconductance of G_{mIRFC} is given by

$$G_{mIRFC} = I_{out}/V_{in+} \quad (3.40)$$

where the output current I_{out} is given by

$$I_{out} \approx g_{m1a}V_{in+} + g_{m3a}V_{x+} \quad (3.41)$$

From Fig.3.10, it can be seen that transistors M2b and the diode connected transistors M11a and M3b1 act as a common source amplifier with a voltage gain of approximately $-1/a$. Since, the input applied to M2b is in opposite direction, the voltage at node X_+ (or X_-) has the same phase as that of V_{in+} (or V_{in-})

where

$$V_{x+} \approx -g_{m2b}R_xV_{in-}$$

$$R_x = 1/a \cdot g_{m3b1}$$

Hence

$$V_{x+} \approx \frac{-V_{in-}}{a}$$

Substituting V_{x+} in (3.41)

$$I_{out} = g_{m1a}V_{in+} + \frac{1}{\alpha}g_{m3a}V_{in+} \quad (3.42)$$

Substituting (2.42) in (2.40) gives the small signal transconductance G_m .

$$G_{mIRFC} = g_{m1a} + \frac{1}{\alpha} \cdot g_{m3a} \quad (3.43)$$

Where

$$g_{m3a} \approx K \cdot g_{m1a}$$

The output impedance R_{out} of the IRFC OTA is given by

$$R_{outIRFC} = g_{m5}r_{05}(r_{01a}||r_{03a})||g_{m7}r_{07}r_{09} \quad (3.44)$$

Substituting (2.43) and (2.44) in (2.39) the voltage gain of IRFC OTA is given by (2.45)

$$A_v = g_{m1a}\left(\frac{K}{\alpha} + 1\right) * g_{m5}r_{05}(r_{01a}||r_{03a})||g_{m7}r_{07}r_{09} \quad (3.45)$$

Frequency Response Analysis

From Fig.3.11, it is observed that there are three poles and one zero. For practical purposes, we need to consider only the poles occurring at the output node and cascode node as the other pole and zero lie far away from origin.

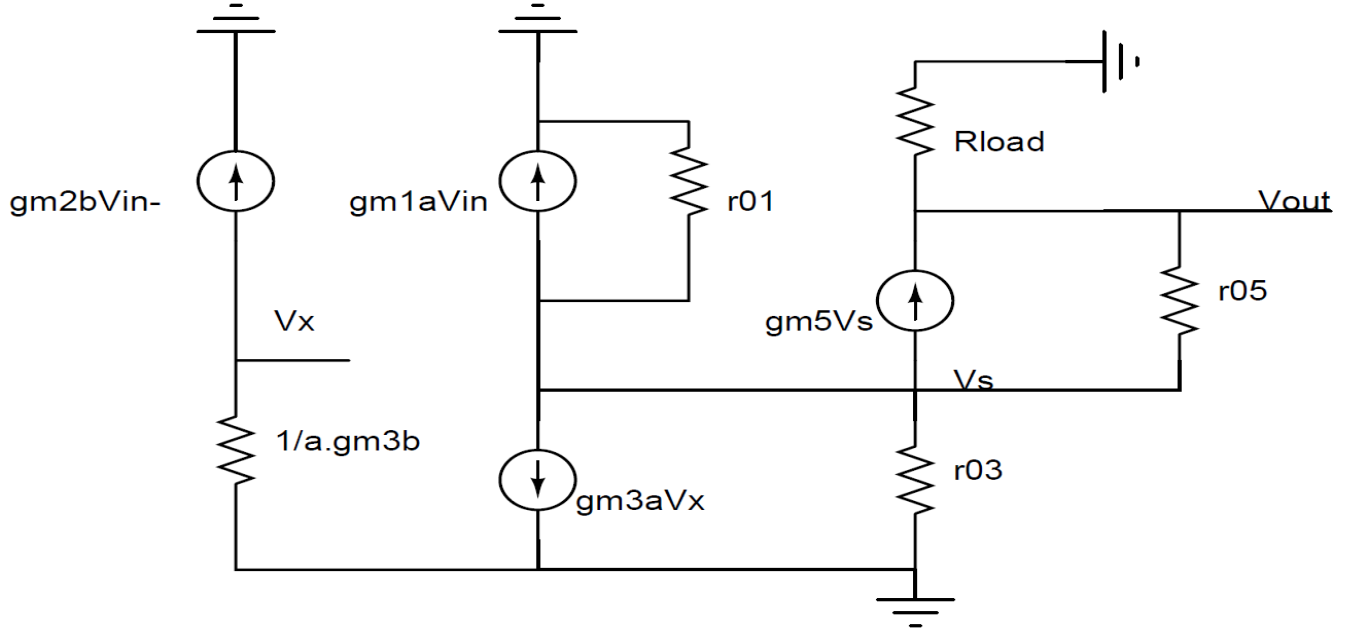


Fig 3.10 Small Signal equivalent of IRFC

1 Dominant Pole:

Because of high impedance ($R_{outIRFC}$) and large capacitance (C_L) at the output node, the dominant pole occurs in this node.

The dominant pole frequency ω_{p1} (f_{-3db}) is given by

$$\omega_{p1} = 1/R_{outIRFC}C_L \quad (3.46)$$

where

$$R_{outIRFC} \approx g_{m5}r_{o5}(r_{o1a}||r_{o3a})||g_{m7}r_{o7}r_{o9}$$

and

$$C_{out} = C_l + C_{DB8} + C_{GD8} + C_{GD6} + C_{DB6}$$

2. Non-Dominant Pole:

It occurs in the cascode node C at a high frequency compared to the dominant pole. Since the output capacitance bypasses the effect of output impedance, an equivalent impedance R_C at the cascode node is approximately $1/g_{m5}$. Hence, the non-dominant pole frequency ω_{p2} is given by

$$\omega_{p2} = 1/RC.CC \quad (3.47)$$

where

$$C_c \approx C_{GD3a} + C_{GS5} + C_{GD1a} + C_{DB3a} + C_{DB1a} + C_{SB5}$$

The UGB of the OTA is given by

$$UGB = Av * f_{3db} \quad (3.48)$$

Substituting

$$UGB \approx g_{m1a} \left(\frac{K}{a} + 1 \right) / C_L \quad (3.49)$$

From (3.45) & (3.49), it is observed that the A_V and UGB are enhanced by a factor of $1/a$, compared to the RFC [4] for the same power and area.

Common mode gain of IRFC

In the IRFC OTA, for common mode input, the signal at the gate of M1a and M3a are out of phase. So, as the common mode input decreases, the current in M1a increases and the current in M3a also increases because of out of phase. So, if the small signal current through the M1a is ΔI_d , then current through M3a is $K/a \Delta I_d$. Hence, a current of $\left\{ \frac{K}{a} - 1 \right\} \Delta I_d$ flows from the output node to the cascode node. Hence, the transconductance and output impedance may be shown to be given by (3.50) and (3.51).

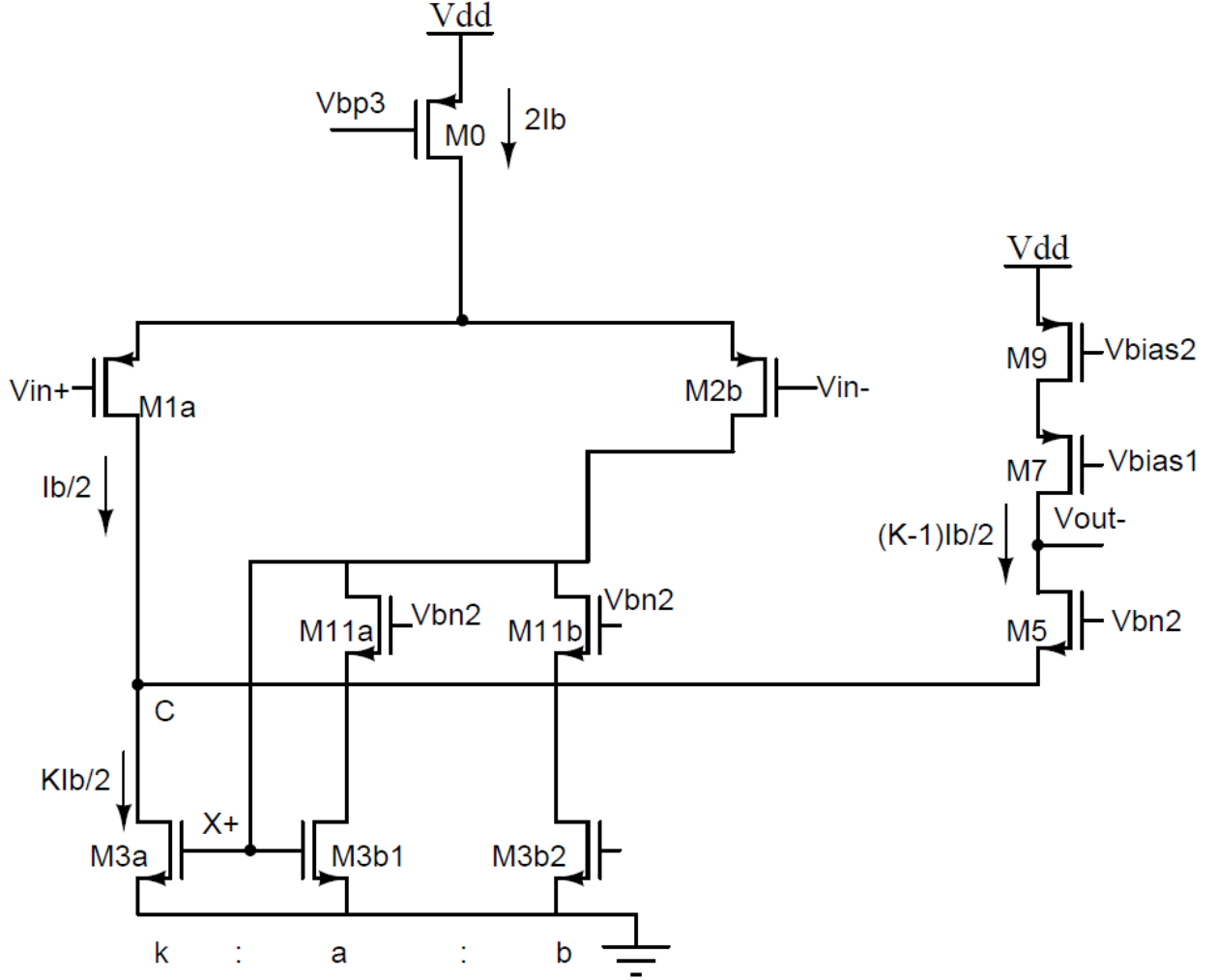


Fig 3.11 Half circuit of IRFC for finding common mode gain

$$G_m = \frac{I_{out}}{V_{in}} \approx g_{m1a} \cdot (K/a - 1) \quad (3.50)$$

$$R_{out} = \left(\frac{g_{m7} r_{o7} r_{o9}}{2} \right) \parallel \frac{g_{m5} r_{o5} (r_{o1a} \parallel r_{o3a})}{2} \quad (3.51)$$

Hence, the CM gain of IRFC is given by (3.52)

$$A_{cmIRFC} = g_{m1a} \cdot \left(\frac{K}{a} - 1 \right) * \left\{ \left(\frac{g_{m7} r_{o7} r_{o9}}{2} \right) \parallel \left(\frac{g_{m5} r_{o5} (r_{o1a} \parallel r_{o3a})}{2} \right) \right\} \quad (3.52)$$

3.5 Comparison of All the OTAs

Performance Parameters	Telescopic Differential	Folded Cascode OTA	Recycling Folded Cascode OTA	Improved Recycling Folded Cascode OTA
Transconductance	High	Low compared to telescopic differential OTA	High compared to Folded Cascode OTA. Similar to Telescopic OTA for $K=3$.	High compared to all the OTAs.
Output resistance	High	Same as that of the Telescopic OTA	Same as that of the Telescopic OTA	Same as that of the Telescopic OTA
Phase Margin	High	High	Low compared to folded cascode OTA due to current mirror node in the signal path.	Low compared to RFC due to a high resistance Path formed by M11,M3b and M12,M4b.
UGB	High	Low compared to Telescopic OTA	High compared to folded cascode OTA. Similar to telescopic for $K=3$.	High compared to all the OTAs
CMRR	High	High	Low compared to Folded cascode due to transconductance of M3a.	Same as that of the RFC.
Signal Swing	Medium	High compared to telescopic OTA.	High compared to telescopic OTA.	High compared to telescopic OTA.
Slew Rate	High	Same as that of the telescopic OTA.	High compared to Folded cascode OTA.	High compared to RFC OTA.

3.6 Application of the OTAs

The OTA is the main block of any system design. The power consumption of the system depends on the power consumed by the OTA. So for low power application the OTA power should be reduced.

The different applications Of the OTA are

1. Buffer, Integrator, etc.
2. Comparators
3. High Performance Analog to Digital Converters
4. OTA-C Filters
5. Switched Capacitor Filters

Chapter 4

4.1 G_m/I_D methodology

4.1.1 Introduction

With the advent of advanced fabrication process the transistor dimensions have reduced drastically. Although the trend towards miniaturization has helped digital circuitry with densely packed transistors, the analog counterpart had to pay the price with decreasing supply voltage headroom, reduced dynamic range, lower gain and similar other attributes.

As a consequence the conventional long-channel equations employed in the analog design were no longer producing desired results. The short channel-noise combined with the need for precise and intuitive design procedure called for a complete characterization of the process technology. A methodology is devised where currents are fixed to arrive at the transistor dimensions to satisfy specifications like gain-bandwidth, low power, area, etc. The g_m/I_D is a ratio obtained by complete characterization of the process for the NMOS and PMOS transistors.

For a given set of design specifications, we may start our design by using MOSFET square law equation. However the modern device models given by BSIM model, or any other models are too complicated for hand analysis. There is a huge discrepancy between modern CMOS models and traditional equations. All these pose a challenge for a modern circuit designer, as shown in Fig.4.1.

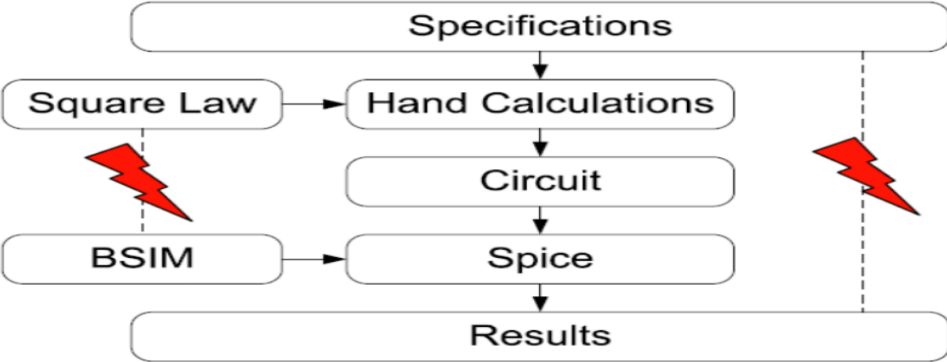


Fig. 4.1 The Problem while designing

The lack of good hand analysis models to design circuits forcing many designers to give up hand calculation /analysis, and iterate the design problem in simulators to meet the specifications. So design should be based on systematic design analysis and reasonable considerations, the simulator is just a calculator to check the design meet the specifications or not. From a designers point of view we should understand the optimizations to be done for proper operation of the circuit and not a pile of equations which does not give any design intuition.

4.2.2 Different regions of Operation

The long-channel design has different set of equations which govern each region of operation. The overdrive voltage V_{ov} is a key parameter which defines the region the device is operating in. The g_m/I_D characterizes the performance of a transistor in all regions of operation. The following section develops the long-channel equations of the transistor. From these equations we derive the figures of merits for the g_m/I_D method.

Triode region

$$I_D = \mu_n C_{ox} \frac{w}{l} \left[(V_{gs} - V_T) - \frac{V_{DS}}{2} \right] \cdot V_{DS} \quad (4.1)$$

Saturation region

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{w}{l} (V_{gs} - V_T)^2 \quad (4.2)$$

Transconductance

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu C_{ox} \frac{W}{L} (V_{GS} - V_T) = \mu C_{ox} \frac{W}{L} V_{OV} \quad (4.3)$$

$$g_m = \sqrt{2I_D \mu_n C_{ox} \frac{W}{L}} = \frac{2I_D}{V_{ov}} \quad (4.4)$$

Output conductance with channel length modulation

$$g_{as} = \frac{\partial I_D}{\partial V_{DS}} = \frac{\partial}{\partial V_{DS}} \left[\frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \right] \quad (4.5)$$

$$g_{DS} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 \lambda = \frac{\lambda I_D}{1 + \lambda V_{DS}} = \lambda I_D \quad (4.6)$$

The performance of any analog circuit can be broadly divided into its large signal and small signal characteristics. The current I_D determines the power dissipation; voltage V_{DS} and available swing (both the ICMR and ODR); the transconductance g_m signifies speed and voltage gain; the intrinsic impedances C_{GS} , C_{GD} , C_{DB} determine the speed and the output impedance; r_0 the voltage gain of the circuit. Summarizing above we have

D.C. Voltage Gain

$$A_{DC} = g_m * r_0 \quad (4.7)$$

Bandwidth

$$f_{transit} = \frac{1}{2\pi R_{in} C_{GG}} \quad (4.8)$$

Power Dissipation

$$P = V_{DD} * I_D \quad (4.9)$$

Figure of Merits

Some figure of merits can be defined for the technology characterization in the g_m/I_D - based method.

Transconductance Efficiency

$$\frac{g_m}{I_D} = \frac{2}{V_{ov}} \quad (4.10)$$

Transit Frequency

$$\frac{g_m}{C_{GG}} = \frac{3\mu V_{ov}}{2L^2} \quad (4.11)$$

Intrinsic Gain

$$\frac{g_m}{g_{ds}} = \frac{2}{\lambda V_{ov}} \quad (4.12)$$

The equations in the right hand side are derived from the square law equations. In saturation there are three regions of operation depending upon the effective voltages applied across the gate of the transistor.

Weak Inversion

$$v_{gs} - v_t < -0.72 \quad (4.13)$$

Moderate Inversion

$$-0.72 < v_{gs} - v_t < 0.25 \quad (4.14)$$

Strong Inversion

$$v_{gs} - v_t > 0.25 \quad (4.15)$$

The g_m/I_D Vs V_{gs} curve for NMOS in different regions of operation using 90nm CMOS technology is shown below.

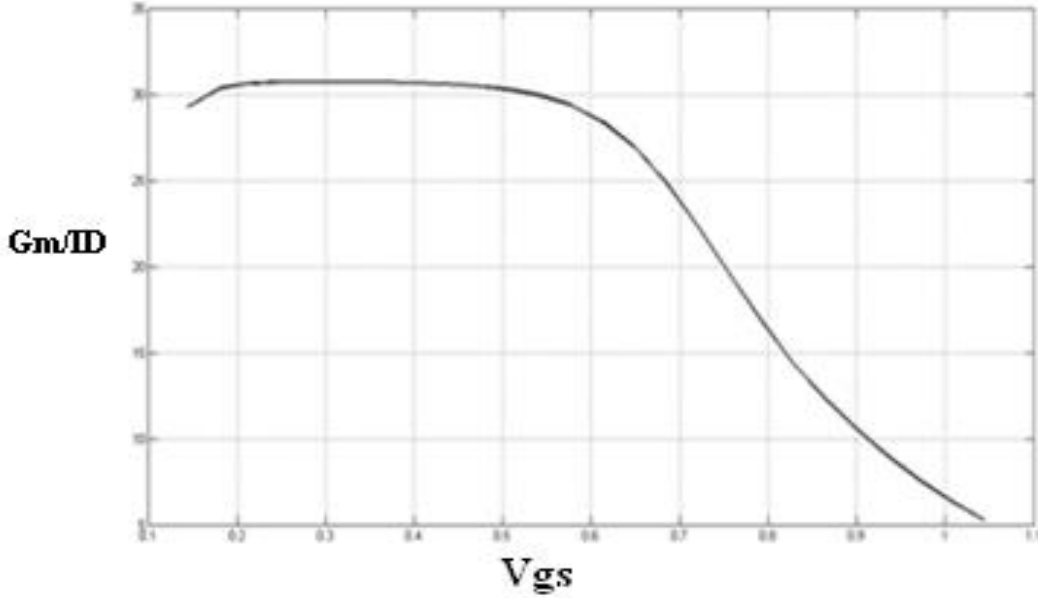


Fig. 4.2 Gm/Id vs Vgs plot

4.2.3 Weak Inversion

Weak inversion occurs for MOSFETs operating at sufficiently low effective gate-source voltages ($V_{\text{eff}} = V_{\text{GS}} - V_{\text{T}} < -72\text{mV}$) where the gate-source voltage, V_{GS} , is below the threshold voltage V_{T} , by at least 72mV for a typical bulk CMOS at room temperature. In this region, the channel is weakly inverted and drain diffusion current dominates. MOS drain current in weak inversion is proportional to the exponential of the effective gate-source voltage. Weak inversion drain current is approximated from the EKV MOS model.

$$I_D(WI) = 2n\mu C_{ox} U_T^2 \left(\frac{W}{L}\right) \left(e^{\frac{V_{GS}-V_T}{nU_T}}\right) \quad (4.16)$$

W and L are the effective channel width and length, μ is the channel carrier mobility, and C'_{ox} is the gate oxide capacitance per unit area. In weak inversion n is related to the capacitive voltage division between the gate voltage and silicon surface potential resulting from the gate oxide, depletion, and interface state capacitances. In weak inversion, n is expressed by [6]

$$n(WI) = \frac{C'_{ox} + C'_{DEP} + C'_{INT}}{C'_{ox}} \quad (4.17)$$

In weak inversion, n is approximately 1.4-1.5 for typical bulk CMOS process, but can be as low as 1.1 for fully depleted Silicon-on-insulator (SOI) CMOS process where there is little substrate effect.

The transconductance efficiency in weak inversion is found to be

$$\frac{g_m}{I_D} = \frac{1}{n U_T} \quad (4.18)$$

The g_m and g_m/I_D in weak inversion are independent of MOS sizing and process parameters, except for dependence on n . g_m only depends on the DC biasing current I_D . The exponential current voltage relationship in weak inversion results in optimally high transconductance efficiency. Unfortunately, weak inversion operation requires a large MOS shape factor. This results in large gate area, high gate capacitance and relatively poor circuit bandwidth [6].

4.2.4 Strong Inversion

Strong inversion occurs for MOSFETs operating at sufficiently high effective gate-source voltages where the gate source voltage is above the threshold voltage by at least 225mv for a typical bulk CMOS process at room temperature. Here the channel is strongly inverted and drain drift current dominates. Strong inversion drain current, excluding the small geometry effects like velocity saturation and VFMR effects is proportional to the effective gate source voltage [6].

The transconductance g_m in the strong inversion is independent of MOS sizing and process parameters, depending only on the DC bias conditions, I_D and V_{eff} . Transconductance efficiency decreases by around 35% at the onset of strong inversion compared to weak inversion. Transconductance efficiency continues to drop further as the MOS inversion increases. Decreasing transconductance efficiency and increasing drain source saturation voltage are disadvantages of the MOS compared to weak inversion. This results in smaller gate area, lower gate capacitances, and relatively good circuit bandwidth since the decrease in capacitance exceeds the decrease in transconductance. The assumption of MOS strong inversion operation, however should always be carefully stated and verified by ensuring sufficient gate source voltage.

MOS drain current and transconductance can drop significantly from the ideal square law relationships in strong inversion due to high field, small geometry effects. The velocity saturation associated with loss of effective carrier mobility caused by high tangential or horizontal electric field between the pinched off drain and source divided by the channel length. As the effective gate-source voltage increases for small channel length devices, the horizontal electric field becomes so high that the average channel carrier velocity begins to drop from its normal value that linearly tracks the electric field. This causes the drain current to drop from its expected strong inversion, square law value [6].

Another effect lowering drain current and transconductance is referred to here as vertical field mobility reduction (VFMR). This describes the loss of effective carrier mobility due to a high normal or vertical electric field, E_y , between the gate and the inverted MOS channel. As the effective gate-source voltage increases, mobile carriers are increasingly attracted closer to the Si-SiO₂ interface where their mobility reduces due to interface states and other imperfections at this interface. The loss of drain current due to VFMR is dominant for devices operating as resistors in the deep linear or deep ohmic region where the effective gate-source voltage is high and the drain-source voltage is low, well below the drain-source saturation voltage. Here, the average carrier velocity is low, resulting in small velocity saturation effects, but the carrier mobility can be significantly reduced due to VFMR associated with the high vertical field.

4.2.5 Moderate Inversion

Between weak and strong inversion, there is a transition region known as moderate inversion where both diffusion and drift current are significant. As anticipated over 25 years ago moderate inversion is an increasingly important region for modern analog MOS design. Moderate inversion offers higher transconductance efficiency and lower drain-source saturation voltage compared to strong inversion, combined with smaller gate area and capacitances and higher bandwidth compared to weak inversion.

The moderate inversion current equation is given as the interpolation equation between weak inversion and strong inversion. The moderate inversion region is free from all velocity saturation and VFMR effects which reduces the transconductance efficiency. It requires a smaller width compared to weak inversion for a constant current, therefore it has a higher bandwidth

compared to weak inversion. The power consumption and signal swing is higher compared to the strong inversion. So this region is more useful as the technology scales down.

4.3 Performance Comparison among different regions of operation

Performance Parameters	Weak Inversion	Moderate Inversion	Strong Inversion
Transconductance	High	Low compared to Weak inversion. High compared to Strong inversion.	Low compared to weak and moderate inversion.
Transconductance Efficiency	High	Low compared to Weak inversion. High compared to Strong inversion.	Low compared to all regions of inversion.
Gain	High	Low compared to Weak inversion. High compared to Strong inversion.	Low compared to all regions of operation.
Capacitance	High	Low compared to Weak inversion. High compared to Strong inversion.	Low compared to all regions of operation.
UGB	Low	High compared to Weak inversion. Low compared to Strong inversion.	High compared to all regions of operation.
Signal Swing	High	Low compared to Weak inversion. High compared to Strong inversion.	Very Low

4.4 Different Types of Models

- Spice models
- PHILIPS model
- SP model(Surface-Potential-Based Compact MOSFET Model)
- PSP model
- EKV model (Enz, Krumenacher, Vittoz)
- BSIM(1,2,3,4) models (Berkeley Short-channel IGFET Model)

4.4.1 Spice models

- These models are not used nowadays, since they are inaccurate for submicron technologies and present discontinuities in current derivatives

4.4.2 PHILIPS model

- The more recent MOS model 11 is a compact surface potential-based model dedicated to design of digital, analog and RF circuits
- Main drawback is that it is a surface potential based model, so model equation becomes complex.

4.4.3 SP model

- SP is surface-potential-based which includes all major short-channel effects.
- G_m/I_d ratio is modeled correctly.
- SP has 113 model parameters.

4.4.4 PSP model

- The model structures of SP and MM11 turned out to be compatible, enabling the merger of both models into a single new model called PSP, that combines the best features of SP and MM11.

4.4.5 EKV model

- The EKV model has been developed as a charge-based physical model.
- Its version 2.6 (level 5) is dedicated to the design of low voltage and low power analog circuits using submicron CMOS technologies.
- The most recent version 3.0 also includes modeling of all relevant effects for RF circuit design. This continuous and compact model shows good accuracy, even though it has a small number of parameters
- It respects the intrinsic source/drain symmetry, introduces the inversion factor as a transistor parameter, and shows the correct behavior in all inversion regions
- Version 3.0 is validated for nanometer technologies down to 65 nm

4.4.6 BSIM (1,2,3,4) models

4.4.6.1 BSIM. V(1,2)

- The BSIM1 and its improved version BSIM2 are threshold voltage-based empirical models, having good accuracy and continuous derivatives.
- The BSIM1 model requires about **60** DC parameters, whereas BSIM2 requires about **90** DC parameters.

4.4.6.2 BSIM.V3

- The next version, referred to as BSIM3, which needed **40** parameters for DC analysis. The derivatives are continuous and the important improvement is that there is one single expression for the drain current.
- Concerning the design of analog circuits, two main problems are reported: less accurate modeling of weak/moderate inversion behavior and incorrect intrinsic capacitances in some regions.

4.4.6.3 BSIM.V4

- BSIM4 was developed as an extension of BSIM3 and it models more physical effects characterizing the sub-100 nm devices. Numerous high frequency and parasitic effects are also added, making it possible to use this model for the design of RF circuits

Chapter 5

OTA Design and Analysis

5.1 The conventional folded cascode Amplifier

Recently, one of the most commonly used architectures, whether as a single-stage or first stage in multi-stage amplifiers, had been the folded cascode (FC) amplifier for its high gain and reasonably large signal swing in the present and future low voltage CMOS processes. Moreover, the PMOS input FC has become the prime choice over its NMOS counterpart for its higher non-dominant poles, lower flicker noise, and input common mode level. The latter allows input switching using a single NMOS transistor in switched-capacitor (SC) applications.

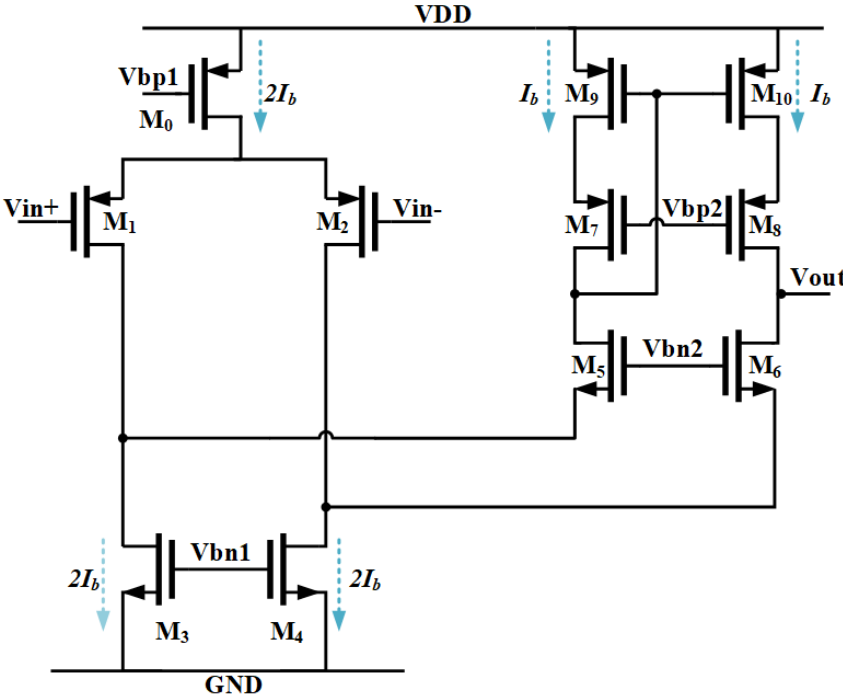


Fig: 5.1 Folded Cascode Amplifier

- Trans-Conductance (G_m)
- Output Impedance
- First Pole

$$G_m = g_{m1}$$

$$R_{out} = (g_{m8}r_{o8}r_{o10}) || (g_{m6}r_{o6}r_{o4})$$

$$\omega_{dominant} = \frac{-1}{(R_{out}C_L)}$$

➤ 2nd Pole

$$\omega_{non-dominant} = \frac{-g_{m6}}{C_{gs6} + C_{gd4}}$$

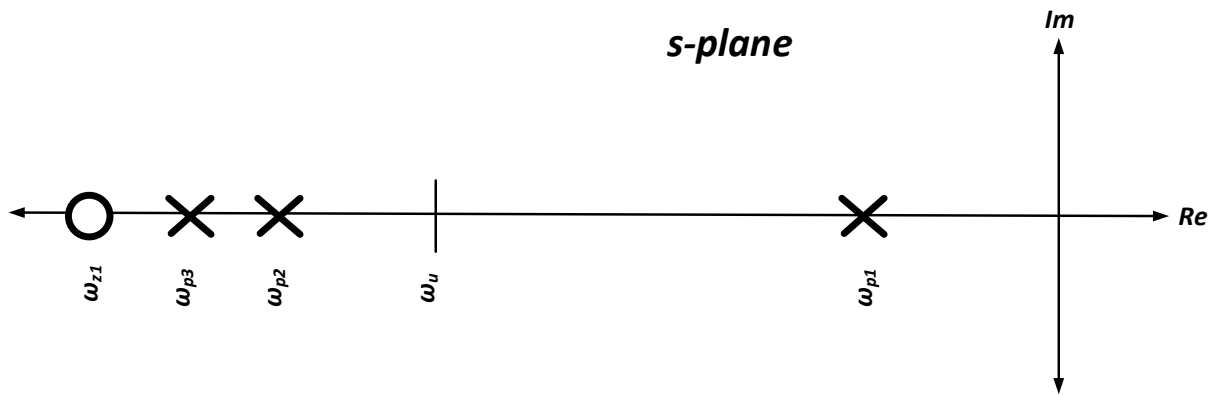


Fig: 5.2 Pole-Zero Location of Folded Cascode Amplifier

5.2 The Recycling Folded Cascode Amplifier

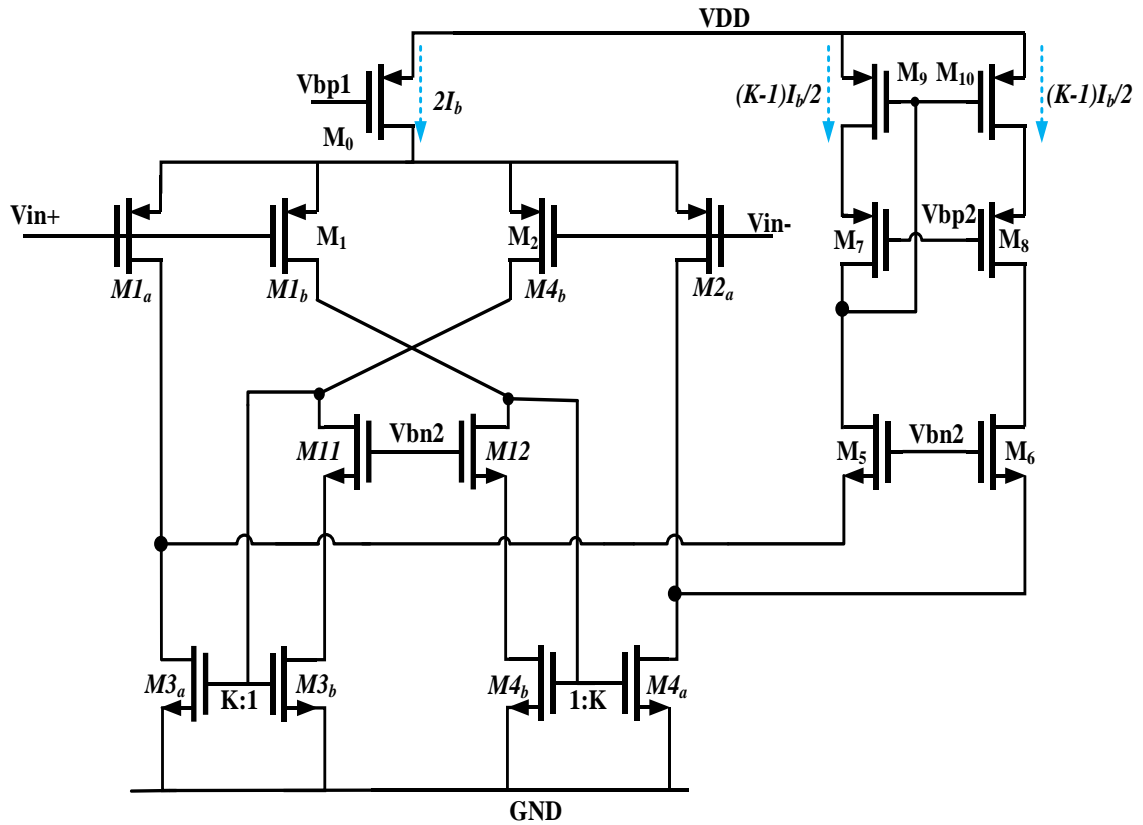


Fig: 5.3 Recycling Folded Cascode Amplifier

To address this inefficiency, a modified FC is presented in Fig. The proposed modifications are intended to use M3 and M4 as driving transistors. First, the input drivers, M1 and M2, are split in half to produce transistors M1a, M1b, M2a and M2b, which now conduct fixed and equal currents of $I_b/2$ (Fig.). Next, M3 and M4 are split to form the current mirrors, M3a:M3b and M4a:M4b with a ratio of K:1. The cross-over connections of these current mirrors ensure the small signal currents added at the sources of M5 and M6 are in phase. Finally, M11 and M12 are sized similar to M5 and M6, and their addition helps maintain the drain potentials of M3a:M3b and M4a:M4b equal for improved matching.

- Trans-Conductance (Gm)

$$G_m = g_{m1a}(1 + K)$$

- Output Impedance

$$R_{out} = \frac{1}{g_{m11}}$$

- First Pole

$$\omega_{dominant} = \frac{-1}{((g_{m8}r_{08}r_{010}) || (g_{m6}r_{06}r_{04a}) * 2C)}$$

- 2nd Pole

$$\omega_{1-non-dominant} = \frac{-g_{m12}}{C_L}$$

- 3rd Pole

$$\omega_{2-non-dominant} = \frac{-g_{m3b}}{C_{gs3a} + C_{gs3b}}$$

- 1 Zero

$$\omega_{1-non-dominant\ Zero} = \frac{-g_{m3a}}{C_{gs3a} + C_{gs3b}}$$

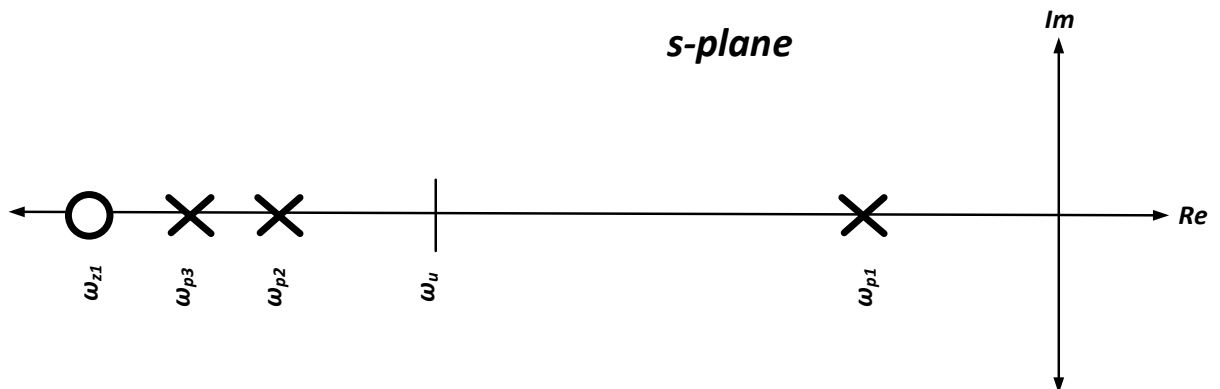


Fig: 5.4 Pole-Zero Location of Folded Cascode Amplifier

5.3 Two Stage Recycling Folded Cascode Amplifier

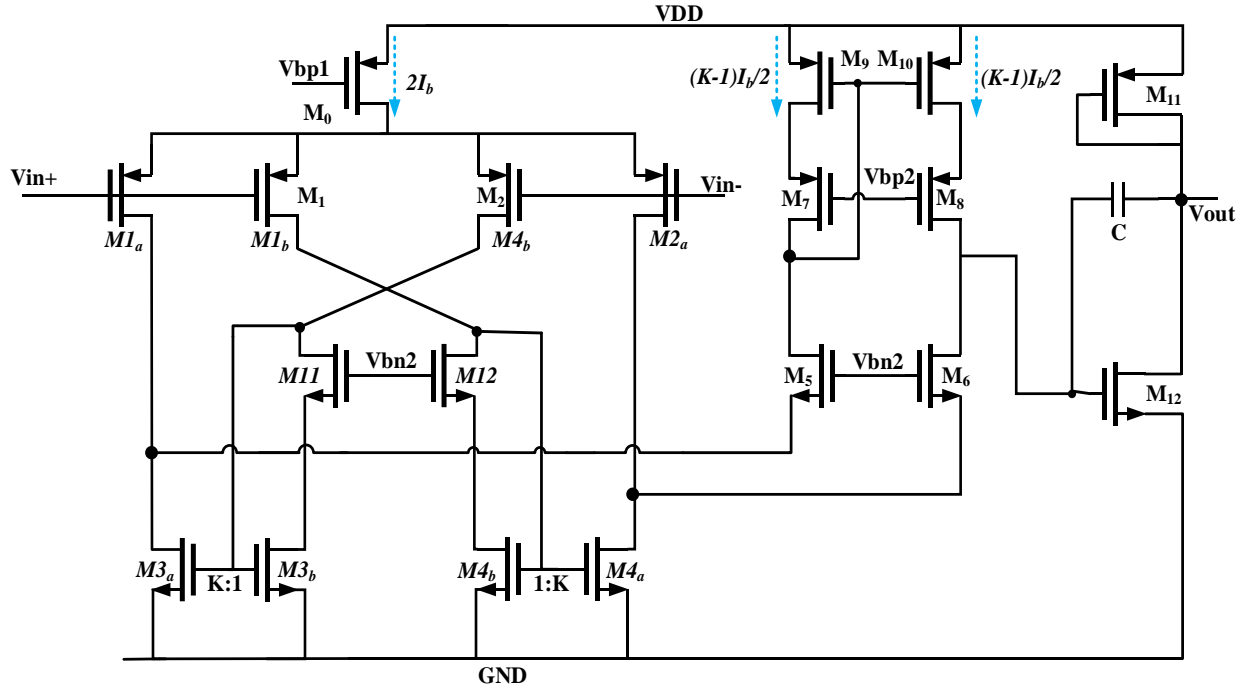


Fig: 5.5 Two Stage Recycling Folded Cascode Amplifier

- Trans-Conductance (Gm)

$$G_m = g_{m1a}(1 + K)$$

- Output Impedance

$$R_{out} = \frac{1}{g_{m11}}$$

- First Pole

$$\omega_{dominant} = \frac{-1}{((g_{m8}r_{08}r_{010}) || (g_{m6}r_{06}r_{04a}) * 2C)}$$

- 2nd Pole

$$\omega_{1-non-dominant} = \frac{-g_{m12}}{C_L}$$

- 3rd Pole

$$\omega_{2-non-dominant} = \frac{-g_{m3b}}{C_{gs3a} + C_{gs3b}}$$

- 1 Zero

$$\omega_{1-non-dominant\ Zero} = \frac{-g_{m3a}}{C_{gs3a} + C_{gs3b}}$$

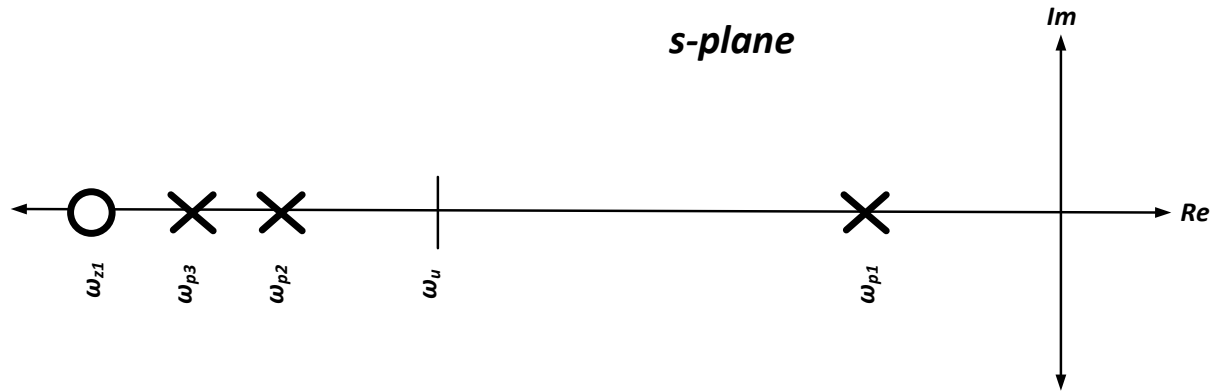


Fig: 5.6 Pole-Zero Location of Two Stage Recycling Folded Cascode Amplifier

5.4 OTA Design Requirements

The Low-pass Filter OTA is driving a low resistance i.e. 175K.

- For this we need to design a two stage amplifier as in low power it will load the first stage amplifier and operating points will be disturbed.
- Specs of the OTA derived from Notch characteristics.

5.4.1. OTA Design Parameter :

UGB, Maximum Load Cap, Gain and Phase Gain

Table 2.1 OTA Parameter

OTA Parameters	Value
UGB	500Hz
Maximum Load Cap	10pF
Gain	>80dB
Phase Margin	>60

5.4.2 Power Consumption of First Stage OTA

The power consumption for an amplifier can be reduced by operating the input transistors with high trans-conductance efficiency. Trans-conductance efficiency is chosen to be around 26. Then current requirement is around 8nA.

5.4.3 2nd Stage OTA

The trans-conductance of the 2nd stage should be 10 times higher compared to the first stage trans-conductance to have compensation without resistance. Hence $G_{m2} = 700\text{nS}$. The power required to get the amount of trans-conductance is 80nA.

5.5 Design Procedure of RFC

5.5.1 Design Of RFC

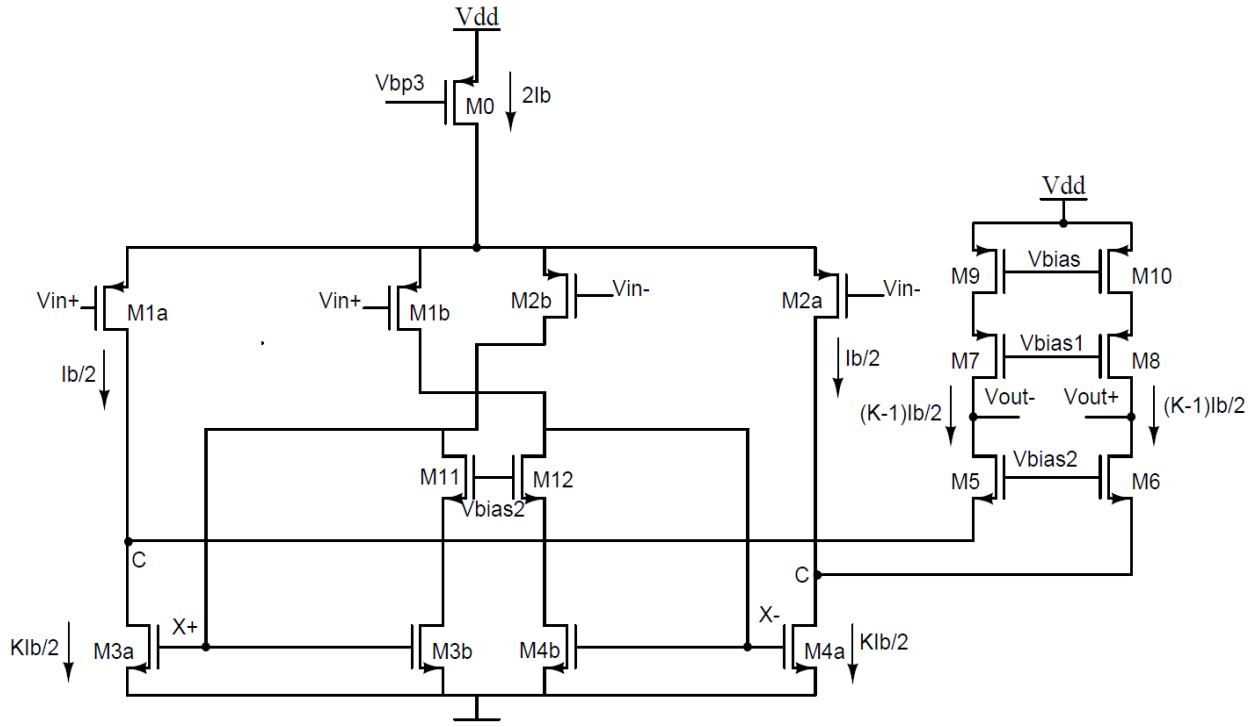


Fig. 5.7 Design of RFC in strong inversion region

For design of RFC using g_m/I_D methodology specifications are

- Unity gain bandwidth = 120MHz
- Load capacitance = 5.6pF
- Parameter $K = 3$
- Supply voltage = 1.2v

The UGB is taken as 120MHz. The relation between transconductance of the OTA and the UGB is given by

$$G_{mRFC} = \omega_t C_L \quad (5.1)$$

The transconductance of the input transistor is given as

$$G_{mRFC} = g_{m1a}(1 + k) \quad (5.2)$$

The g_{m1a} gives the transconductance of the input PMOS transistor named as M1a. The value of K is assumed to be 3. The input transconductance required for the UGB is found by substituting (5.2) in (5.1).

$$g_{m1a}(1 + k) = \omega_t C_L \quad (5.3)$$

$$g_{m1a} = \frac{\omega_t C_L}{(1 + k)} \quad (5.4)$$

By putting all the values in the above equation the transconductance of the input transistor required is 1.05mS. The DC current required for getting the transconductance is given by

$$I_{D1a} = \frac{g_{m1a}}{g_m/I_D} \quad (5.5)$$

The power consumption depends on the g_m/I_D . As we are operating in weak inversion the g_m/I_D is chosen to be very high so the power consumption is very low and the parasitic capacitance is very high. We assumed a g_m/I_D of 26. So the input DC current is found to be 8nA. The transconductance of M1a and M2a are assumed to be equal so the power consumed by them are also same. M1a and M2a comprises the half circuit so the power consumption by M1a, M2a, M3a and M4a is $4I_D$. So the current flowing through M0 is 32nA. As we have assumed K as 3 so the transconductance of M3a is 3 times that of the M3b. The transconductance of M3a is 240nS. By choosing same g_m/I_D for M1a and M3a the DC power is required is three times of input so the DC current is 24nA. By applying KCL at the cascode node the current flowing in M1a is 8nA and current flowing in M3a is 24nA so the current flowing through M5 and M7 is 16nA. As the path M2b, M11 and M3b acts as a unity gain amplifier so the transconductance of M3b should be

same as M2b which is same as that of M1a. By choosing the same region of operation the DC current through M3b is same as that of the M1a and is 8nA. As the current flowing through M5, M7 and M9 are same so the current consumed by them is also same 16nA. So the total current consumption of the OTA is

$$I_{RFC} = 8 * I_{bias} = 64nA \quad (5.6)$$

The design is carried out in TSMC180nm technology. The power supply voltage used is 1volts. So the power consumption is found to be

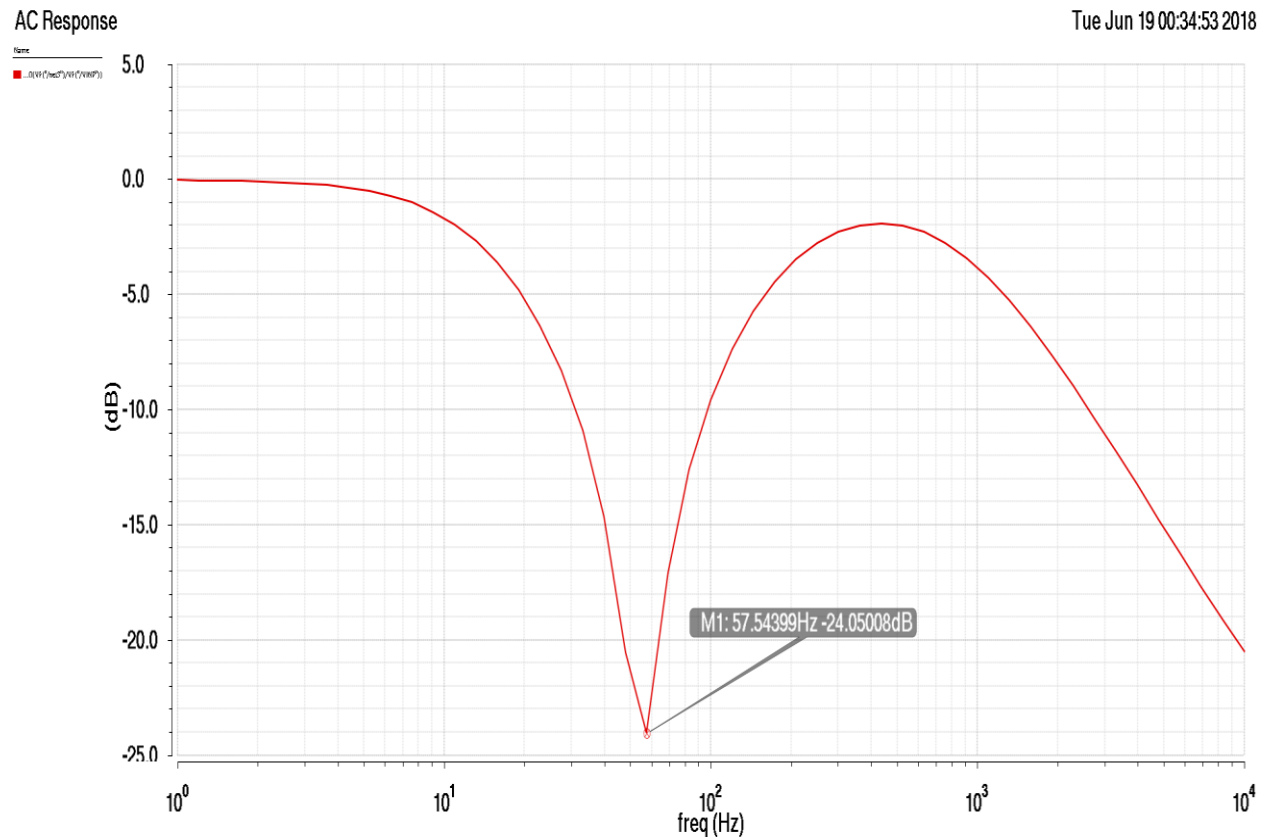
$$Power_{RFC} = 1 * I_{RFC} = 64nW \quad (5.7)$$

All the transistors in the RFC OTA are operated in weak inversion region of operation. The gain of the OTA decreases with the increase of channel inversion as the channel inversion increases the gate to source voltage increases which leads to increase in drain to source potential and the resistance becomes dependent on the drain to source potential which leads to decrease in the gain of the OTA. For reducing the effects of drain and source voltages on channel length, using minimum technology channel lengths are avoided.

Chapter 6

Simulation Results

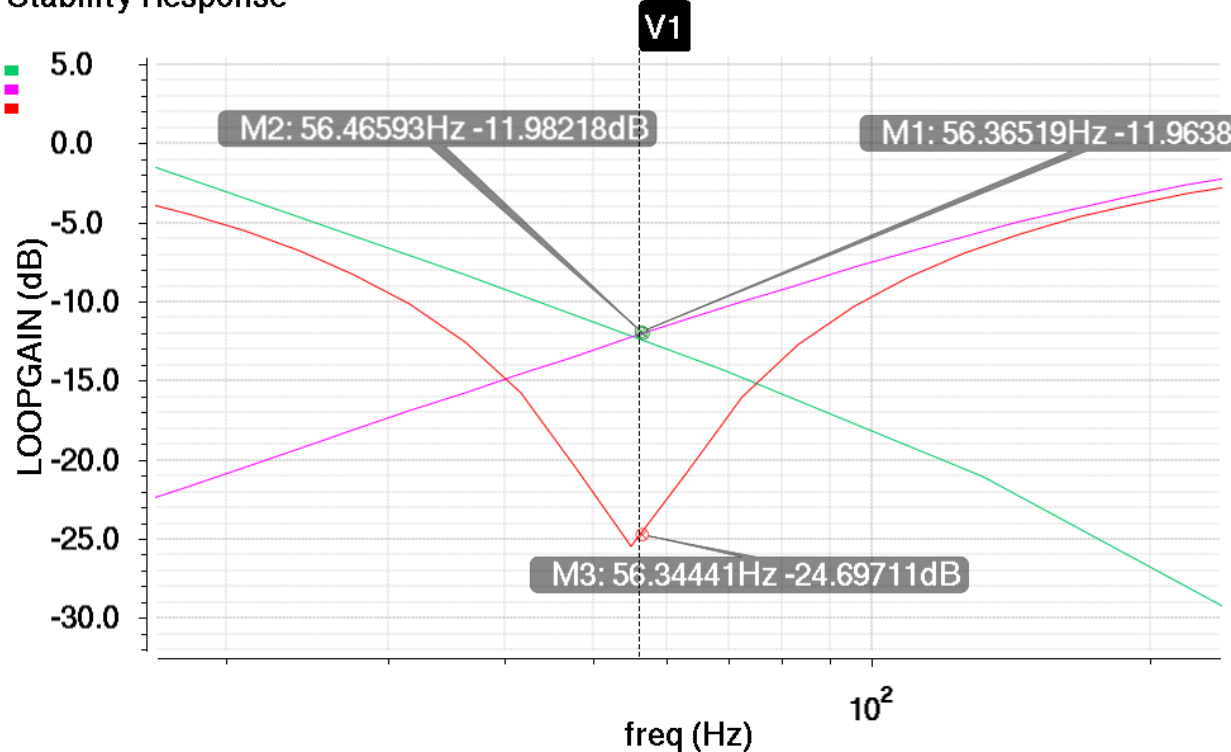
6.1 Notch Filter Result



- From this plot, we can easily observe Notch lies @ 57.5 Hz.
- It attenuates Line frequency i.e. 50-60 Hz by 25dB.
- It can also be observed that the Lower passband and Upper passband till the bandwidth requirement has a Gain of Zero dB.

6.2 Notch Filter with Low Pass loop gain and High Pass

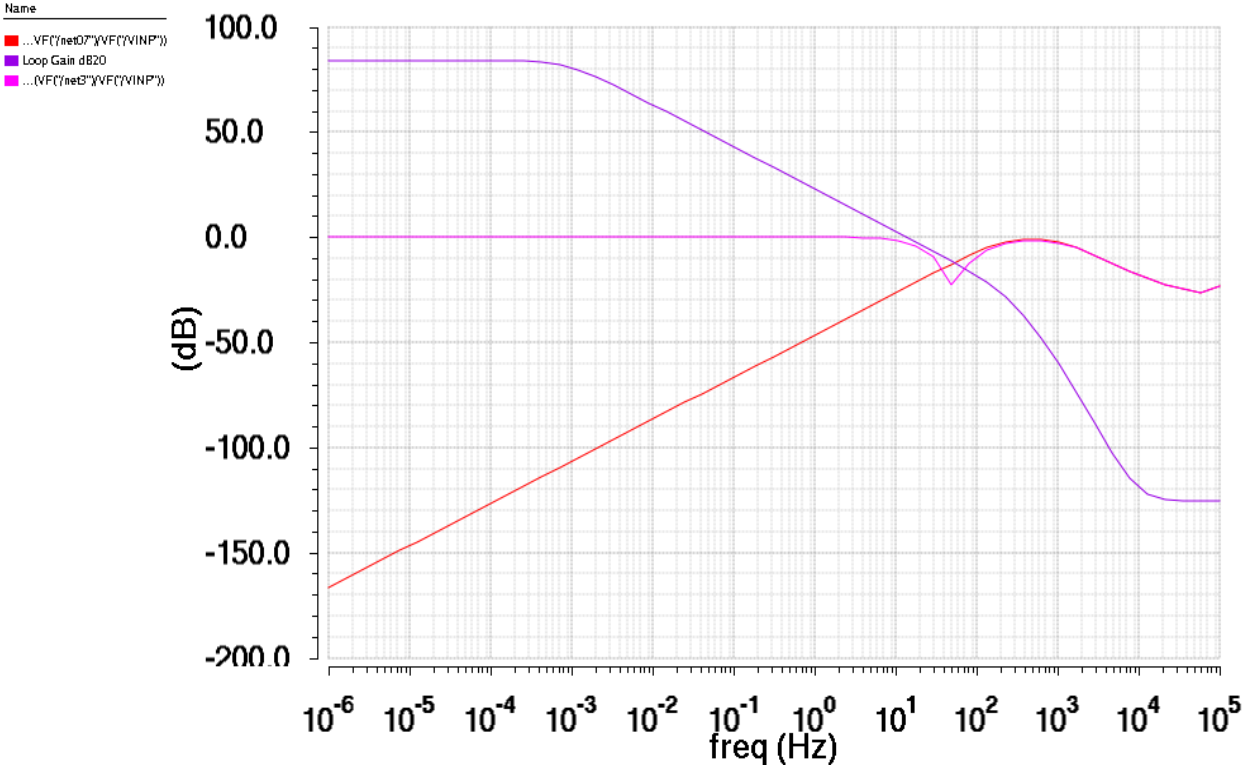
Stability Response



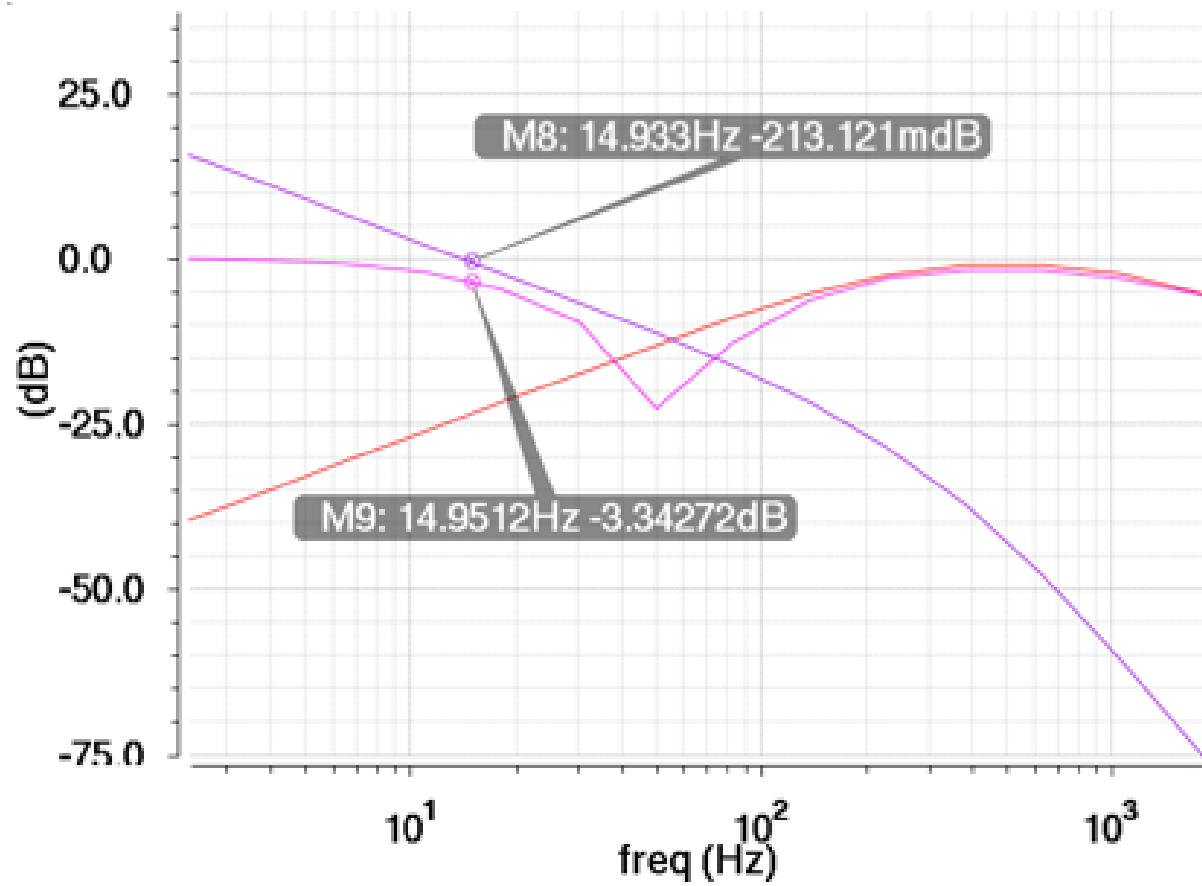
- It can be seen that at the cross over point of low pass Loop Gain and High Pass transfer function we are getting the notch.
- The attenuation in the notch is the addition of individual attenuations.

6.3 Loop Gain of Low pass and Forward path of High pass

$$\text{dB}20\left(\frac{\text{VF}("/\text{net07}")}{\text{VF}("/\text{VINP}")}\right)$$

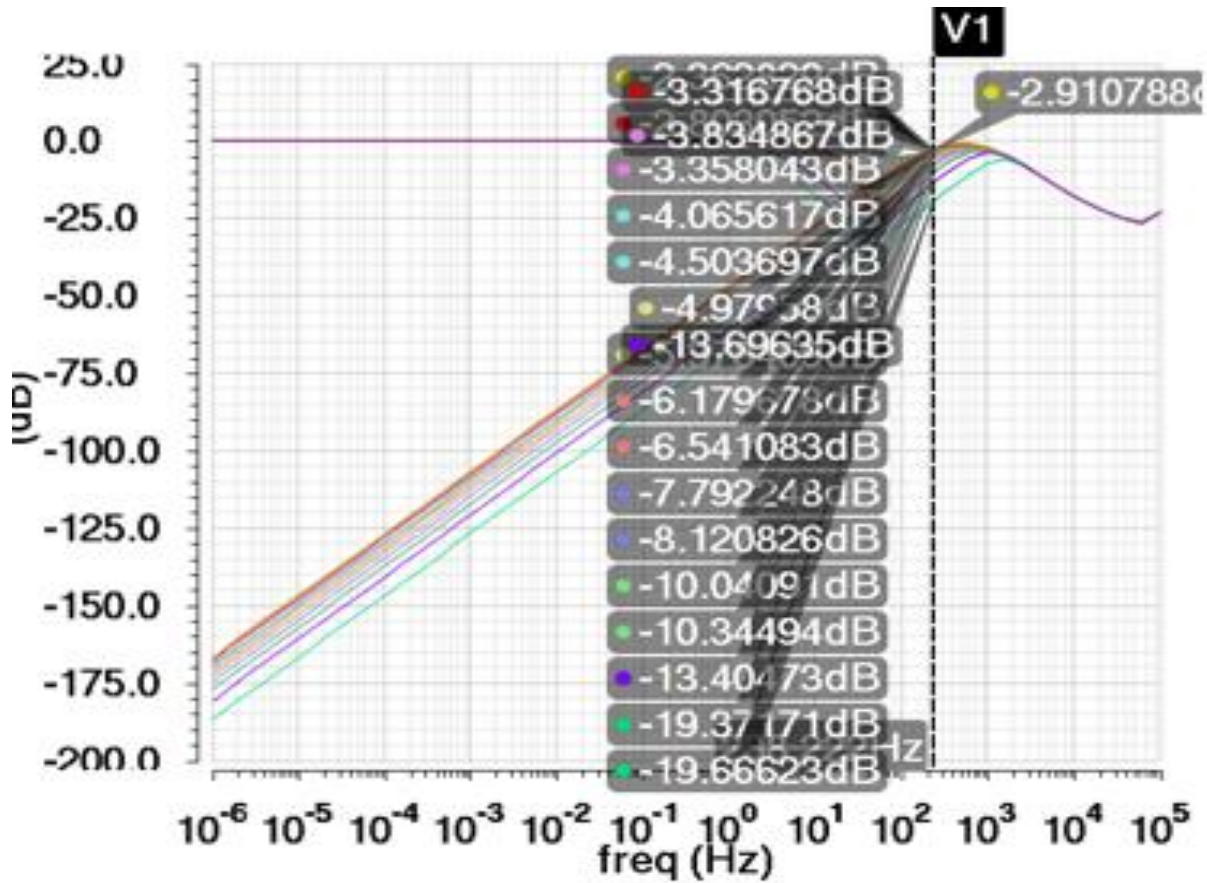


6.4 Relation between the Lower 3-dB point and forward path Loop Gain



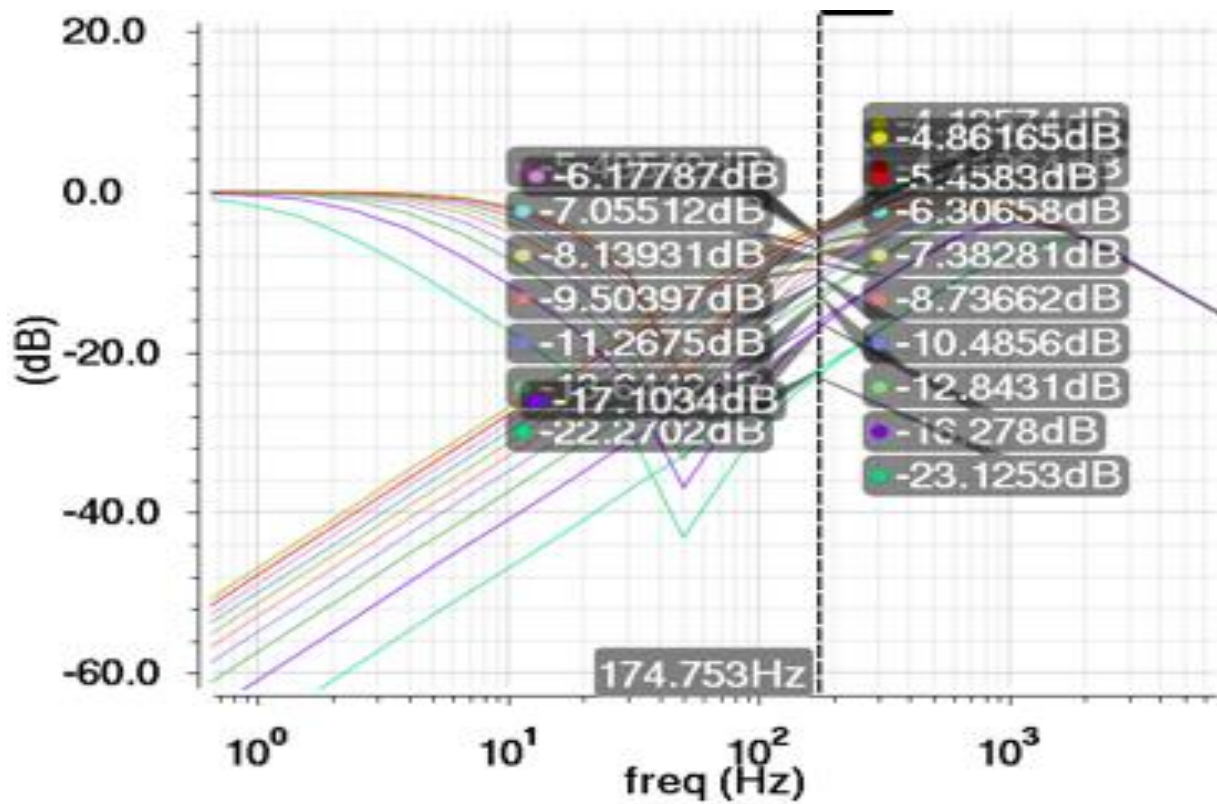
- Lower Cutoff frequency is equal to the UGB of the Low Pass Filter Global Loop Gain.

6.5 Relation between Closed loop Gain of the forward path and Notch depth with different q values



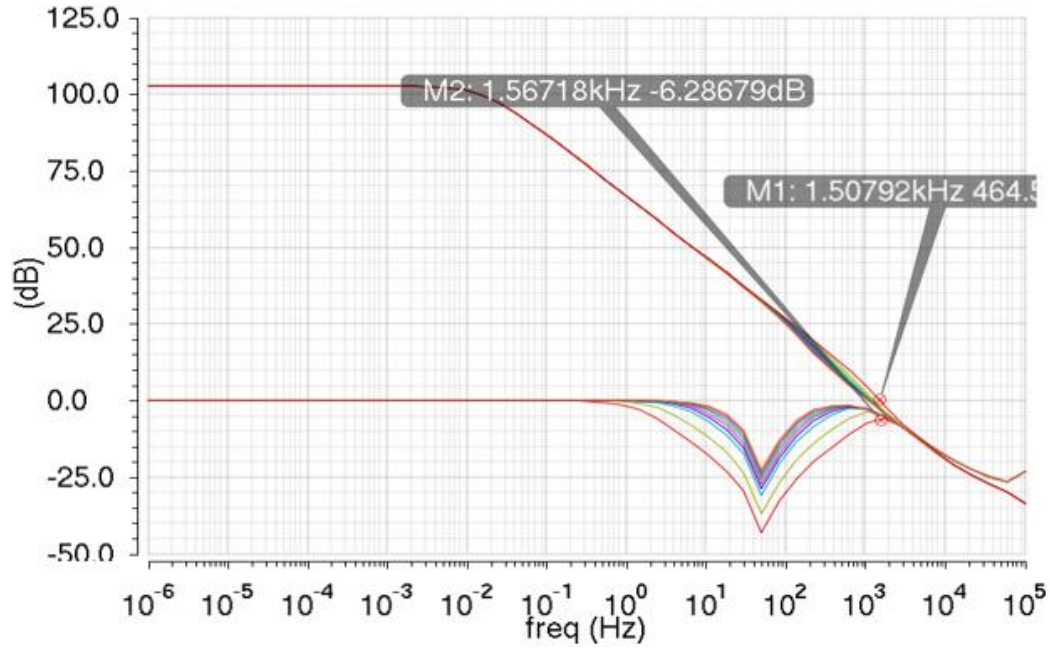
- The Closed loop gain increases with increasing feedback resistance.
- It exactly touches the notch depth at the cross over frequency.

6.6 Relation between Closed loop Gain of the forward path and Notch depth with different q values



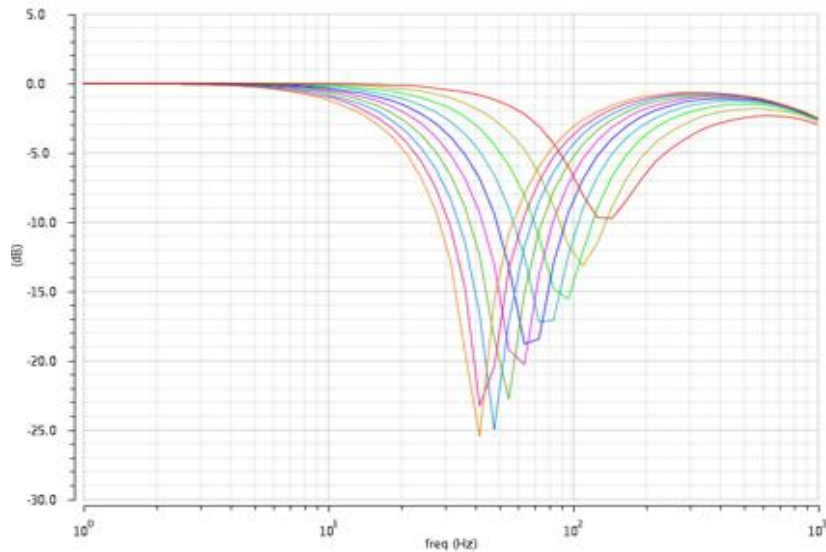
- q is increased by increasing the feedback resistance of the high pass filter.
- As q increases the notch depth increases but at the same time the lower bandwidth decreases.
- One more thing can be verified is that the -3dB of upper notch frequency is exactly at - $1/(2*\pi*qR3C)$

6.7 Relation between loop gain UGB of the forward path and falling out of band for multiple q values



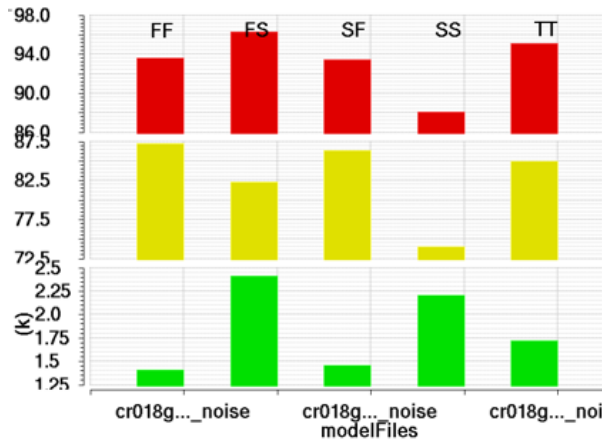
- The Notch gain decreases as the loop gain of the high pass path reaches unity.
- It exactly follows the behavior of forward path or high pass path.

6.8 Change in the lower cutoff frequency with change in the Low pass input Resistance

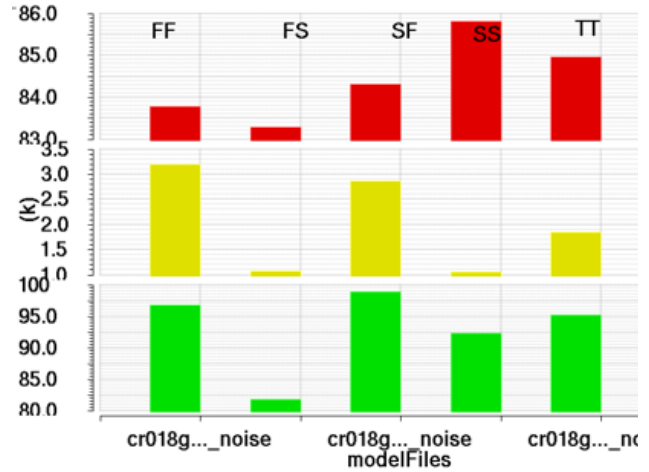


6.9 Gain, Phase Margin and UGB variation across 5 corners with replica bias generation

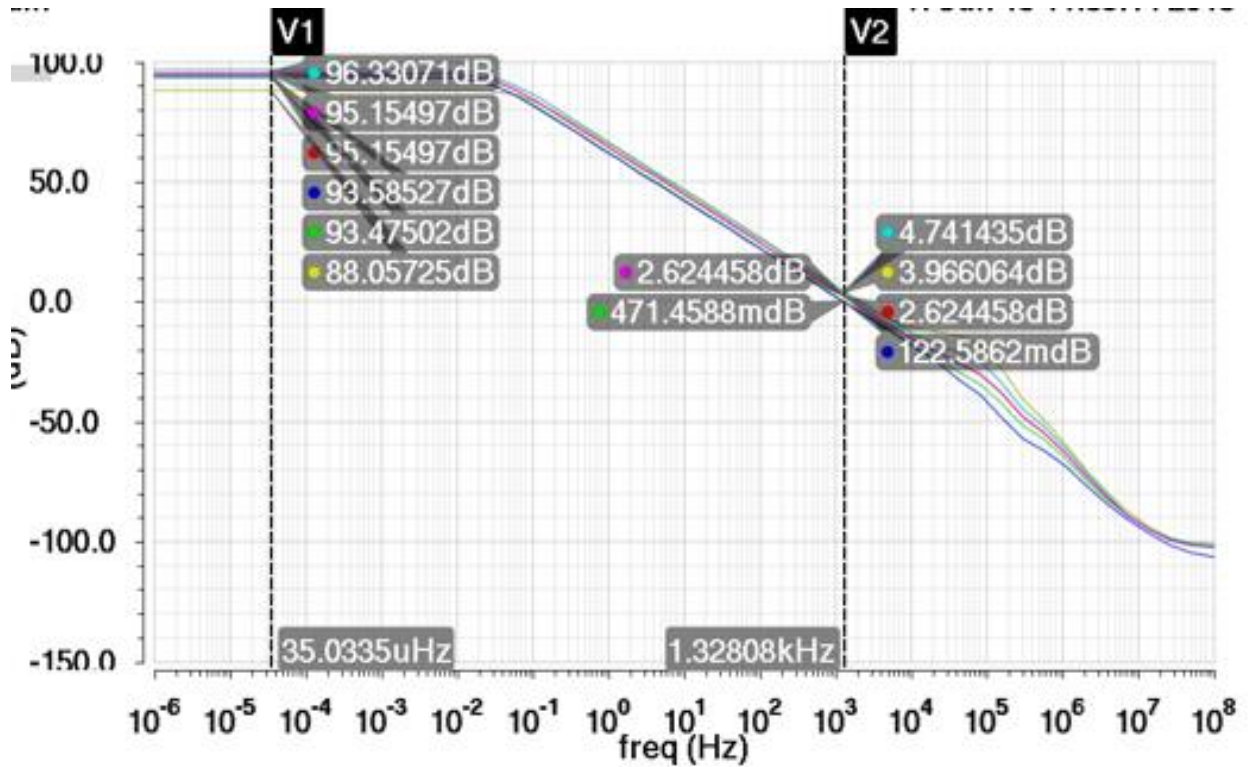
with replica bias generation



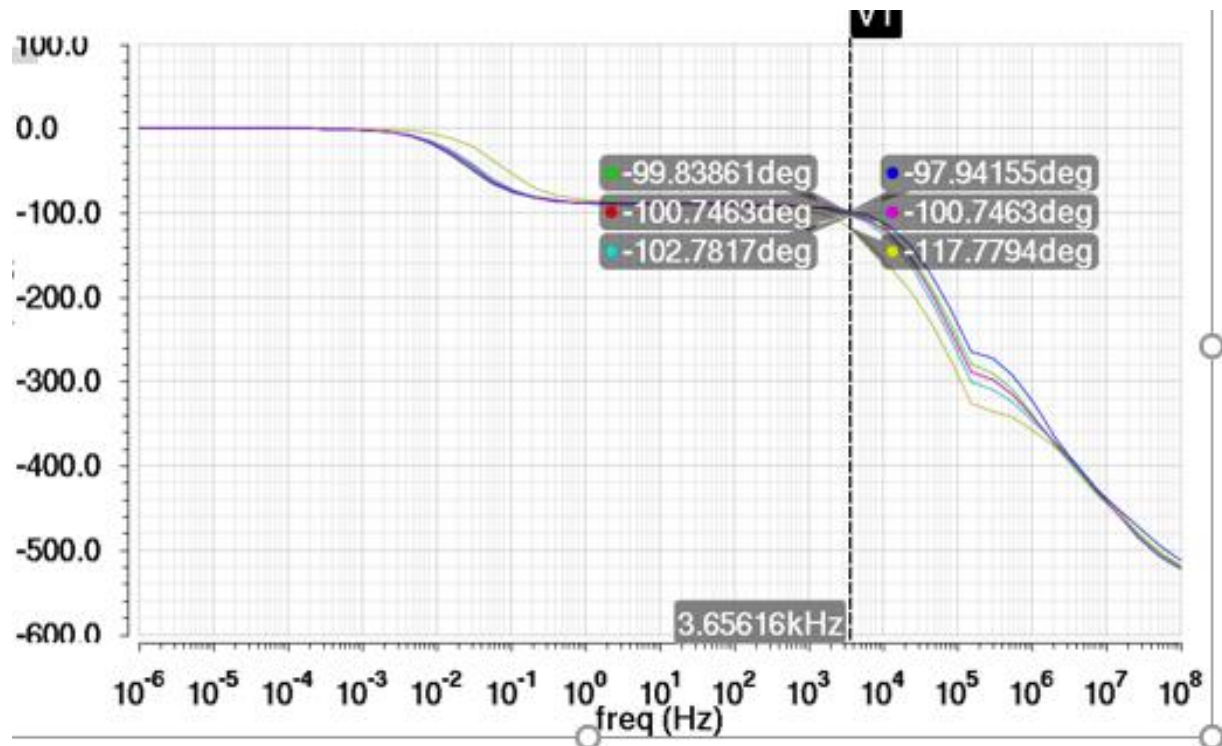
without replica bias generation



6.10 Gain and UGB Variation across 5 Corners

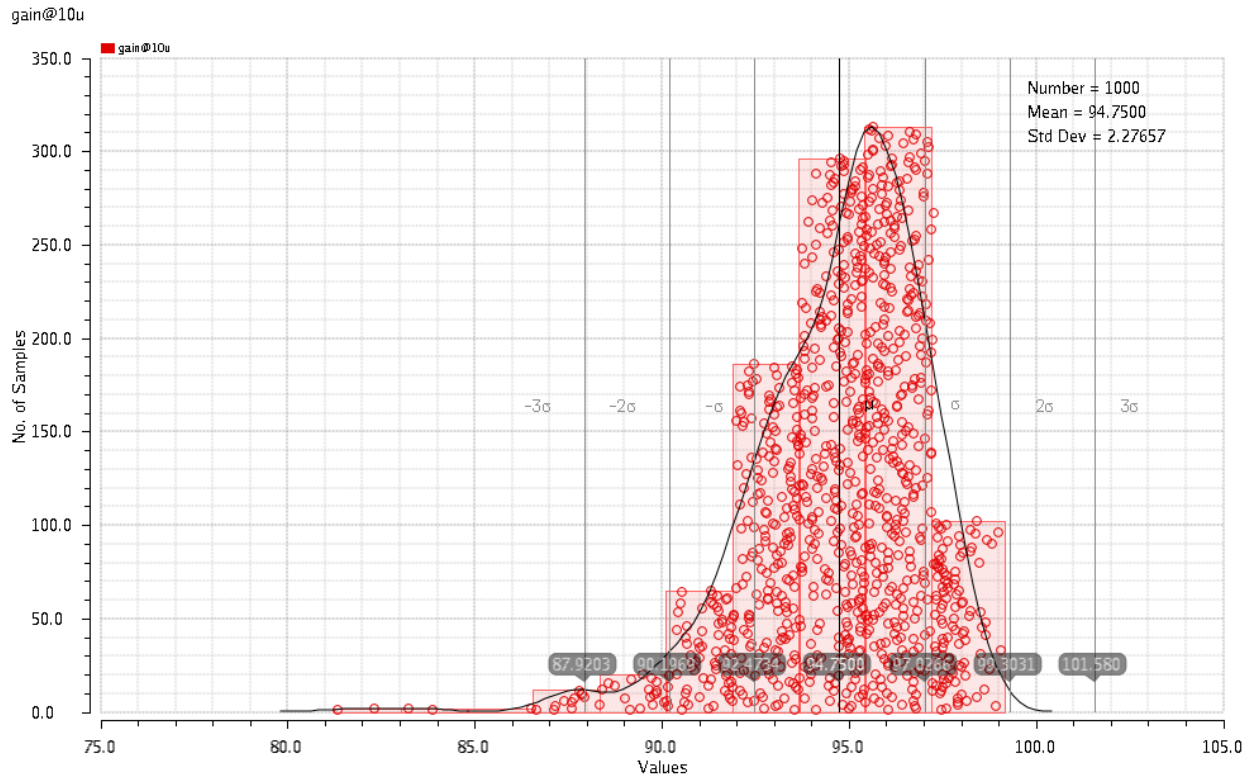


6.11 Phase Margin Variation with replica bias generation across 5 Corners

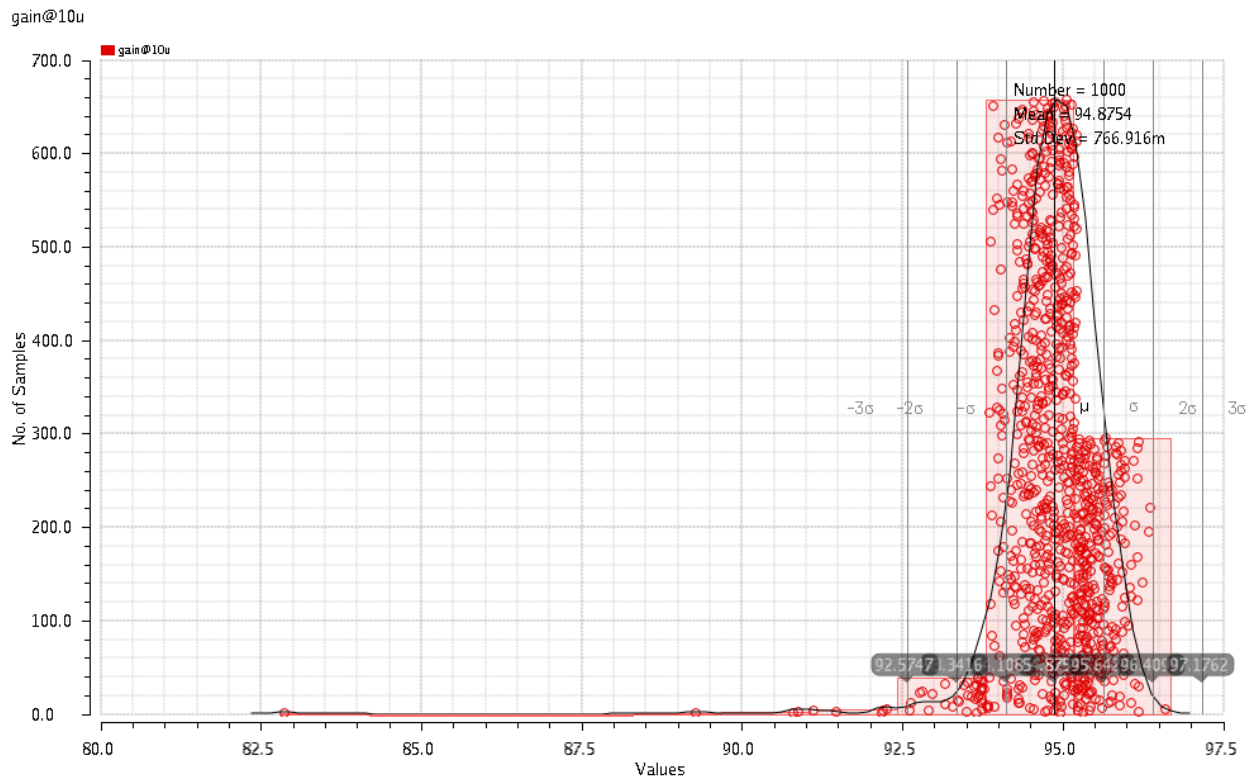


- Phase Margin is (180-angle value) shown in the figure.
- The values shown are the phase values at different frequencies.

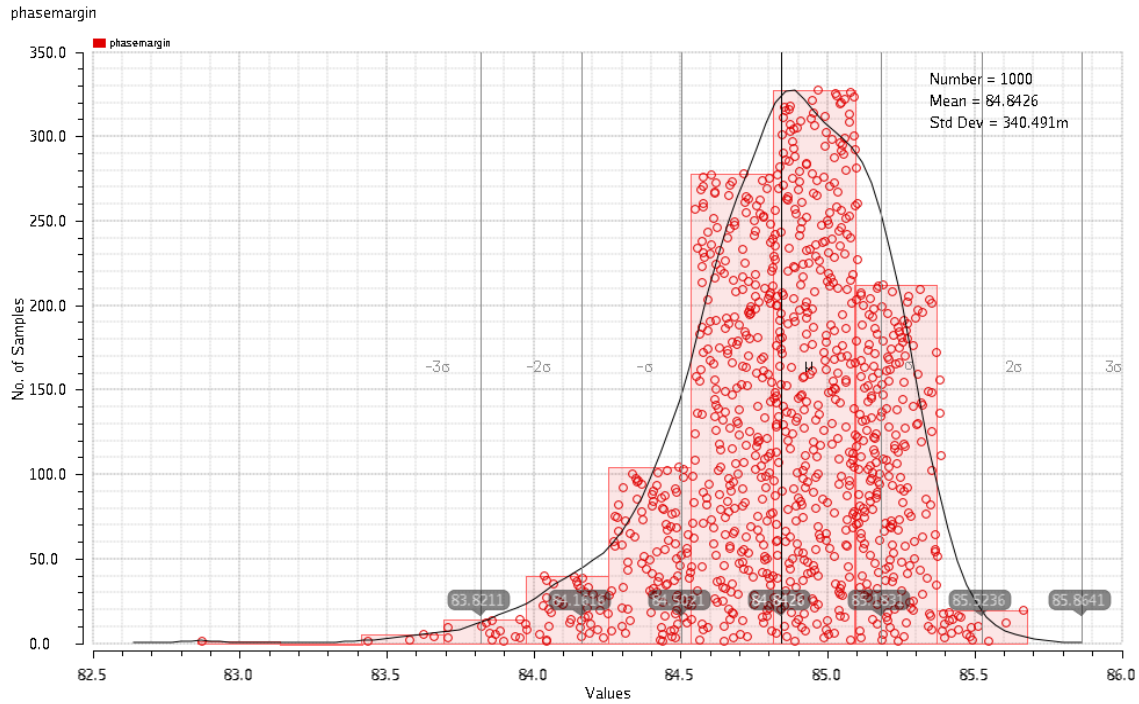
6.12 DC Gain variation of OTA without Replica Bias Generation



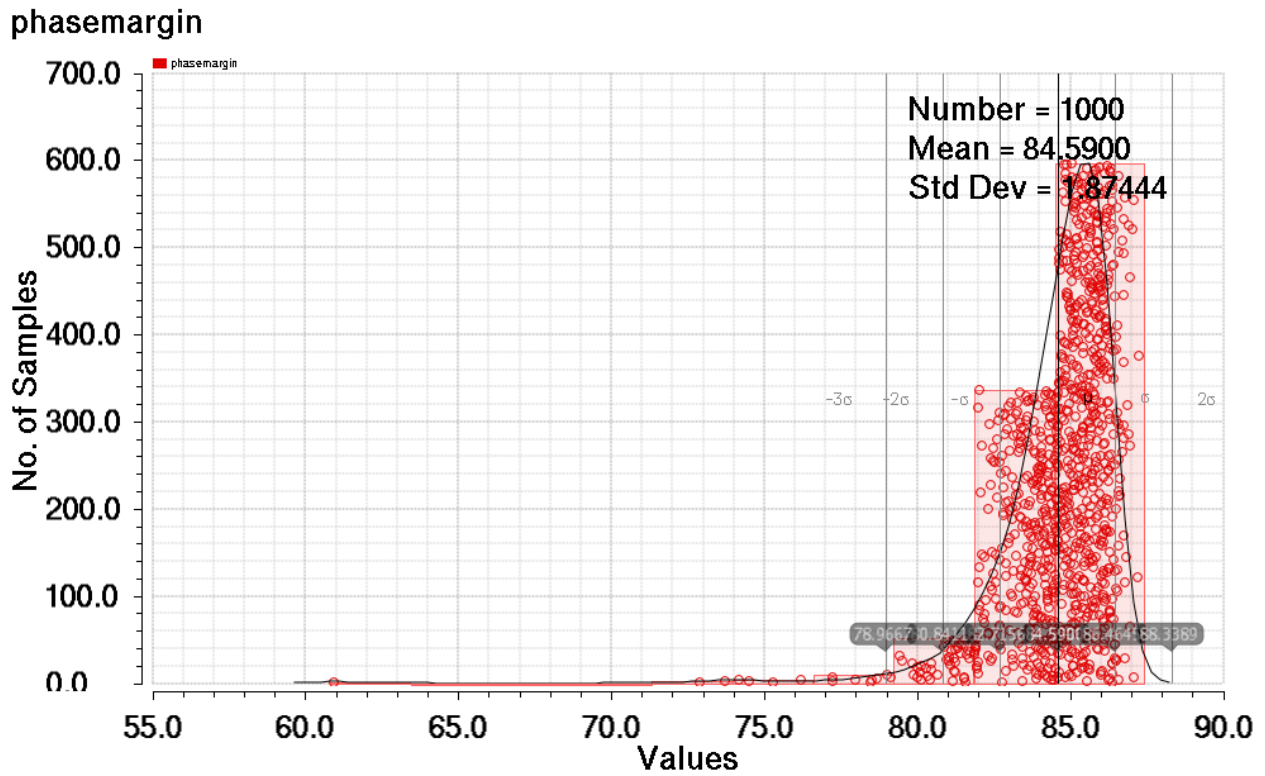
6.13 DC Gain variation with Replica Bias



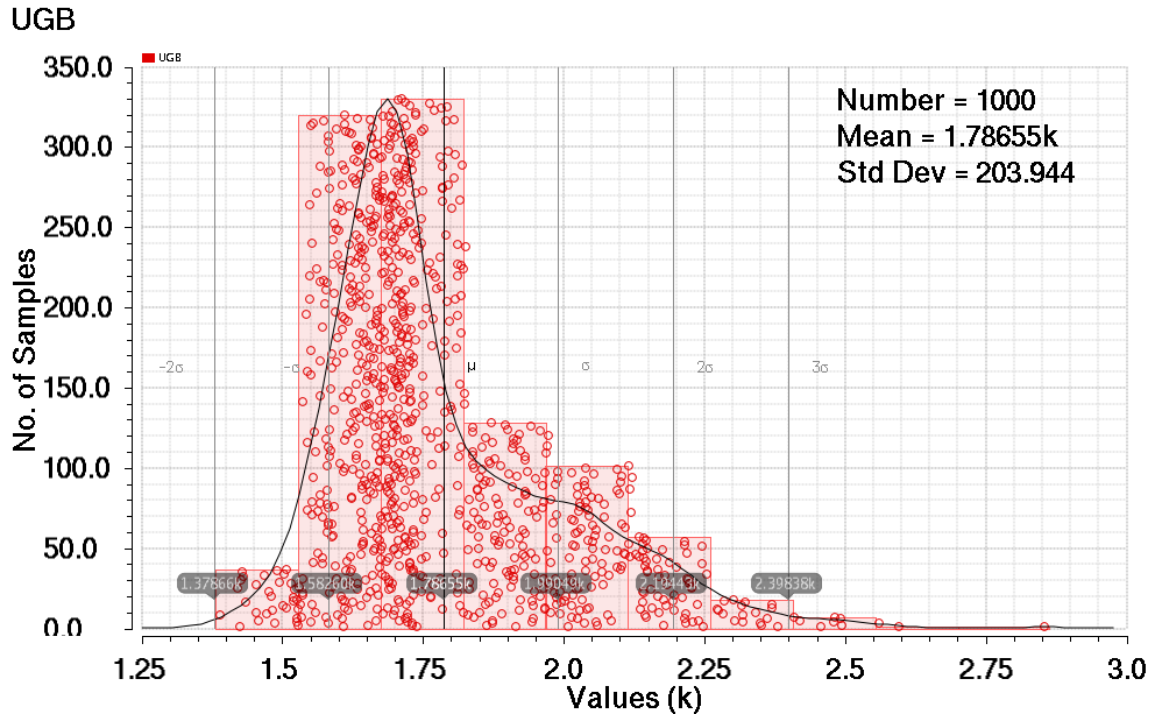
6.14 Phase Margin Variation Without Replica Bias



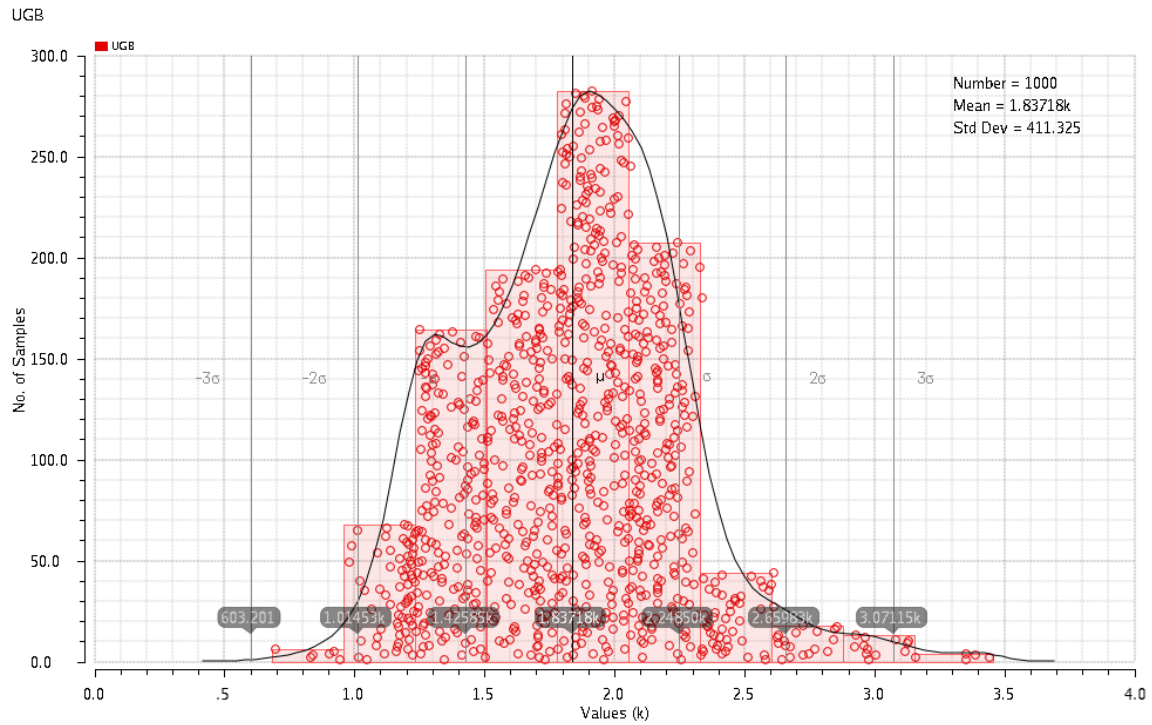
6.15 Phase Margin Variation with Replica Bias



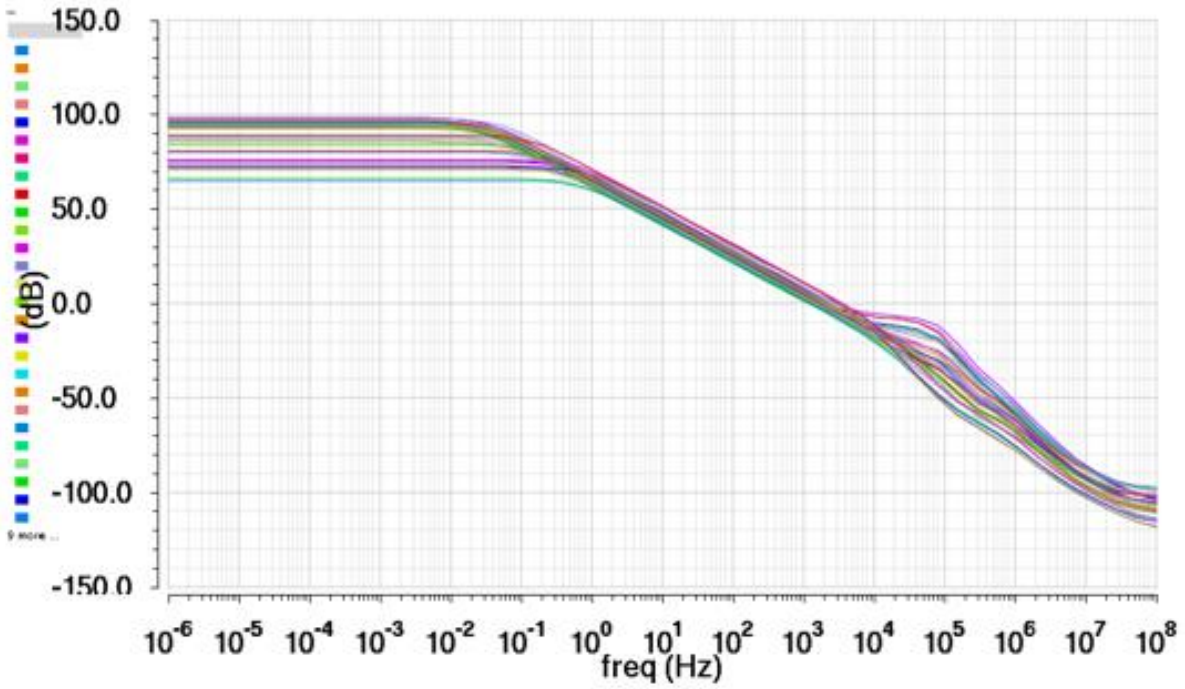
6.16 UGB Variation with Replica Bias



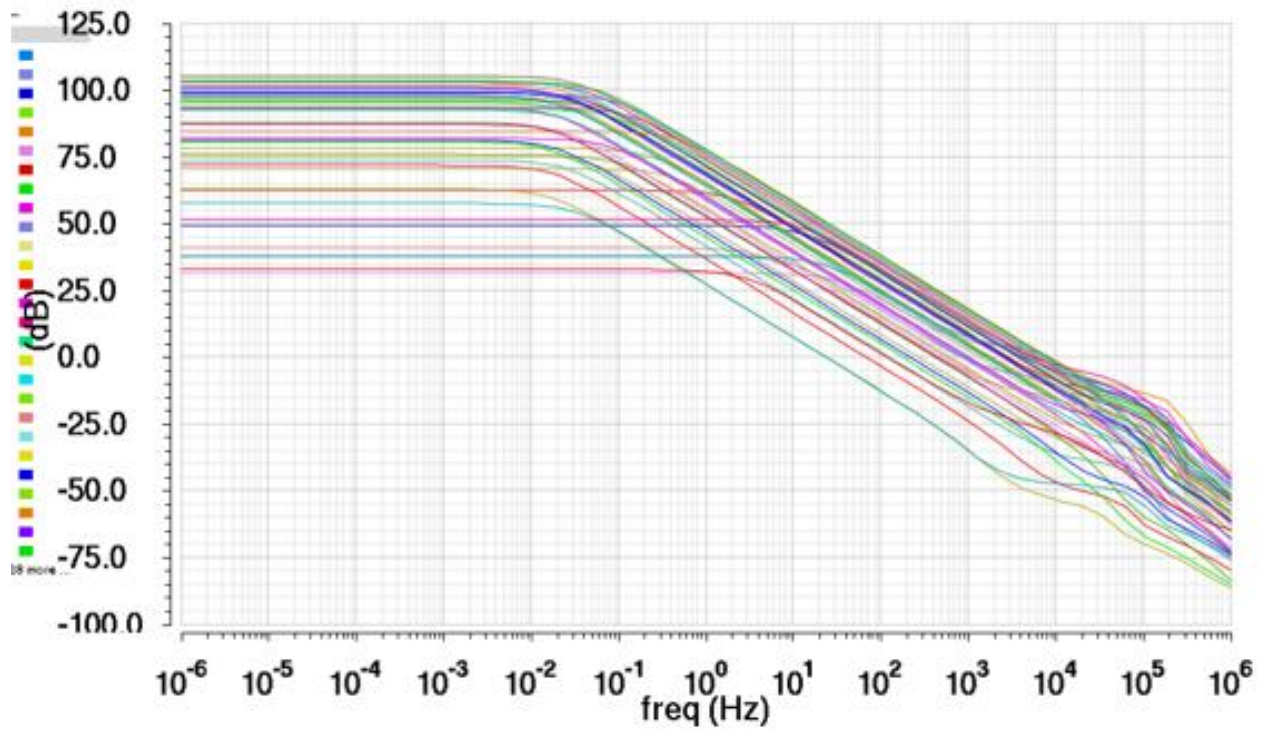
6.17 UGB Variation Without Replica Bias



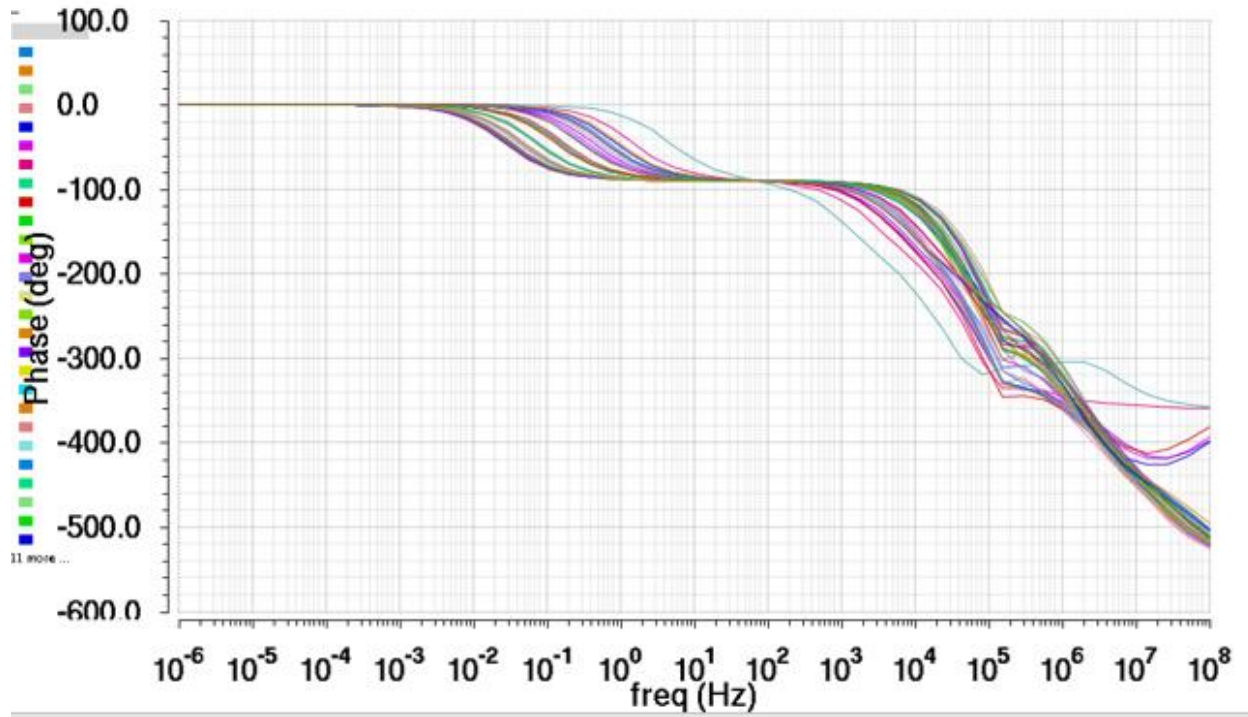
6.18 Gain Plot across 45 Corners with Replica Bias



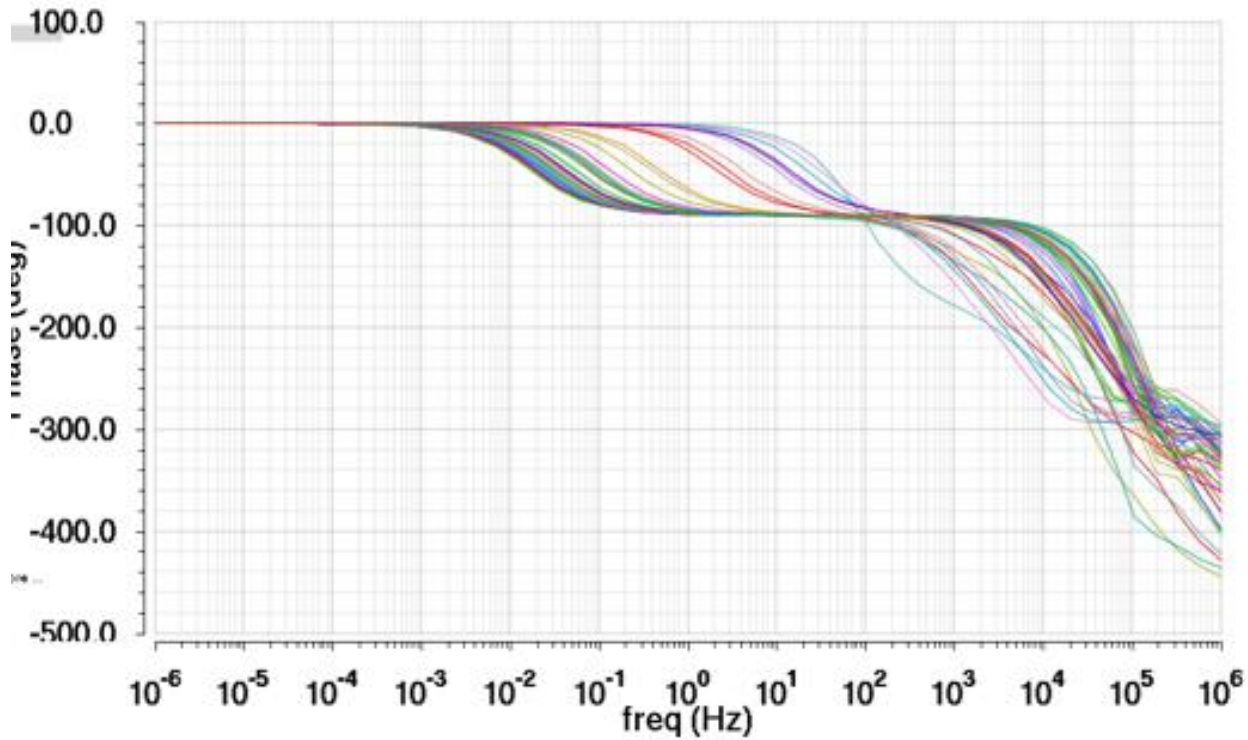
6.19 Gain Plot across 45 Corners without Replica Bias



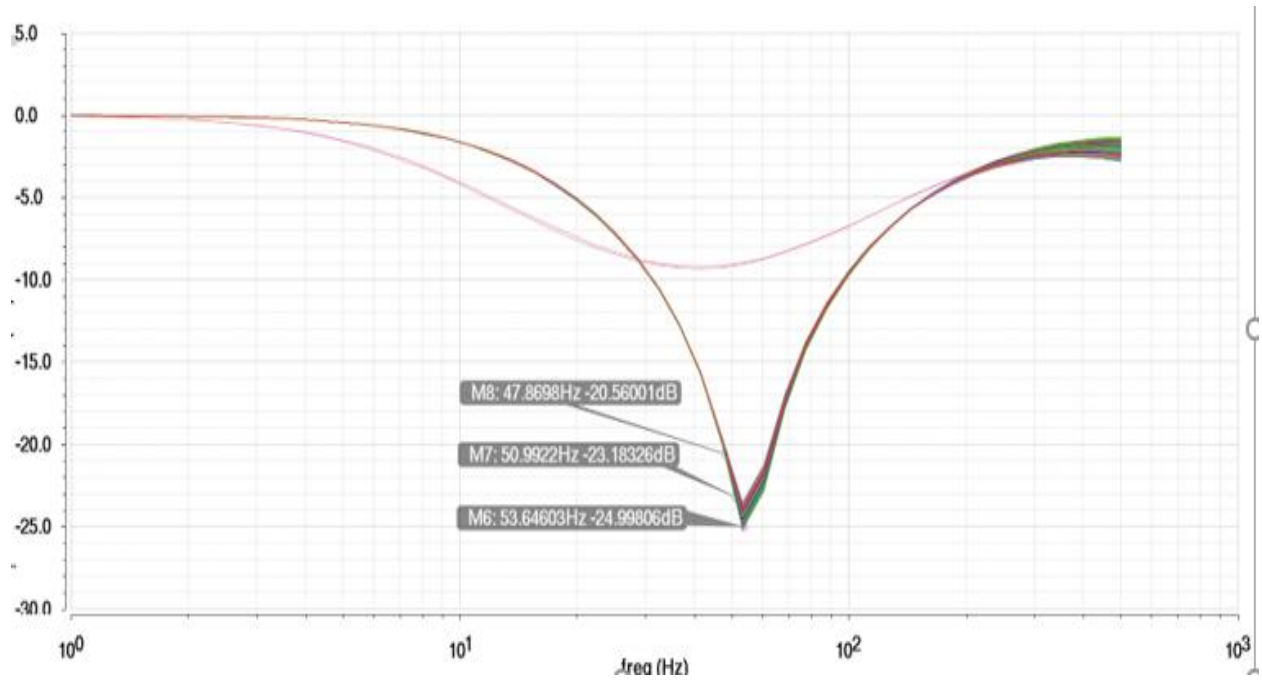
6.20 Phase Plot across 45 Corners with Replica Bias



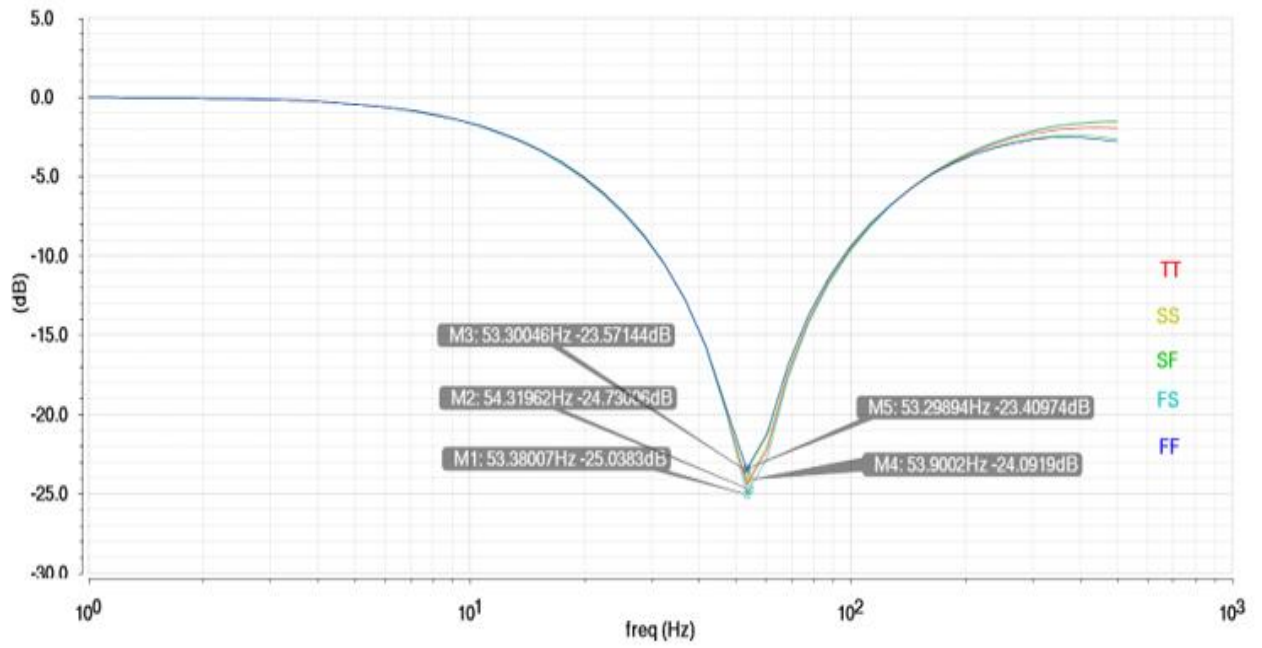
6.21 Phase Plot across 45 Corners without Replica Bias



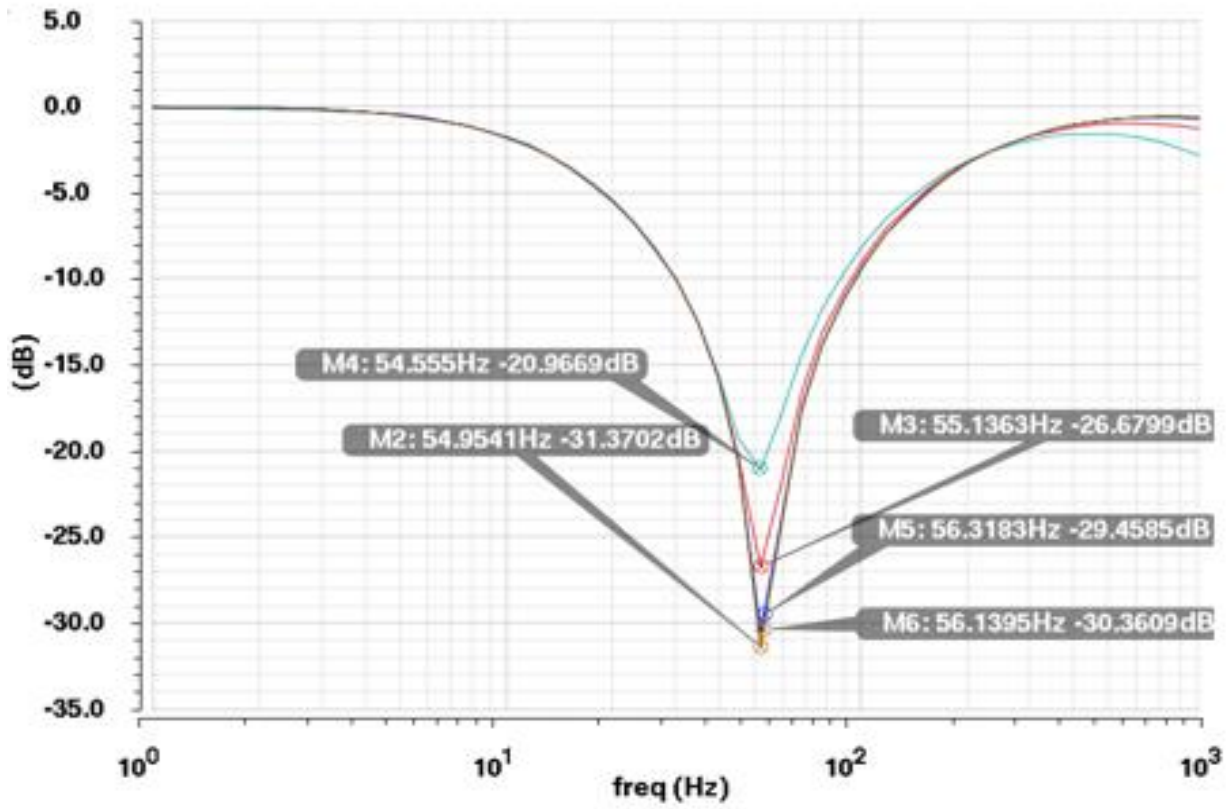
6.22 Notch Filter Gain Response in 1000 Mismatch runs



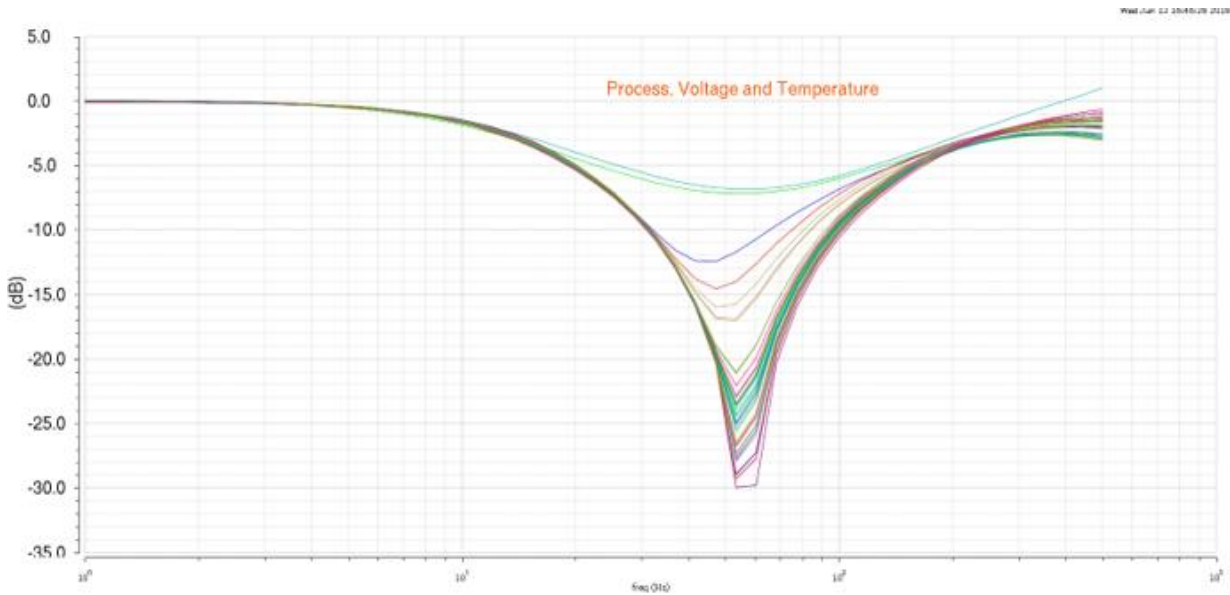
6.23 Notch Filter Gain Response across 5 corners with bias Generation



6.24 Notch Filter Gain Response across 5 corners without bias generation



6.25 Notch Filter Gain Response across 45 corners with bias generation



References

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