Design and Analysis of Charge Pump and Loop Filter for Wideband PLL

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Dedicated to

My parent

Abstract

The growing market for wireless applications demands low-cost low-power system-on-chip (SOC) transceiver systems. The frequency synthesizer, used as local oscillator, is one of the most critical building blocks in any integrated transceiver sys-tem. As the demand of low-power low-voltage cost-effective high frequency system increases, design is getting more and more challenging. Due to the high level of integration, digital CMOS process is most favorable for SOC design but it increases the design challenges for RF circuits. This research work is carried out on the design and implementation of low-power low-noise low-cost frequency synthesizer in 0.18μmepi-digital CMOS process. A new scheme has been used to linearize the VCO output frequency versus tuning voltage characteristic, which reduces the VCO gain. Jitter modeling in cadence has been discussed.

Nomenclature

PLL- Phase Locked Loop

LF-Loop Filter

CP-Charge Pump

VCO-voltage control oscillator

ANA-Analog

Fref -Frequency Reference

Fvco -Frequency of th VCo

Fdiv -Frequency of the divider

Contents

Chapter 1

Introduction

1.1 Introduction:

PLL is a fundamental building block for Wireless communication, High-Speed serial-link and radio technology. It is required to generate wide range of frequency in order to up convert the data for transmission and down convert the receiving signal for processing in a wireless trans receiver. For these essence designing a wide band PLL requires special attention.

PLL is a negative feedback system which can generate high frequency signal with low jitter that is comparable to reference frequency.

1.2 Motivation:

PLL can be a 2^{nd} or 3^{rd} order close loop system depending upon the loop filter order .The loop stability is governed by VCO gain, CP current, Divider and Loop filter values. So, it is obvious for wideband PLL that can prone to instability because of loop parameter variations. Like VCO gain varies when one band is switched to another band (coarse control).On the other hand fine control also makes Kvco (VCO gain) more nonlinear. So, sophisticated VCO design is essential.

A low noise PLL to cover a wide bandwidth is very difficult to achieve. Noise in a PLL broadly classified in two category as phase noise (Random Jitter) and periodic noise (Deterministic Jitter).The source of phase noise are generally thermal noise, flicker noise and shot noise. Periodic noise is generated by switching events in PLL and aggravated by circuit non-idealities. Cause of reference spur is same as periodic noise .Noise spike at multiple frequency from frequency offset from carrier, is called reference spur.

VCO is the main noise contributor in a PLL. In a wide band PLL , VCO has to produce wide range of frequencies to meet the requirement bandwidth. So VCO gain will be higher for wideband PLL to cover the wide tuning range. So, VCO is more sensitive to any external or internal noise. Now, any noise at the input will be amplified by VCO gain and jitter value will boost up. So, VCO design needs special attraction.

Phase noise and Jitter simulation is time consuming, as these value can be calculated only after PLL simulation is done. So, to get the accurate result we need to simulate for longer time. In other way a behavioral modelling can be implemented to reduce the simulation time as well as predict the accurate result for phase noise and jitter.

In these thesis a programmable charge pump has been designed to counter the stability issue. An ideal model has been implemented to recheck the non-idealities effect on the performance of a PLL. All the jitter analysis and phase noise analysis is done through S-domain modelling. To reduce the jitter and Kvco variation, new design has been proposed.

1.3 Thesis Outline:

Chapter 2: reviews the frequency synthesizer basics like stability, order and type. Different blocks of frequency synthesizer have also been discussed.

Chapter 3: different kinds of CP architecture and there application has been reviewed. Design issue of the wideband CP has been taken into account.

Chapter 4: Loop filter design steps have been discussed .PLL parameters have been decided according to jitter specification.

Chapter 5: Jitter model for calculating RJ and DJ in cadence has been proposed. Use of MATLAB have been avoided.

Chapter 6: PLL simulation result has been tabulated after doing the transient simulation ..Scope of future work has been discussed.

Chapter 2

Introduction to PLL

2.1 Introduction:

There are three types of PLL mainly available like analog PLL, Digital PLL and all digital PLL. All these PLL can be categorized in two different section mainly, like integer-N PLL and fractional PLL. In this work all the aspect of wideband integer PLL has been taken into account and designed according to industry standard. All the building blocks of a CP-PLL have been discussed in subsequent paragraph.

2.2 Basic PLL Building Blocks:

Crystal is a good source of low jitter frequency. Maximum frequency from a crystal is around 200MHz.So, there are some problems associated with the crystal oscillator. First, frequency available from crystal is limited within the MHz range. So, crystal is not used for high frequency application like RF trans receiver. Secondly, crystal can generate only particular frequency. So, for wideband application, crystal is not a choice of frequency generator. Multiple frequencies are required in RF transceivers for channel selection purposes. A current-controlled oscillator (CCO) or voltage-controlled oscillator (VCO) can be used as an alternative, and VCO is most commonly used.

The VCO uses a resonance circuit that generates an output signal at a frequency, f_{out}, according to its control voltage. The disadvantage of this system is the output frequency can change accordingly noise from the control voltage. Also, internal noise from the VCO contributes noise and can change the zero crossing points of the generated signal, resulting in jitter.

The advantage of a crystal oscillator's low noise and the frequency tenability of a VCO are combined in a PLL in order to provide a low noise carrier signal. A PLL is a negative feedback system, which compares the VCO output with a reference frequency provided by a crystal oscillator. The basic PLL functional blocks are shown fig 2.1

The VCO output phase, θ_{out}, is divided by N before comparing it with the reference phase provided by the crystal oscillator. A divider is required in the feedback loop to allow operation at much higher output frequencies compared to the frequency from the crystal oscillator. A phase detector (PD) compares the output phase to the reference phase and produce an error phase, θ_e. This phase error is converted to a voltage and is filtered before feeding it to the VCO. Therefore, the VCO control voltage is proportional to the phase error. The VCO control voltage then changes the output frequency. The process continues until θ_e approaches zero or some stable equilibrium value.

Stability is an issue in a PLL design as it is a feedback system. Therefore, PLL performance is not only depends on the noise level at the output but is also based on a few parameters such as locking time (also known as settling time or switching time), acquisition range (also known as capture or

pull-in range), and tracking range (or lock range). Locking time is the time required for the PLL to lock when channel switching occurs. Acquisition range is the maximum value of the phase error for which an unlocked PLL can eventually reach the lock state. In other words, a PLL will never lock if the phase error is more than the acquisition range. The tracking range is the maximum phase error offset for which a locked PLL will remain locked. Outside the tracking range, the PLL loses lock.

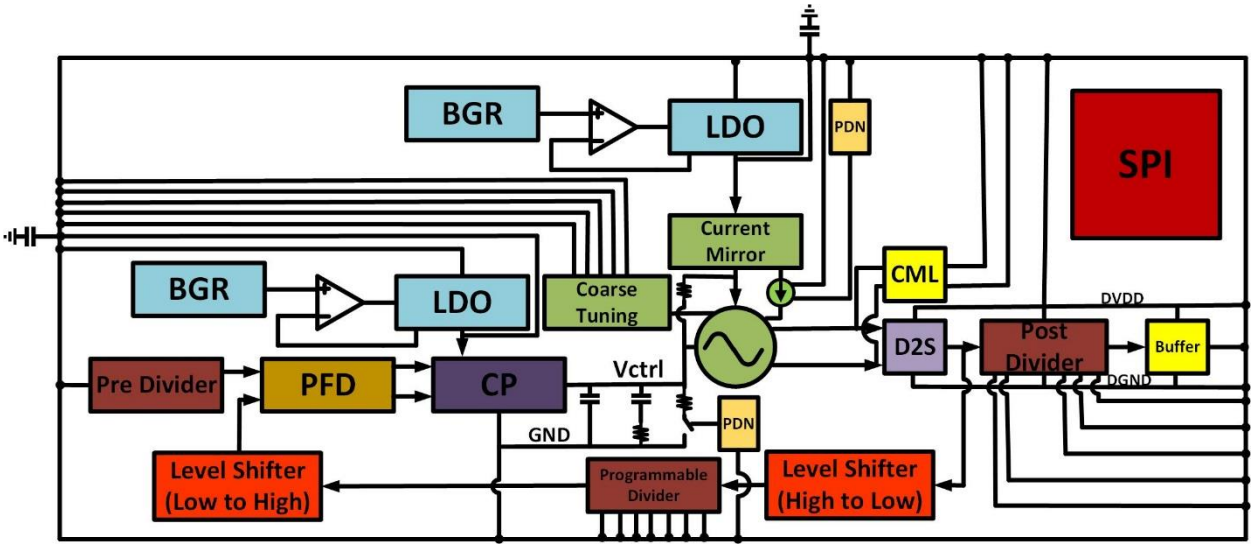


Fig 2.1 PLL_TOP _LEVEL

Next section provides a brief introduction to various feature of integer N-PLL as follows

- PFD based on NAND Gate
- Charge Pump
- Loop Filter
- LC-VCO
- Feedback divider (only integer mode.)

A. PFD based on NAND Gate:

The purpose of a PFD is to compare the reference clock signal and the VCO output clock after division in both phase and frequency. These frequencies are denoted by F_{REF} and F_{VCO} respectively. This circuit employs sequential logic to create three states and responds to the rising (or falling edges) of the Ref and CLK. If initially UP = DN =0,then rising transition Ref leads to

UP=1,DN=0.The circuit remains in this state until CK goes high, at which point UP returns to zero. The behavior is similar for CK input.

In Fig 2.2(a) the two inputs have equal frequencies but Ref leads CK. The output UP continues to produce pulses whose width is proportional to phase difference between two while DN remains at zero.

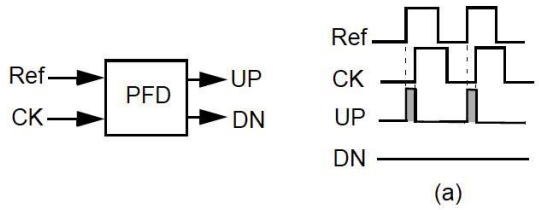


Fig 2.2

3-Stage NAND based PFD is a most obvious choice for wideband PLL .The Circuit Fig 2.2 can be used in various forms. In my thesis I have used NAND-based PFD, Fig 2.3.

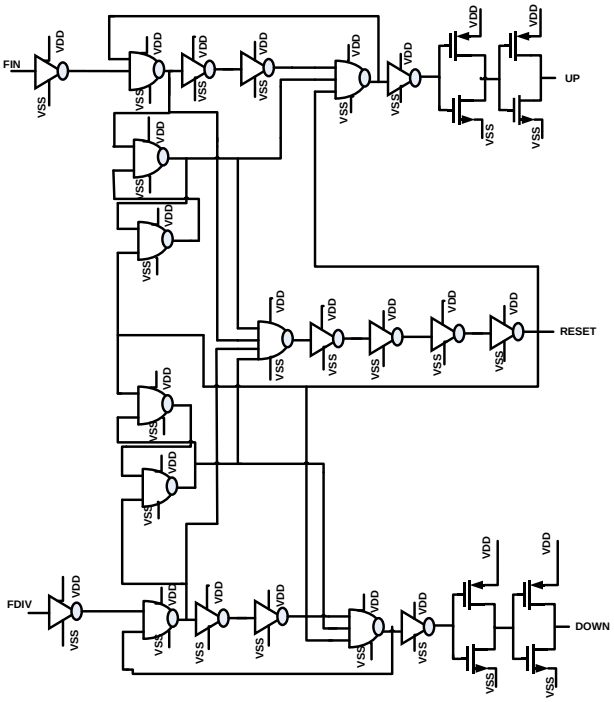


Fig 2.3. NAND-PFD

B. Charge Pump:

The charge pump is the device that translates the digital voltage signals generated from PFD into a current signal .A charge storage capacitor at the input of the vco makes the control voltage stable which is generated through CP charging and discharging action. Figure 2.4 shows the CP implementation used in the design of the PLL used in this thesis. CP works in three state as follows;

In UP state: the switch S1 is on and S2 is off; the load capacitor is charged by Iup and the Next, DOWN state: S1 is off and S2 is on, which causes capacitor to be discharged by Idn and voltage falls. For HOLD state: S1 and S2 are both off, then no current flows into output capacitor which means that the PLL is locked.

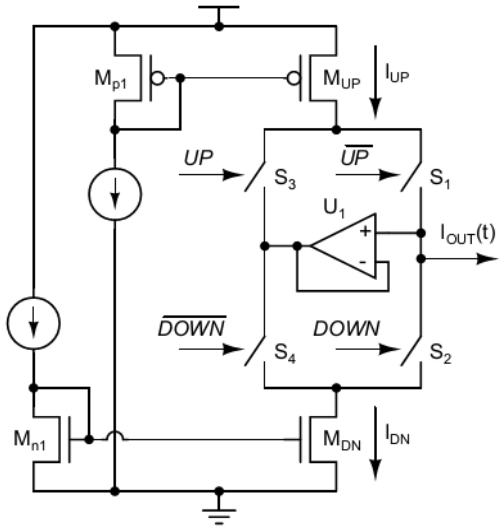


Figure 2.4 CP

C. Loop Filter:

PLLs act as low-pass filters so the purpose of the loop filter is to filter out the high-frequency components from the output of the PFD. Typically, loop-filters are just simple passive RC networks whose main objective is to filter out the high-frequency noise data from the PFD output. Choice of filter order solely depends on the specification like jitter and spur.

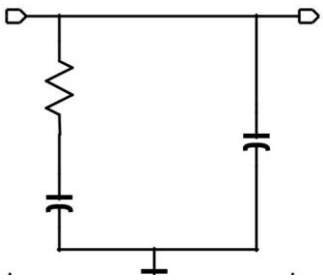


Fig 2.5 Loop Filter

I have chosen 2nd (Fig2.5) order filter to minimize the noise generated from filter register which can contribute to overall jitter. Output of this loop filter connected to the input of the VCO. Components of the loop filter values have been discussed in subsequent chapter.

D. VCO:

VCOs are the most important and complex component of the overall PLL design. The essential idea behind a VCO design is to generate a clock signal based on the Barkhausen criteria for oscillation which states that the magnitude of the VCO transfer function at the oscillation-frequency is 1 while the phase is -180 degrees. Two most popular VCO topologies whose sample architectures are ring-based and LC-tank based. Due to the superior noise performance we chose to design a LC-Tank based VCO. Ideally, its output frequency should be linearly related to the input control voltage. In my thesis I have chosen PMOS-NMOS cross couple (Fig-2.5) LC-VCO to reduce power consumption and get the better phase noise performance.

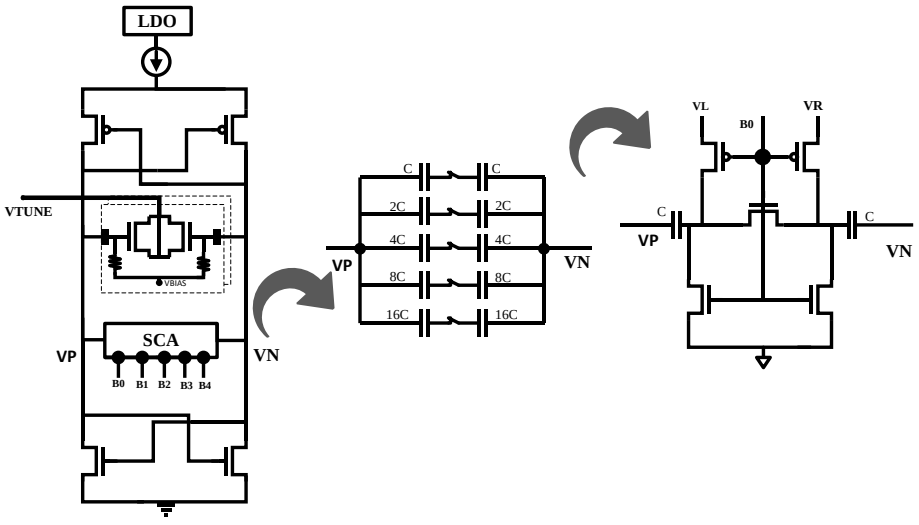


Fig 2.5 LC-VCO

E. Divider:

A frequency divider is needed to produce a clock signal that runs many times faster than the reference clock. The PFD input clock and reference clock have to be synchronized for PLL to be in locked condition. In order to perform this task we use an integer or fractional-N divider circuit, which divides the VCO clock by a factor to synchronize reference clock signal and the divider output clock.

2/3 Div cell has been used in this work (Fig 2.5). Level shifter has been added at the beginning and the end of the divider chain to reduce the dynamic power and improve the reliability.

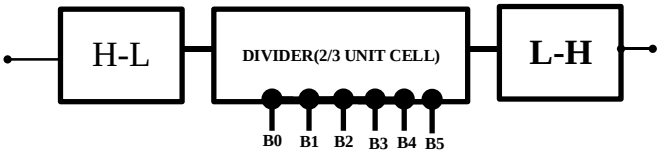


Fig 2.5 Divider

2.3 Performance summary of Different works:

Significant work has been carried out over the last few years in the field of frequency synthesizers for different applications. The reported works on integer-N frequency synthesizers are given in references [2], [3], [4], [5], [6], [7], [8], [9].

The frequency synthesizer [2] based on conventional integer-N PLL architecture in the frequency range from 2.4 to 2.5GHz is implemented in a standard 0.35μmCMOS process. The measured synthesizer phase noises are −104dBc/Hz and −116dBc/Hz at 550kHz and 2MHz offset frequencies. The reference spur is −53dBc and the synthesizer settling time is 140μs. But the VCO is designed with high gain (Kvco) to generate output frequency over the band of 2.4 to 2.5GHz and the loop filter is kept external due its large area requirement, hence does not provide SOC solution. The measured settling time is also high and the achieved phase noises are moderate

A 1V 2.4GHz fully monolithic PLL based integer-N frequency synthesizer [3] is fabricated in 0.2μmCMOS/SOI process. It includes fully differential dual-modulus prescaler and low-off-leakage-current charge pump for open-loop FSK modulation. In the design, Kvco is kept high around 500MHz/V and the used loop filter is off-chip due its required high capacitance. The output phase noise is moderate, −104dBc/Hzat 1MHz offset frequency. The power consumption of the PLL-IC core is 17mW at 1V supply voltage.

The Design of a 2.4GHz integer-N frequency synthesizer for application is discussed in reference [4].Introduction that relaxes the trade-off between the settling speed and the ripple on the VCO control voltage. Discrete time delay cell is used to introduce a zero in the open-loop transfer

function, hence obviating the need for resistor in loop filter to introduce zero. The Kvco value is kept quite high to cover 128 channels of 1MHz channel spacing. The capacitance multiplication technique is used to realize the required high capacitor value in loop filter, hence reduces the silicon area. The circuit is designed and fabricated in 0.25μm CMOS technology. The synthesizer achieves a phase noise of−112dBc/Hzat 1MHz offset. The frequency synthesizer settles in approximately 60μs with 1MHz channel spacing while exhibiting a reference spur of−58.7dBc.

A PLL-based frequency synthesizer with an on-chip passive discrete-time loop filter is reported in reference [5]. The closed loop is robust, stable. A fast switching speed is achieved by creating a stabilization zero in the discrete-time domain, rather than an RC time constant. It does not require a large capacitance and an accurate stabilization resistor. These factors make it attractive for on-chip implementation. The synthesizer has developed in a 0.25μmCMOS process for Bluetooth applications. It has a low settling time of less than 30μsfor 100MHz jump from 2.5GHz. Phase noise is−105dBc/Hz at 0.55MHz offset frequency and reference spur is −62dBc. But it has used off-chip VCO and off-chip programmable divider, hence it is not a SOC design.

A 2.4-GHz fully integrated frequency synthesizer for Bluetooth applications de-signed in 0.25μmCMOS technology is given in reference [6]. An improved current-match charge pump circuit without the start-up problem is used to reduce the spur level. A standard integer-N synthesizer architecture is used. The simulated phase noiseat1MHzoffset is−115dBc/Hz and designed Kvco is less than 120MHz/V. The frequency synthesizer can operate at 1V of power supply and consume 14mW which does not suit to low-power design. The locking time is moderate, less than 100μs for 80MHz output frequency change.

Reference [7] describes the implementation of 2.4GHz integer-N type frequency synthesizer in 0.18μm standard CMOS process for low-power wireless sensor applications. The standard integer-N topology is used for implementation. The measured power consumption is 8mW at 1.8V supply and settling time of 50μs. The achieved phase noises are−76.3dBc/Hz and −98.7dBc/Hz at 100kHz and 0.5MHz offset frequency, respectively. The phase noise and the settling time are moderate. Also the designed Kvco is kept 250MHz/V to cover the frequency range of 2.1 to 2.4GHz, which is quite high and used loop filter is off-chip for its large capacitor value. Hence, it is not suit to SOC solution.

A 2.4GHz integrated PLL-based integer-N frequency synthesizer in 0.3μm RF process is presented in reference [8]. Prescaler accompanied with phase-switching technique is used to eliminate the glitch when division ratio changes. The synthesizer has a frequency tuning range from 2.28 to 2.75GHz. The simulation results show that synthesizer dissipates less than 66mW from 3.3V

supply; settling time is less than 100μs and the phase noise is −117dBc/Hzat 600kHz offset. Power consumption is quite high but phase noise is very low, thus it suits more for low noise applications than low-power applications. The synthesizer has used MOS varactor with high Kvco of 400MHz/V. This needs large loop filter capacitors to filter out noise from VCO control voltage, increases the silicon area.

A digital to analog converter (DAC) with tunable gain is used along with a linearized varactor [10] for the direct VCO control path to minimize the gain mismatch between these two paths. The output frequency settling time must be zero for any frequency change if the gain of two paths is perfectly matched. However, in reality there are residual mismatches due to the varactor non-linearity and finite rise time of the DAC output voltage, which limits the settling time enhancement. The designed frequency synthesizer has very low power consumption of 3.48mW from 1V supply, low settling time of less than 10μsfor 80MHz frequency jump from 2.4GHz and moderate phase noise of−112dBc/Hzat 1MHz offset frequency. All results given are based on simulations and the circuit has designed in RF-CMOS process which is not favourable for SOC design. The performances mainly phase noise and power consumption of frequency synthesizer implemented in RF-CMOS process, are superior over the synthesizer realized in digital CMOS process. In addition, the inclusion of DAC increases the complexity. The performance of all the relevant works discussed so far is summarized in table 1.1.

In summary, the power consumption (simulated result) and the settling time of he synthesizer [9] is quite low but the frequency synthesizer is designed using RF-CMOS process which is not favored in digital circuit realization for SOC design. Frequency synthesizers reported in [2], [4], [5], [6] and [7] are realized in standard CMOS process. The power consumption of the Synthesizer in [7] is 8mW but the off-chip loop filter is used due to its large capacitance

	Process	**Type**	**Loop Filter**	**Phase Noise**	**Reference Spurs**	**Settling time**	**Power**
Ref[2]	0.35 um	Integer-N	Off-chip	-116dBc/Hz @2MHz offset	-53dBc	140uS	-at 2.7- 3.3V
Ref[3]	0.2 um	Integer-N	Off-chip	-104dBc/Hz @1MHz offset	-	<600uS	17mW at 1V

Ref[4]	0.25 um	Integer-N	On-chip	-112dBc/Hz @1MHz offset	-58.7dBc	60us(for 64MHz Jump)	20mW at 2.5V
Ref[5]	0.25 um	Integer-N	On-chip	-105dBc/Hz @0.55MHz offset	-62dBc	30us(for 100MHz jump)	VCO at 5V test chip
Ref[6]	0.25 um	Integer-N	-	-115.9dBc/Hz @1MHz offset	-	<100us(for 80MHz jump)	14mW at 1V
Ref[7]	0.18 um	Integer-N	Off-chip	-98.7dBc/Hz @0.5MHz offset	-	50us(for 80MHz jump)	8mW at 1.8V
Ref[8]	0.35 um	Integer-N	-	-117dBc/Hz @0.6MHz offset	-	<100us	66mW at 3.3
Ref[9]	0.18 um	Integer-N	-	-112dBc/Hz @1MHz offset	-	<10us(for 80MHz Jump)	3.8mW at 3.3

Table 2.1: Performance summary of different reported works

requirement. Also for the designs in [2] and [3], off-chip loop filters are used. The phase noise is small for the design [8] but realized in RF process. The phase noise performances of all other designs reported in the table are moderate. The off-chip VCO and programmable divider have

2.4 Specification

This section lists the output specification of an integer PLL from various datasheet available in the market.

Parameters	TI (LMX2581)	ST (STW81200)	Maxim IC MAX2870	Analog Device ADF4351
Operating Frequency	50 to 3760 MHz	46.875 to 6000MHz	23.5MHz to 6000MHz	35 MHz to 4400 MHz
Loop BW PM	256 kHz 50 deg	 NA	 NA	60 kHz
Icp Range	110 uA-3410 uA (5bit)	4.9mA (5bit)	0.32-5.12mA	0.312-5mA
Kvco	12 MHz/V -37 MHz/V	35MHz/V to 95MHz/V	100MHz/V	40MHz/V
Phase Noise VCO@1MHz	-132.6dBc/Hz	-135 dBc/Hz	-136dBc/Hz	-134dBc/Hz
Jitter (DJ)	100fS	NA	0.25ps	0.27ps
Settling Time	10uS	NA	NA	20us
Type 1.Integer 2.Fractional	 Y Y	 Y Y	 Y Y	 Y Y

2.5 Conclusion:

In this chapter some basic knowledge for frequency synthesizer has been reviewed. Different frequency synthesizer specification also have been briefly reviewed. Specification from industry have been discussed at the end to get better idea of target specification.

Chapter 3
CP architecture & design

3.1 Introduction:

Various CP architecture are available for PLL .These architecture have been studied and compared to find the suitable application for Wideband PLL. CP is one of the power hungry block its current consumption can be as high as 7mA to provide better spur performance over the leakage current. High CP current improves the PLL noise. But high current CP magnifies so many nonlinearities like charge injection, clock feedthrough, settling time etc. Different kind of CPs design techniques and issues have been addressed in following section.

3.2 CP Working Principle:

Charge pump is used to sink and source current into a loop-filter capacitor based on the UP or DOWN pulse with from the PFD. Basically the charge-pump (Fig 4.1) converts the difference between UP and DOWN pulses into current pulses and these current pulses change voltage drop on the loop filter impedance which is also

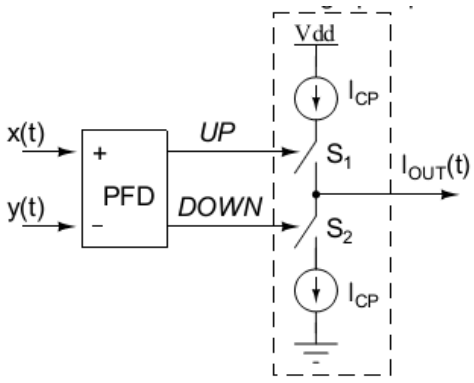


Fig -3.1

change the control voltage at the input of the VCO. When the rising edge of the reference input Fref leads that of the divided VCO feedback input, the PFD output UP is high and the charge pump delivers charges to the capacitors in the loop filter. Thus, the loop filter output voltage increases and do the VCO output frequency and phase. When the rising edge of the divider o/p Fdiv leads that of the Fref, then charge pump discharges the loop capacitor. Thus VCO output frequency decreases.

3.3 CP Architectures:

CP architectures are subdivided into two categories likely single ended and differential ended.

3.3.1 Single Ended CP:

Single-ended charge pumps are popular since they do not need an additional loop filter and offer low-power consumption with tristate operation. Three typical charge pump topologies namely switch at drain, switch at gate and switch at source are shown in figure [12].

1) Switch in Drain

First one in Fig. 4.2(a) is the CP with the switch is connected at the drain of the sources The up current (I_{UP}) and the down current (I_{DN}) of charge pump are realized by the transistors M_{UP} and M_{DN}, respectively. When the switch S2 is turned off, the current pulls the drain of M_{DN} to ground and transistor M_{DN} enters in deep linear region. After the switch S2 is turned on, the voltage at the drain of M_{DN} increases from ground to the

loop filter voltage held by frequency synthesizer and M_{DN}, enters in saturation region. During this switching time, high peak current (ignoring charge coupling effect) is generated by the voltage difference of two series resistors: M_{DN}, turn-on resistor and the switch turn-on resistor. On the pull up side, the same situation will occur and the matching of this peak current is difficult since the amount of the peak current varies with the output voltage increases from ground to the loop filter voltage held by frequency synthesizer and M_{DN} enters in saturation region. During this switching time, high peak current(ignoring charge coupling effect) is generated by the voltage difference of two series resistors: M_{DN}, turn-on resistor and the switch turn-on resistor. On the pull up side, the same situation will occur and the matching of this peak current is difficult since the amount of the peak current varies with the output voltage

2) Switch in Gate

Figure 4.2(b) shows the switch at gate topology where the gate is switched instead of the drain. In this topology, M_{UP} and M_{DN} transistors will be either in cut-off region or in saturation region depending on UP and DOWN signals. The capacitance seen by UP and DOWN signals, is substantial when the output current of the charge pump is high and the long channel device is used for better matching. This high Capacitance increases the switching time constant and limits the speed of operation. The bias current of Mp1 and Mn1 may not be scaled down since gmp1 and gmn1 also affect the switching time constant. Due to above problems, this topology is not widely used

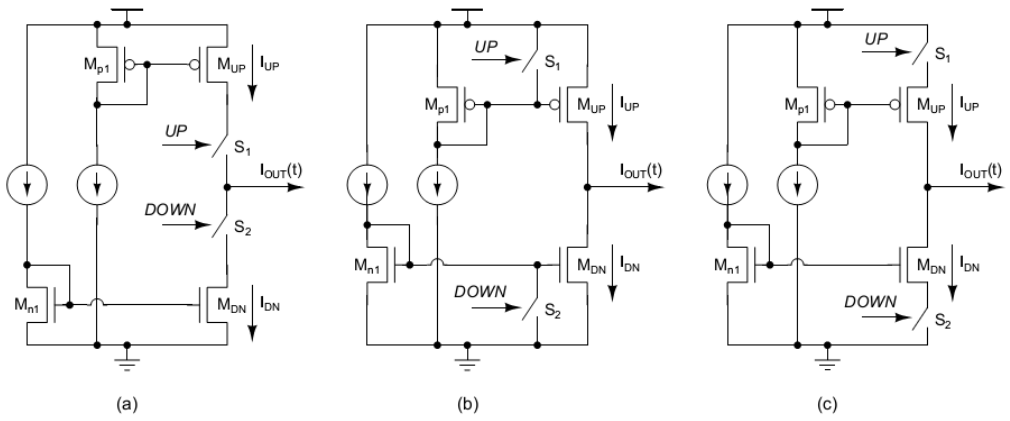


Fig-3.2 Type 1 (a) Switch at Drain (b) Switch at gate (c) Switch at Sour

3).Switch in Source

Figure 4.2(c) where switch is located at the source of the pull up and pull down current sources. Transistors M_{UP} and M_{DN} are in saturation all the time. Unlike the switch at gate topology, the capacitance seen by UP and DOWN signals is not large, and gmp1, gmn1 don't affect the switching time constant. As a result, the bias current of Mp1 andMn1 can be kept low with high charge pump output current. This architecture gives faster operating speed than the gate switching

Other than the basic topologies discussed so far, some variations are done to mitigate some specific problems associated with the architectures. Figure 4.3(a) shows switch at drain architecture with an unity-gain amplifier U1 and a dummy switching branch consists of S3, S4 switches [13]. The problem of the charge pump shown in figure 4.2(a) is the charge sharing between the nodes at the drain of M_{UP} M_{DN}; and the loop filter when the switch is turned on. When the switch S1 (S2) is off, the unity gain amplifier sets a voltage, which equals the charge pump output voltage, at the drain of M_{UP} M_{DN} through switch S3 (S4) to reduce the charge sharing effect when the switch S1 (S2) is turned on. In the similar way, the voltage at the drain of both M_{UP} and M_{DN} is set to the charge pump output voltage when both S1 and S2 are off. Thus the charge sharing problem of charge pump in 4.2(a) is reduced in the charge pump of 3.18(a). But the presence of amplifier adds the complexity and noise contributing components as well A charge pump with thecurrent steering switchis shown in figure 3.18(b). Because of the current steering switches (transistors Mp3 and Mn3) transistors M_{UP} and M_{DN} never go out of saturation. This improves the switching time and peak current matching as well. The performance is similar to the one shown in 4.2(a). This structure provides high-speed single-ended charge pump. In 4.3(c), the inherent mismatch of PMOS and NMOS is avoided by using only NMOS switches [14]. When UP signal is disable, there is no current flow in the current mirror Mp1 andMp2, thus the current mirrors still limit the performance unless large current is used. Also the up and down current paths have different switching time.

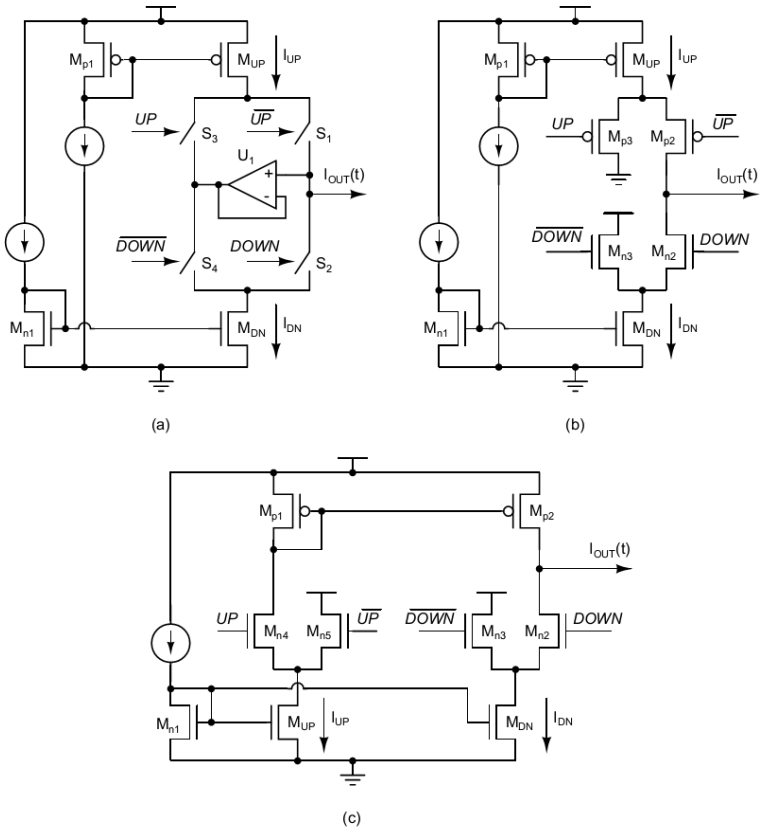


Fig-3.3 Type 2 (a) switch at drain with active amplifier, (b) with current steering switch, (c) with NMOS switches only

3.3.2 Differential CP:

The fully differential charge pump architecture has many advantages over the conventional single-ended charge pump [12].

i) The performance of the differential charge pump is less affected from the mis-matches between NMOS and PMOS switch transistors. Hence, the matching requirement between NMOS transistors and PMOS transistors are relaxed.

ii) The differential charge pump has switches using only NMOS transistors and the inverter delays for UP and DOWN signals do not generate any offset due to its fully symmetric operation.

iii) Differential configuration doubles the output range compared to the single-ended charge pump. It is very much helpful for low-voltage application because the limited

output voltage range of the charge pump makes it difficult for the VCO to meet the specified tuning range unless the VCO gain is increased.

iv) The differential architecture suffers less from the leakage current since the leakage current behaves as a common-mode offset with the dual output stages.

v) The differential charge pump with two loop filters provides better immunity to the supply, ground and the substrate noise when on-chip loop filters are used. However, these advantages can be achieved at the cost of two loop filters, common-mode feedback circuitry and more power dissipation due to the constant current biasing.

3.4 Challenges in CP Designing and There Effects in System:

3.4 .1 Leakage Current:

MOS switches, loop filter components are not ideal .So there always leakage current associated with the off condition of the CP. The leakage current can be 1 nA in sub-micron CMOS. It causes phase offset and leakage current synthesizers .The sideband due to the phase offset can be predicted assuming the narrow-band FM modulation [15].

If the spur level does not meet the requirement, then loop bandwidth should be reduced or the charge pump current should be increased.

3.4.2 Mismatch in CP Current:

Another consideration is the mismatch in the charge pump current. CMOS charge pumps usually have UP and DOWN switches with PMOS and NMOS current source respectively. These current values are not exactly same due to channel length modulation. This mismatch current creates periodic variation in the VCO control node which introduces spur .It can be minimized by minimizing with switching time of the CP.

3.4.3 Mismatch in switching Signal:

The timing mismatch is inherent in the PFD with the single-ended charge pump since the UP and the DOWN outputs have to drive PMOS and NMOS switches. The single gate delay mismatch in the PED is far more dominant over any mismatch in the charge

pump. Controlling the turn on time to reference frequency ratio, switching mismatch can be minimized.

3.4.4 Clock feed through:

The clock feedthrough mechanism is happened because of the coupling capacitance from the gate to both the source and drain of the CMOS device. This will cause a ripple at the output if the switches are placed next to the output terminal. A simple is placing the switch away from the output node. This will reduce the charge injection and clock feedthrough effects

3.4.5 Charge Injection

Charge injection is another consideration when designing a good CP. When the switches in CP are on, there are charges under the gate of the transistor. When the switch is turned off, the charge under the gate will be injected to voltage control through loop filter and creates voltage spike. There are several method to remove charge injection like 1) using transmission gate switch instead single MOS switch 2)using switch at source CP 3)using dummy MOSCAP at the o/p of switches.

3.5 Comparison:

There comparison between different types of CP has been tabulated.

Type-1 CP	Type-2 CP	Type-3 (Differential CP)
1. Low power consumption 2. Moderate speed 3. Applicable for low power frequency synthesizer.	1. Type-2 are mainly current steering type. 2.High speed .It can be applicable for high reference clock frequency	1.Low Skew Clock Generator 2. Medium Speed, Moderate power.

Table 4.1-CP Comparison Table

3.6 CP Programmability for Wideband PLL:

In my work I have chosen the switch at drain with active amplifier CP because of low power, less current mismatch and less settling time. The current of this CP has been decided from stability point of view.

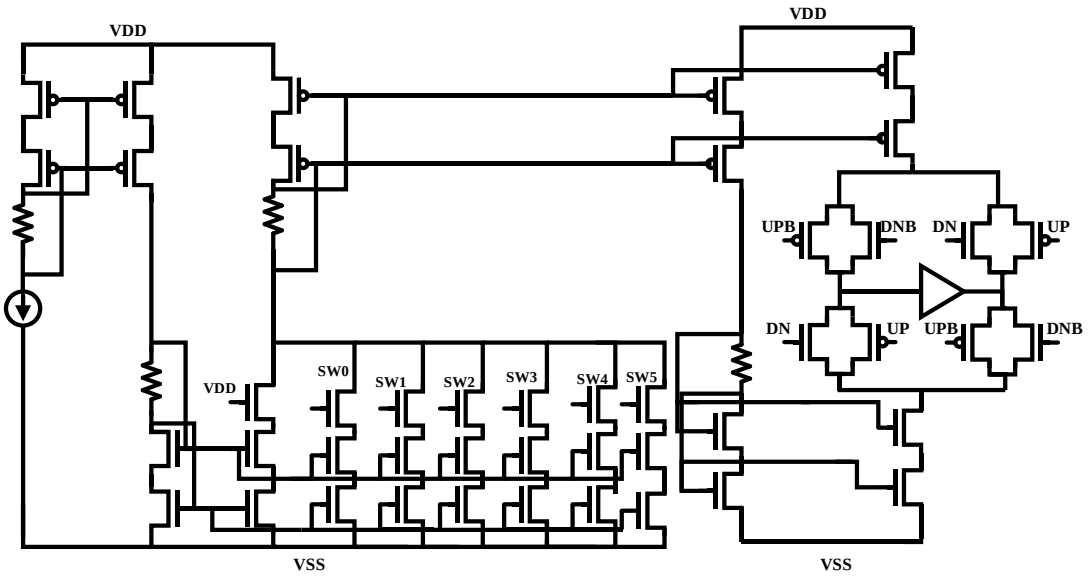


Fig-4.4 Programmable CP

As in designed PLL, the o/p frequency range is 25MHz to 3GHz, so the divider ratio changes from 64 to 127 to be comparable with input reference frequency i.e 25MHz.To counter this divider variation, CP current need to programmable. Here 5-bit binary current DAC has been designed, each current step is 22.3uA .At [00000] CP current is 1.13mA.INL has been given below.

Code No : Decimal	Real Value Icp(mA)	Ideal Value Icp(mA)	Mismatch(INL)
0	1.1327mA	1.1327mA	0
1	1.1547mA	1.1547mA	0
2	1.1768mA	1.1767mA	-90nA
3	1.1988mA	1.1987mA	-100nA

30	1.7926mA	1.7936mA	1uA
31	1.8146mA	1.8156mA	1uA
32	1.8364mA	1.8376mA	1.2uA
33	1.8583mA	1.8599mA	1.6uA
60	2.4519mA	2.4545mA	2.6uA
61	2.4739mA	2.47653mA	2.6uA
62	2.4959mA	2.4985mA	2.6uA
63	2.5179mA	2.5205mA	2.6uA

Table 3.2 CP INL Calculation

To check the CP mismatch, a voltage source is connected at the o/p of CP keeping all the switches in CP. Then voltage of the voltage source is being changed from 0 to 2.5V.From Fig 4.5, CP mismatch current is within 5nA for the voltage range between 0.4 to 2.1V.So voltage control range for the VCO is within 0.4 to 2.1 which is quite wide range.

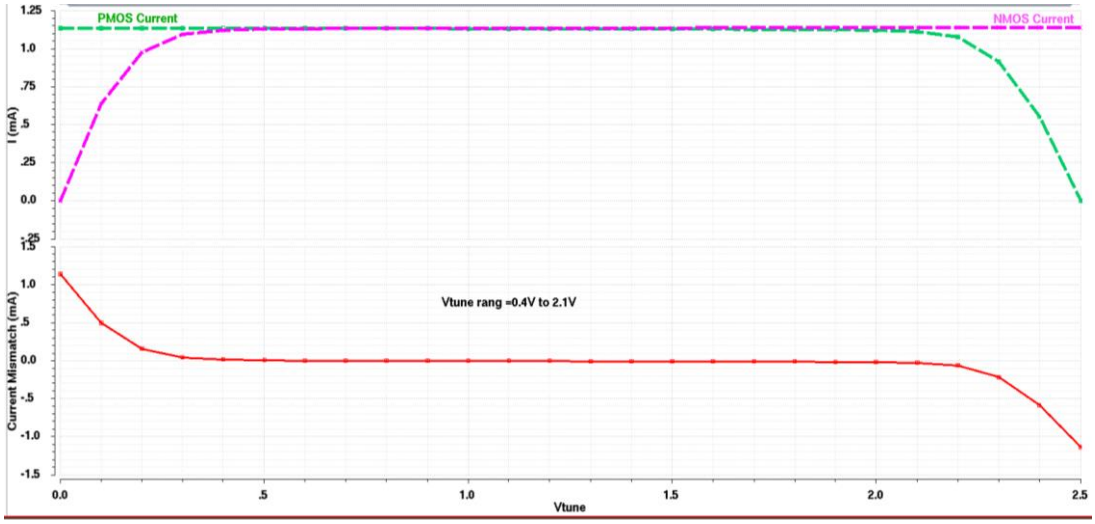


Fig-4.5 CP Mismatch

3.7 Conclusion:

Various issues of the CP has been discussed**.** CP current decides the loop stability and CP non idealities generates the spur in PLL**.** Depending upon the PLL architecture and its application, CP will be chosen accordingly.

Chapter 4

LF architecture & design

4.1 Introduction

Choosing the appropriate LF architecture is one of the key aspect of designing LF. Once LF order, phase margin, loop bandwidth, and pole ratios are chosen, the poles and zero of the filter can be determined. From these, we will evaluate the loop filter components. This chapter discusses the loop filter design aspects.

4.2 LOOP FLTER CHOICE:

The second order loop filter is the least complex loop filter and allows one to explicitly solve for the component values in closed form. The no of resister in second order filter is less so noise produced by thermal from resister is less.That's why for low jitter application 2nd order loop filter is most obvious choice.

4.3 PLL TF WITH LOOP DESIGN PROCEDURE:

To calculate the loop filter parameters, we have to visit the transfer function once.

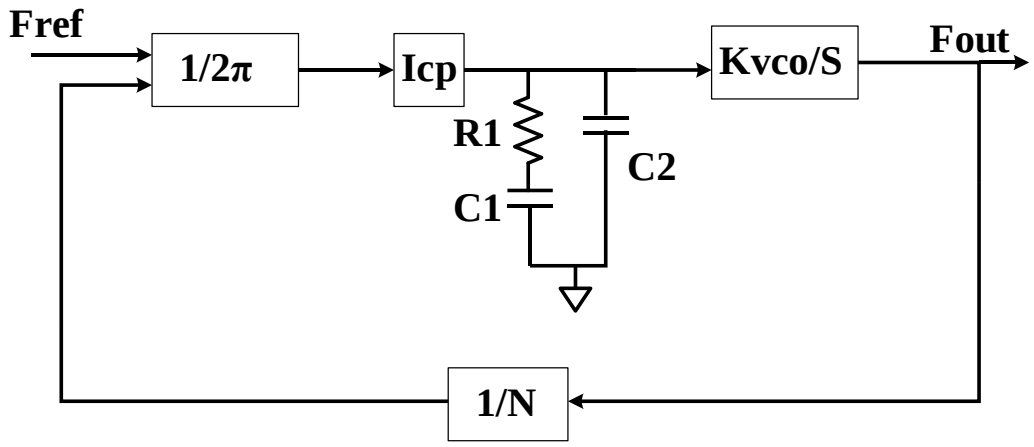


Fig 4.1 Design Considerations for Loop Filter Parameters:

The open-loop transfer function for the comple system is given below:

Where K_{PD} is the combine of CP and PFD gain, F(S) represents the LF TF.

$$LG(s) = K_{PD} \cdot F(s) \cdot \frac{K_{VCO}}{s}$$
$$= K_{PD} \cdot K_{VCO} \cdot \frac{s + \frac{1}{RC_1}}{C_2 s^2 \left(s + \frac{C_1 + C_2}{RC_1 C_2}\right)} \quad (4.1)$$

So the zero and pole locations of the total Loop are :

$$\omega_z = \frac{1}{RC_1};\ \omega_{p1} = \omega_{p2} = 0; \omega_{p3} = \frac{C_1 + C_2}{RC_1 C_2} \quad (4.2)$$

Phase margin for the complete system is :

$$\phi_M = \arctan\left(\frac{\omega_{ugb}}{\omega_z}\right) - \arctan\left(\frac{\omega_{ugb}}{\omega_{p3}}\right) \quad (4.3)$$

Wugb is the open loop unity gain bandwidth.

The phase margin of the total system solely depends on the C_1 and C_2 ratios. In order to get maximum phase margin we will take the derivative with respect to *Wugb* end equal the rsult eith 0 such that:

$$\omega_{ugb} = \omega_z \sqrt{\frac{C_1}{C_2} + 1}$$

$$\phi_{M\_max} = \arctan(\sqrt{\frac{C_1}{C_2} + 1}) - \arctan(\frac{1}{\sqrt{\frac{C_1}{C_2} + 1}}) \quad (4.4)$$

So design procedure for loop filter is as follows

1. Loop Band width(Wu) and Phase Margin(PM) Will be Given

2. Chose Kc=C1/C2 ration according to phase margin.

3. Chose R depending on the thermal noise which leads to jitter.

4. From UGB, determine the Icp to make system stable.

5. For Wide band PLL, divider ratio varies So ,Icp need to be adjusted accordingly

In this work following are the loop filter parameter to meet the jitter and stability specifications:

Parameter	Values
C1	180pF
C2	18pF
R1	8.35KOhm
Icp	2.5mA
Kvco	110M
N	120
PM	56deg
BW	400KHz

Table 4.1

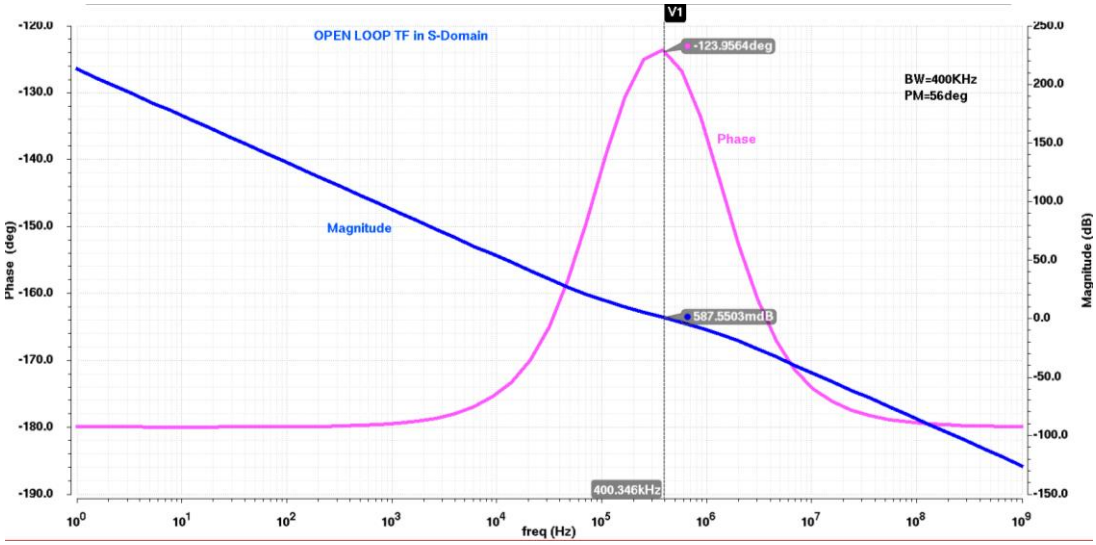


Fig 4.2 OPEN LOOP SIMULATION IN S-DOMAIN

4.4: Overall Effect of Loop Filter on Final PLL Jitter:

Following equations show the overall transfer function from each and every node

$$NTF_{IN}(s) = \frac{\Phi_{OUT}(s)}{\Phi_{IN}(s)} = \frac{N \cdot LG(s)}{1 + LG(s)}$$

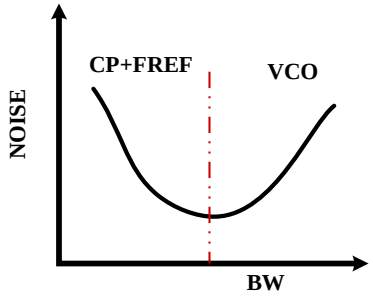
$$NTF_{DIV}(s) = NTF_{IN}(s)$$

$$NTF_{CP}(s) = \frac{\Phi_{OUT}(s)}{i_{CP}(s)} = \frac{2\pi}{I_{CP}} \cdot NTF_{IN}(s)$$

$$NTF_{R}(s) = \frac{\Phi_{OUT}(s)}{v_{R}(s)} = \frac{\frac{K_{VCO}}{s}}{1 + LG(s)}$$

So PLL acts 1)a low pass filter for the Fin ,Fdiv and CP noise 2) high pass for VCO o/p frequency 3)band pass for regiter noise.That why band width of the PLL

has to be selected carefully .Like for high BW PLL ,VCO noise will be corrected



more but it will amplifie the noise from the input clock..

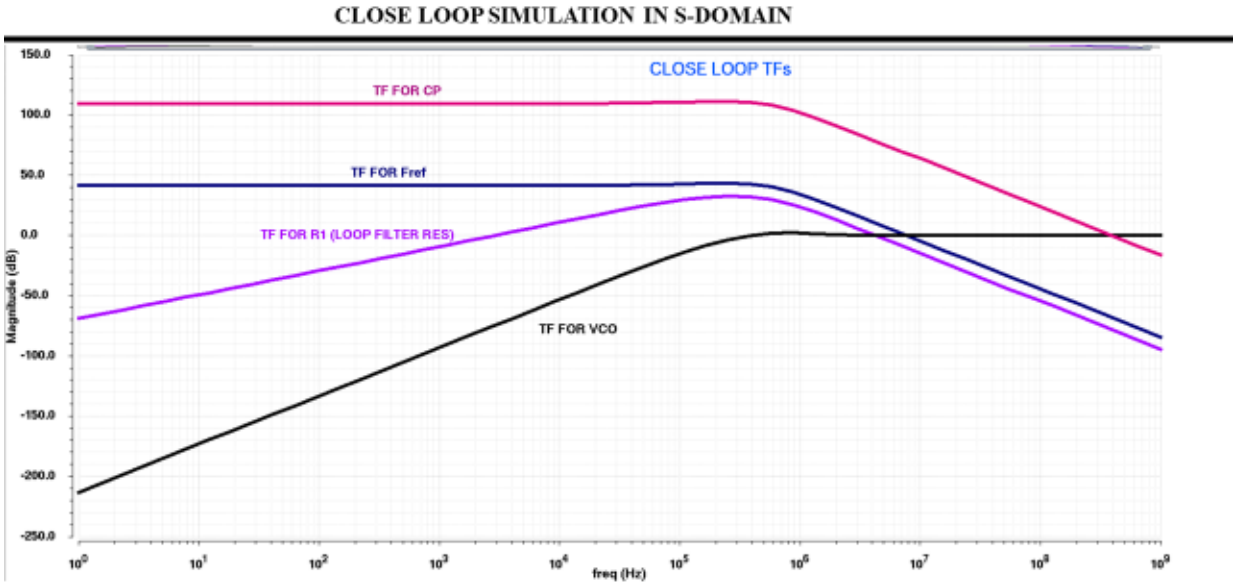


Fig 4.3 TF from all noise sources in PLL

If we change the BW we can check the variation in Jitter values .It has been experimented below.

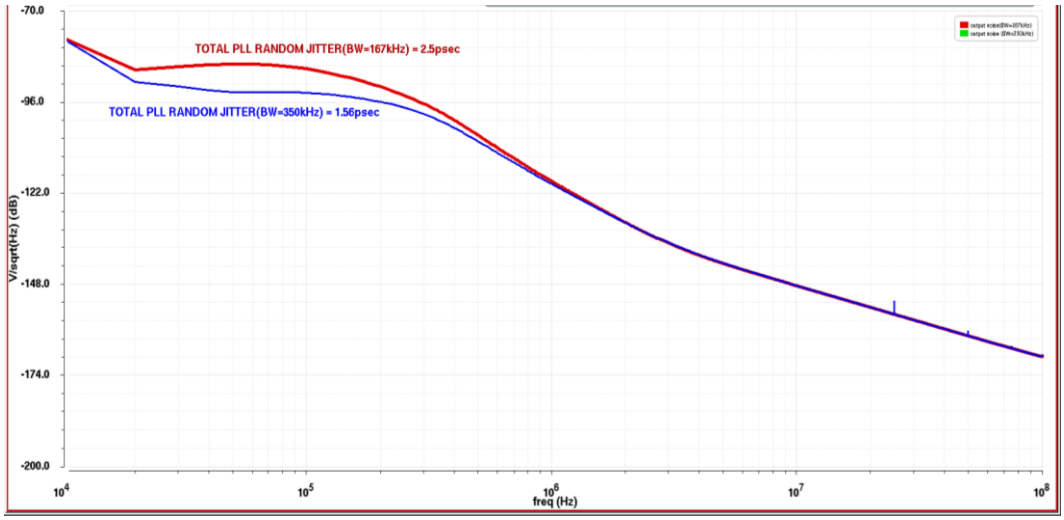


Fig 4.4 Jitter value according to the loop BW

4.5 Conclusion

The formulas for the second order passive loop filter have been presented in this chapter. Transfer functions for each and every noise sources has been checked and BW for overall system has been chosen accordingly.

Chapter-5

Jitter Modeling

5.1 Introduction:

Jitter can be defined as “the short-term variation of a signal with respect to its ideal position in time. Calculating this jitter in Cadence accurately is the key function in this chapter. There are two different deterministic jitter and random jitter. Two different have been implemented to extract the accurate value.

5.2 Types of Jitter:

5.2.1 Random jitter:

Source of random jitte(RJ) rare device thermal noise and flicker noise. Mathematically noise random jitter a unbounded function. RJ.is a significant contributor on overall jitter. The nature of RJ is hard to predict because of its randomness.

5.2.2 Deterministic Jitter

Deterministic jitter is not from unpredictable disturbance. It has specific reason to occur. This means it is repetitious at one or more frequencies. Therefore deterministic jitter can be taken care easily within specific bound. Deterministic jitter has two categories 1) periodic jitter and 2) data-dependent jitter. Switching power supply at particular frequency generates periodic jitter. In contrast, inter symbol interference (ISI) is an example of data-dependent jitter from an isochronous. These protocols use dynamically changing duty cycles and irregular clock edges, which contribute to overall jitter. Data-dependent jitter measurement varies by system, functionality, and other factors, and are not specifically addressed in this document.

5.3 Steady State Closed Loop Model in S-Domain:

To calculate the total jitter, the first step is to model each sub-block of the PLL in Cadence. A phase noise profile is then injected for each sub-block. The PLL schematic with phase noise injection for each sub-block is given in Fig

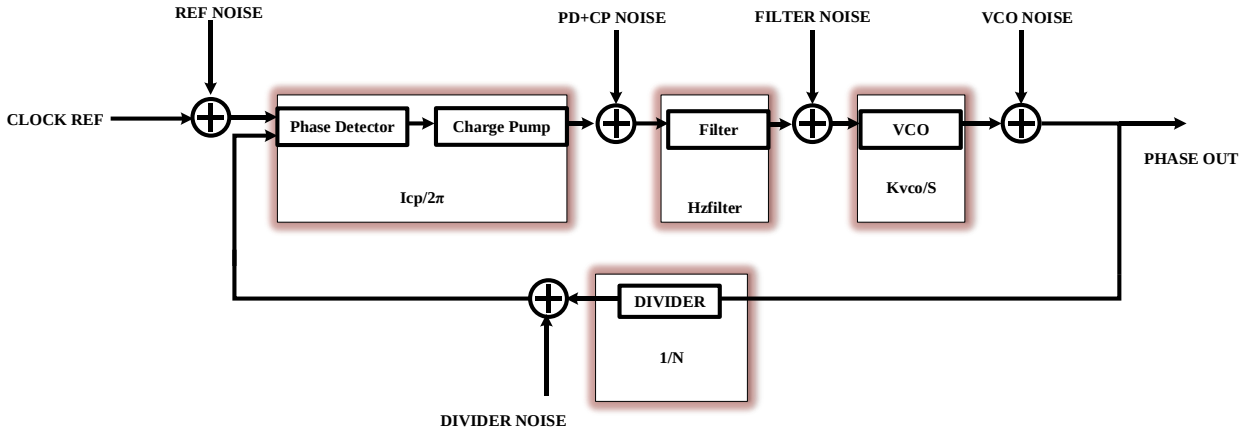


Fig-5.1

Jitter is a time domain phenomenon while phase noise is frequency domain phenomenon. In theory and with perfect measuring equipment, phase noise measured to an infinite carrier offset would provide the same value as jitter. In practical there is always some mismatch between two values.

5.4 Method for calculating RJ:

Calculation of RJ started width the simulation of PSS for each and every block. Then all the CSV file generated from the PSS , will be added to the system shown in Fig 5.1.Then next task is simulation of noise profile generation after filtered by the PLL. All the filtered noise file will be combined together and then we will the noise profile up to 100MHz carrier offset. To get the phase jitter,we have to multiply the area by 2 ,after that take the root square value. This unit is in radian. It can be converted in time domain by dividing upon the carrier frequency. Calculated RJ is 2.5pS.

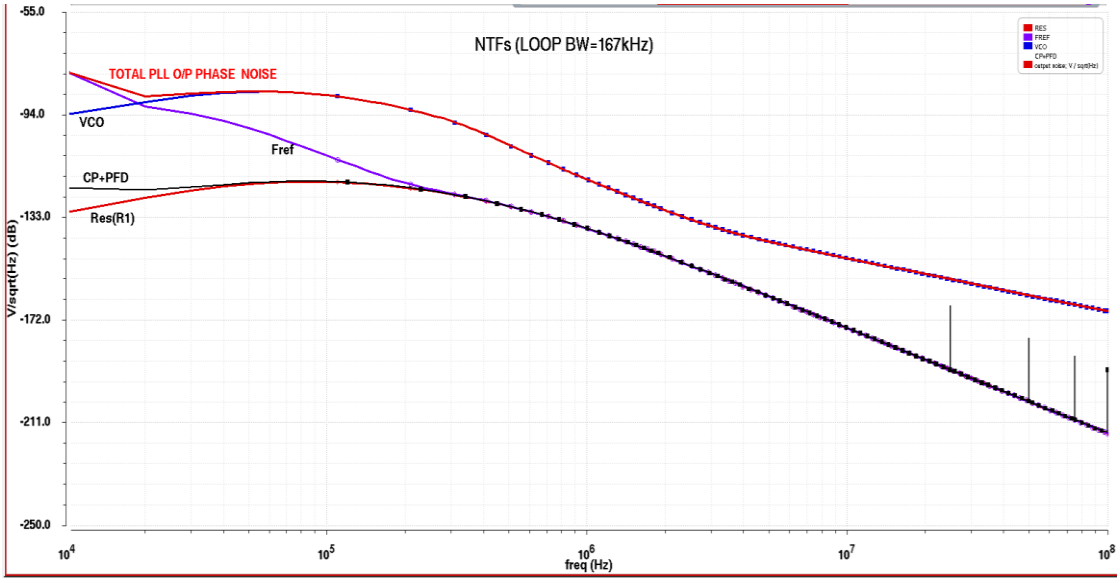
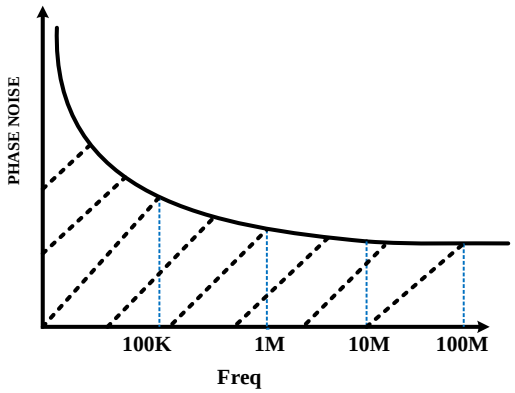


Fig-5.2 Phase noise Plot for each and every block by through PLL.



$$\mathbf{A}=\int_{10K}^{100M} V^2 dF$$

$$\textbf{RMS Phase Jitter(radian)}=\sqrt{2*A}$$

$$\textbf{RMS Phase Jitter (seconds)}=\frac{\sqrt{2*A}}{2\pi*f}$$

Fig-5.3 Calcultion of RJ

5.4 Method for calculating DJ:

Transient simulation is performed to calculate the DJ. Control voltage point is periodic in nature even after PLL is locked. This translates to periodic frequency variation at the o/p of VCO. To perform the DJ calculation here 2 cycle have been considered. Then through integration operation, frequency modulation value has been evaluated. This integrated value has been multiplied with Kvco and divided by the carrier frequency.

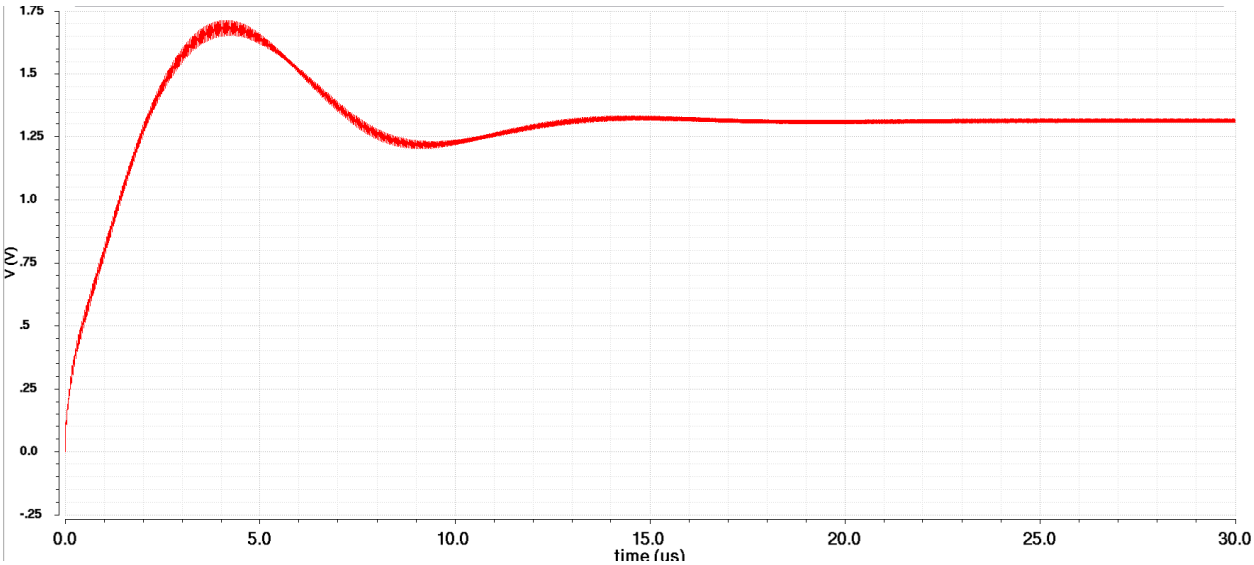


Fig-5.3 Vtune after Transient Simulation

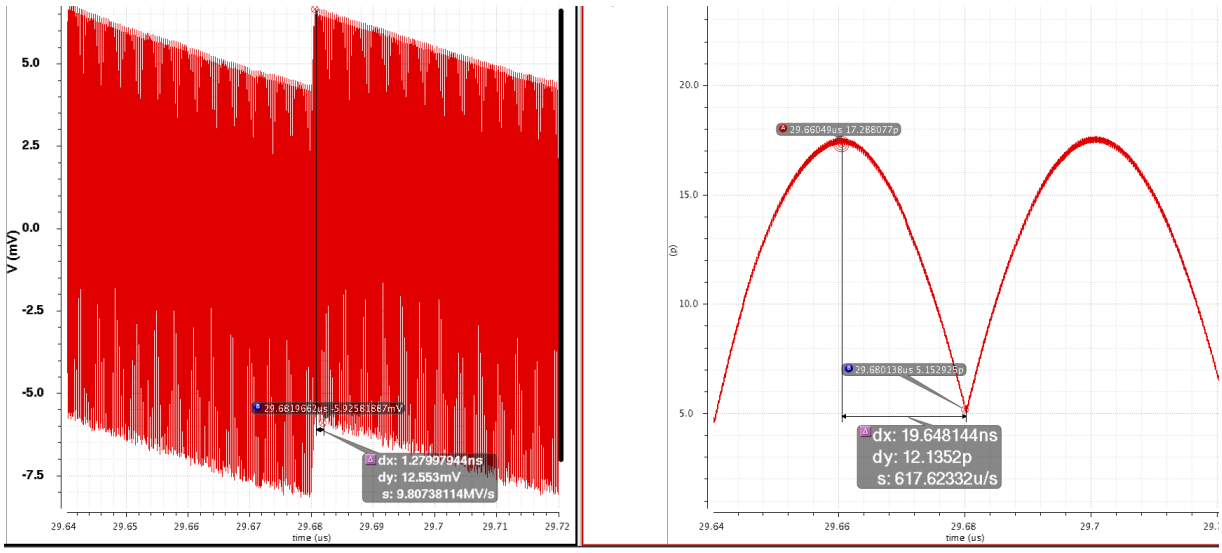


Fig-5.3 DJ calculation method

Over all DJ of full system is 150fS where Kvco=90MH/V ,f=3GHz,Vp-p=12.13pV

5.5 Conclusion:

RJ and DJ calculation method needs special attention to get the accurate result. With help of Cadence RJ and DJ has been calculated. So we no need to use MATLAB or other tool to get the result.

Chapter-6

PLL Simulation result and Future work

6.1 Introduction

This chapter solely devoted to PLL transient simulation result. Settling time, stability, jitter all are calculated to verify the PLL design(Fig 6.1)

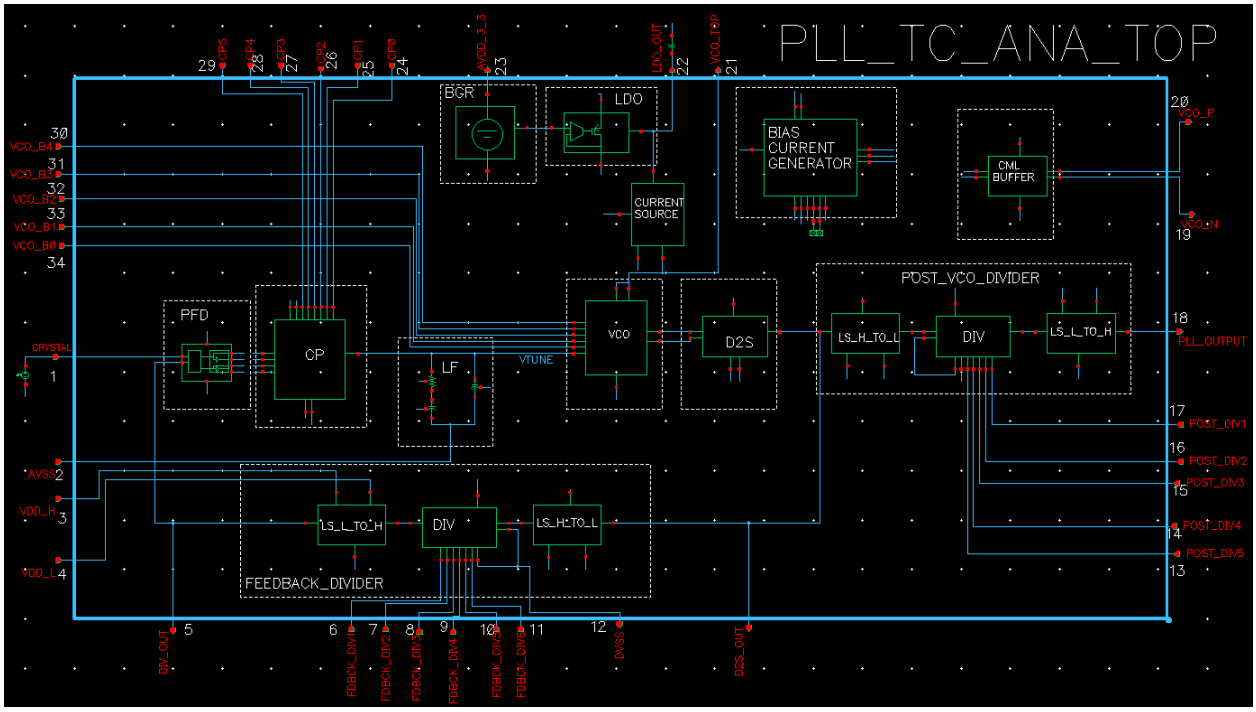


Fig-6.1

6.2 Operating voltage

Parameter	Min	Typ	Max	Units	Details
VDDA1 Analog voltage	3.0	3.3	3.6	V	At module boundary
VDDA2 Analog voltage	2.2	2.5	2.7	V	At module boundary
VDDD1 Digital voltage	2.2	2.5	2.7	V	At module boundary
VDDD2 Digital voltage	1.07	1.2	1.32	V	At module boundary
VDDD1noi			100	mVp2p	
VDDD2noi			100	mVp2p	

Table 6.1: Operating voltage

Two supply voltages (VDDA1, VDDA2) are used for supplying power to sensitive analog blocks. For digital interface, also two power supplies (VDDD1, VDDD2) have been used.

The core supply drops at chip-level are budgeted as shown below:

Nominal Supply is 3.3V, 2.5V, 1.2V

Static Variation: +/- (7%)

Chip-level IR drop: +/- (2%)

Thus, at the boundary of PLL, design consideration has been taken care, taking into account of lower minimum voltage of all power supplies.

6.3 Operating temperature

Parameter	Min	Typ	Max	Units	Details

T_j Junction temperature	-40	27	120	degC	
T_{jEM}			100	degC	For EM signoff

Table 6.2: Operating temperature

6.3 PLL Input Clock Requirements

The input clock to PLL is derived from an external crystal. The input noise of crystal within the LOOP-BW is passed unfiltered and high frequency noise i.e. out of LOOP-BW is filtered out.

Table 6.3: Input clock requirement

Parameter	Min	Typ	Max	Units	Details
$FREQ_{pllinclk}$ Input Clock Frequency	15	25	100	MHz	
$FREQ_{loopclk}$ Loop Clock Frequency	15		30	MHz	Pll_prediv_i [2:0] programming to be done

Parameter	Min	Typ	Max	Units	Details
$FREQ_{pllinclk}$ VCO Clock frequency	1.7	25	3.2	GHz	
$FBDIV_{int}$ Feedback-divider range	64		123	Integer Decimal	FDBCK_DIV_CNTRL_[5:0] programming has been done
POSTDIV Post-divider range	16		31	Integer Decimal	POST_DIV_CNTRL_[4:0] programming has been done
PFD reset pulse width	400	450	500	ps	To switch on the CP switches, minimum clock pulse would be the minimum reset pulse width.

6.4 PLL Output Specifications

This section lists the output specifications of the PLL

Table 6.4: PLL output clock characteristics

LOOP BW(2^{nd} order filter) PM		400 57^0		kHz	LOOP filter parameters are R1=7.5k,C1=170pF,C2=17p
Icp range	1.12		2.5	mA	Icp has to be decided according to feedback divider value
Kvco	60		120	MHz/V	SCA combination[5:0] has been designed to

					accommodate broad band.
Phase Noise of VCO @10K @100K @1M		 -77 -101 -127		 dBc/Hz	
RJ_{clkout} N-period RMS jitter			2.2	ps RMS	
DJ_{clkout} Deterministic jitter			300	fs RMS	Clock feedthrough and Vctrl periodic variation contributes DJ, has been measured for 3 cycles.
DC_{vcoclk} Duty Cycle	25		60	%	40-55%for post-div =1 45-55% for post div=2 25-55% for post div more than 2(using 2/3 Divider module)
$T_{lock\_powerup}$ Lock Time		10		us	PLL lock time for lock assertion. This lock time is for large frequency change at the input frequency or divider bits
Fppm Ppm accuracy of pll_clkout defined			3000	ppm	Frequency accuracy of the synthesized clock with respect to target value measured over 100us time

					duration (0.3%)

6.5 Power Consumption

BLOCK	Min	Typ	Max	Units	Details
VCO	14	18	22	mA	ACROSS all process
CP	1.12		2.5	mA	Across all divider combination
PFD		230		uA	TT @27
DIV		800		uA	TT @27
LS+D2S		7		mA	TT @27
Power Management		740		uA	TT @27

Table 6.5: PLL power consumption

6.6 PLL configuration

The PLL input clock (pll_clkin_i) after pre-division is referred to as "loopclk". The internal analog output of the PLL is called "vcoclk". The "vcoclk" and the "loopclk" are related by the feedback division ratio (integer). The "vcoclk" after post-division is called pll_clkout_o. Refer Figure 3.1. The relations between the different clocks are established by correctly programming the dividers as described:

The post-divided clock of frequency FREQ_pllclkout is given out on pll_clkout_o .The value of pll_fbdiv is provided by integer and fractional registers for FBDIV. The PLL registers are programmed by APB interface. PLL output frequency formula with respect to input and configuration bits is given as follows prediv = 0 and prediv = 1 will act a bypass for pre-divider

Few examples of the input and output frequency relationship with multiplication factor has been given below :

Pll_clkin(MHz)	prediv_i	Pll_pre_div_i<2:0>	Fbdiv_int_i<6:0>	Vco_clk (MHz)	Postdiv_i	Pll_clkout_o(MHz)
25MHz	1	2b01	120(6b1110000)	3G	0	3G
25MHz	1	2b01	100(6b1001110)	2.5G	1	1.25G
25MHz	1	2b01	70(6b0000110)	1.75G	0	1.75G

Table 6.6 Output frequency configuration

6.7 Future Work

1. Testing the silicon result::Integer PLL has been taped out and silicon result has to be proven in future.

2. Implementing self calibration technique for VCO: There are 5bit controller for LC-VCO. To make LC-VCO process independent,5-bit controller will be controlled through the calibration algorithm.

3. SPI module integration with PLL_TC_ANA_TOP module. To reduce the no of test SPI module has to be developed.

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