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A True 1V 1 μ W Biomedical Front End with Reconfigurable ADC for Self powered Smarter IoT Healthcare Systems

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Abstract—This work proposes an ultralow power highly linear analog front-end (AFE) with an input dynamic range from $200\mu V_{pp}$ to $20mV_{pp}$. The system consists of a signal conditioning instrumentation amplifier (IA), two programmable gain amplifiers (PGA), a mixed signal automatic gain control (AGC), two sample and hold (S/H), a 10 bit successive approximation register (SAR) analog to digital converter (ADC), and a $\Sigma\Delta$ modulator with 10 bit effective number of bits (ENOB). A highly linear capacitively-coupled IA is achieved by increasing its feedback factor. Moreover, a transconductance (g_m) cancellation technique is proposed for achieving a high common mode rejection ratio (CMRR). The conditioned signal is digitized using a SAR ADC for an input range of $200\mu V_{pp}$ to $2mV_{pp}$, and, an opamp-shared $\Sigma\Delta$ ADC for an input range of $2mV_{pp}$ to $20mV_{pp}$. The selection between the two ADCs is done by the AGC. The full system is designed using 1V supply in UMC $0.18\mu m$ CMOS technology. The AFE (IA and the two PGAs) achieves an overall linearity of more than 12 bits, for an input range of $200\mu V_{pp}$ to $20mV_{pp}$ while consuming $300nW$ with a bandwidth of $0.05 - 250Hz$. The power consumption of the SAR ADC is $40nW$ while operating at a sampling frequency of $1KHz$. The $\Sigma\Delta$ ADC consumes $300nW$ at a sampling frequency of $32KHz$ with an OSR of 32. The proposed system is intended to be powered by an energy scavenging circuit without compromising its own performance. The system was successfully tested for an ECG signal obtained from PTB database.

I. INTRODUCTION

The growing demand for a low power, miniature bio-potential signal acquisition and digitization system is the motivation for this work. Recent research shows that majority of cardiac diseases are caused due to unhealthy habits e.g. improper diet, meager exercise, etc. A patient-centric healthcare system, emphasizing on prevention of such diseases and continuous monitoring, becomes most relevant in the present scenario. For such a healthcare system a portable, light weight and microscopic devices are in demand. The major bottleneck in the design of these systems is it's power consumption. The power of the system can be scaled by using a higher transconductance efficiency (g_m/I_D) of input devices and lower supply voltage for a particular technology node. But the supply voltage cannot be scaled below $V_{thn} + V_{thp}$ as switches will not be able to operate [1]. Further utilizing a higher g_m/I_D of input transistor will result in lower linearity in high gain stages. So a proper optimized value of g_m/I_D is required for obtaining higher gain, linearity, output swing, while rendering low noise and consuming less power [2].

The bio-potential signal amplitude varies from tens of μV

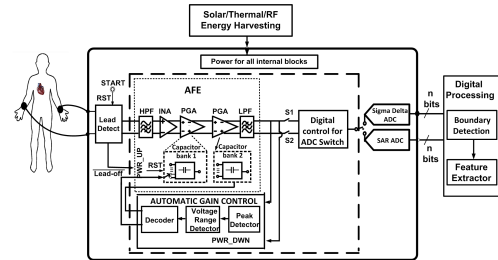


Fig. 1. Block diagram of the proposed acquisition system.

to tens of mV [3][4]. So acquisition system should have a noise level below the minimum signal amplitude for faithful digitization by the subsequent ADCs. The noise of the system is majorly contributed by the IA. Moreover, the flicker noise of IA dominates the overall noise, which in turn degrades the signal to noise plus distortion ratio (SNDR) of the whole system. The flicker noise can be decreased by increasing the width (W) of input transistors (g_m) [5] for a particular bias current, which results in increase of parasitic capacitance. The increase in the input referred noise in gain stages with capacitive feedback is inversely proportional to the net input capacitance [6]. To reduce the input referred noise a high input capacitor has to be used which leads to a lower input impedance. The input capacitor should be less than $100pF$ to have an impedance higher than $5M\Omega$ at $50Hz$ for power line rejection [7]. For a given noise, the higher input amplitudes have a higher SNDR if the gain is low. If higher gain is used for input amplitudes in the range of $5mV - 10mV$, the amplifier output becomes nonlinear because the output swing goes out of the linear range and hence degrades the SNDR of the AFE. Hence a trade-off is required between power, noise, linearity and the input impedance. The pseudo resistance also plays a major role in contributing non-linearity. Thus for achieving a high linearity, an output swing of $100mV$ is generally used [3]. In this paper two channels, one for high amplitude and other for low amplitude signal conditioning are proposed shown in Fig. 1. The multiplexing is done through AGC. Signals above $1mV$ are digitized using a $\Sigma\Delta$ ADC and signals below $1mV$ are digitized using SAR ADC. The AGC also controls the two PGA's as shown in Fig. 1. The IA and PGA are shared among the two channels.

The rest of the paper is organized as follows. Section II describes implementation of individual blocks Section III describes the S/H, SAR and $\Sigma\Delta$ ADC. Section IV shows the

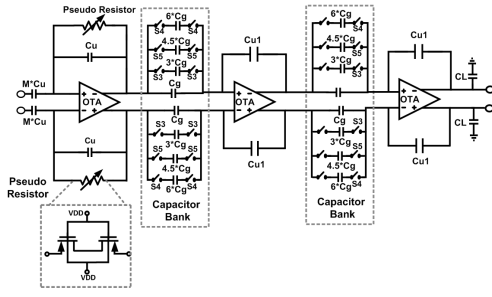


Fig. 2. Block diagram of instrumentation amplifier and programmable gain amplifier. Here $C_u = 0.5pF$, $M=10$, $C_g = 0.4pF$ and $C_{u1} = 0.4pF$.

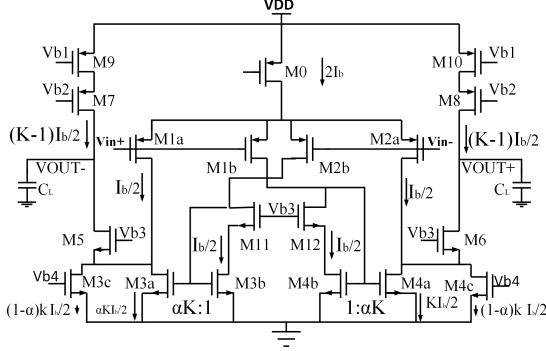


Fig. 3. Proposed improved RFC amplifier for higher CMRR at lower frequencies.

simulation results. Section V gives the conclusion.

II. IMPLEMENTATION OF INDIVIDUAL BLOCKS

A. Instrumentation Amplifier and Programmable Amplifier

The characteristics of an IA for biomedical signal acquisition are as follows (1) A CMRR of greater than $70dB$. (2) An input impedance greater than $5M\Omega$ at $50Hz$ (3) A high pass filter for removing the baseline wandering. (4) A high pass cutoff frequency lesser than $50mHz$ [8] (5) The low pass cutoff is given by the UGB of the amplifier and the closed loop gain. In this work, the gain of the IA is chosen to be 10 to process a signal of $10mV$ as an output swing of $100mV$ will give a high linearity. The Recycling Folded cascode topology is used in IA [9]. This topology renders a higher gain and g_m compared to the folded cascode topology for same power consumption. The differential gain for RFC is given by (1) and respective common mode gain is given by (2). The common mode gain of RFC with common mode feedback is expressed as in (3). The use of lower gain in IA decreases the CMRR as the differential gain is decreased. So to enhance the CMRR, a g_m cancellation technique is proposed on RFC topology as shown in Fig. ???. The DC current flowing through the transistors M3a/M4a is bypassed through M3c/M4c, which decreases g_{m3} . The expression for differential and common mode gain for the proposed amplifier is given in (4) and (5) respectively with CMFB.

$$A_{vDM} = g_{m1a}(K+1) * (g_{m5}r_{o5}(r_{o1a} || r_{o3a}) || g_{m7}r_{o7}r_{o9}) \quad (1)$$

$$A_{vCM} = \frac{g_{m1a}(K-1)}{1+g_{m0}r_0} * (g_{m5}r_{o5}(r_{o1a} || r_{o3a}) || g_{m7}r_{o7}r_{o9}) \quad (2)$$

$$A_{vCM-CMFB} = \frac{g_{m1a}(K-1)}{1+g_{m0}r_0} * \frac{1}{g_{mcmfb}} \quad (3)$$

$$A_{VDM-proposed} = g_{m1a}(\alpha * K + 1) * (g_{m5}r_{o5}(r_{o1a} || r_{o3a}) || g_{m7}r_{o7}r_{o9}) \quad (4)$$

$$A_{VCM-CMFBproposed} = \frac{g_{m1a}(\alpha * K - 1)}{1+g_{m0}r_0} * \frac{1}{g_{mcmfb}} \quad (5)$$

The common mode reduction in bandwidth of IA can be attributed to the introduction of a zero in the closed loop. The location of the zero and poles for common mode feedback is shown in (6).

$$H(s) = \frac{sC_1z_2[1+R_1sC_2-g_{mcmfb}R_1]}{[1+R_1(sC_1+sC_2)][1+\frac{g_{mcmfb}R_1}{R_1sC_2+1}+sC_Lz_2]} \quad (6)$$

where the load capacitor is represented as C_L and

$$z_2 = R_1 || \left(\frac{1}{sC_2}\right) \quad (7)$$

Two PGA's are used with a unity gain bandwidth higher than lower cutoff frequency to avoid decrease in 3db bandwidth with increase in gain. PGA's gain is set by the capacitor ratios. The PGA is implemented with RFC for $K = 3$ and $\alpha = 1$. The capacitor values are programmed by AGC for different gains based on the input signal amplitude. The AGC consists of a peak detector and a digital logic which calculates the peak value and accordingly gain is set shown in Fig. 2.

1) *Noise Analysis:* The noise of the IA is contributed by the modified RFC. The noise in RFC is generated by the flicker noise from M3 and M9 transistors. The noise equation for the RFC is shown in (8). In (8) μ_n and μ_p represents mobility of NMOS and PMOS respectively. The noise of proposed architecture is similar to RFC [9]. The major noise contribution is by M1a, M1b, M3a, M3b and M9. The noise contributed by M3b is higher compared to M3a in RFC because of current multiplication. In proposed architecture the noise due to M3b and M3a will reduce by α times but M3c contribution is $(1-\alpha)*K$ which adds up to same value. The noise contribution due to M3c can be decreased by decreasing the g_{m3c} and decreasing the load current i.e. current through M9 and M10. The noise of RFC and proposed architecture can be reduced by choosing $(1 < K < 3)$. The noise can also be reduced by using source degeneration resistors for M3a and M3b. The source degeneration resistors are neglected here to reduce the area.

$$V_f^2 = \left(\frac{2 * K_p}{C_{ox}L_{1a}W_{1a}(1+K) * f} \right) * \left[\frac{1+K^2}{1+K} + K * \frac{K_N\mu_n C_{oxn}}{K_P\mu_p C_{oxp}} \left(\frac{L_{1a}}{L_{3a}} \right)^2 \left(1 + \frac{W_{3a}}{W_{3b}} \right) + \frac{K-1}{K+1} \left(\frac{L_{1a}}{L_9} \right)^2 \right] \quad (8)$$

The total IA input referred noise power expression is shown in (9). The first term is due to the pseudo resistor and the second term is due to the capacitive feedback [6].

$$V_{in}^2 = \left[\frac{1}{sC_1R_1} \right]^2 * V_{nres}^2 + \left[\frac{C_{in} + C_p + C_f}{C_{in}} \right]^2 * V_f^2 \quad (9)$$

B. Sample and Hold, $\Sigma\Delta$ ADC and SAR ADC

The signal from PGA is passed on to sample and hold amplifier. There are two sample and hold in the proposed system, one for SAR ADC operating at a sampling frequency of 1 KHz, and the other for $\Sigma\Delta$ ADC operating at a sampling frequency of 32 KHz [16]. For a signal swing of 100mV, the 10 bit SAR ADC achieves a 7 bit resolution. For signals of amplitude greater than $2mV_{pp}$, a conventional discrete time (DT) cascaded integrator feedback (CIFB) modulator with 2^{nd} order noise shaping is chosen with a reference voltage of $400mV_{pp}$ Fig. 4. Owing to the fact that the integrator is the most power hungry block of the SDM, twofold strategy was employed to minimize the ADCs power consumption. The integrator is implemented using the enhanced recyclic folded cascode (ERFC) designed in 1V [10][11]. For DT $\Sigma\Delta$ ADC, the use of transmission gates as switches require higher aspect ratio for particular resistance which results in higher parasitic capacitance. So to drive these switches, switch drivers are required which consumes more power. The above constraint can be avoided by using level shifted clock phases without using transmission gates.

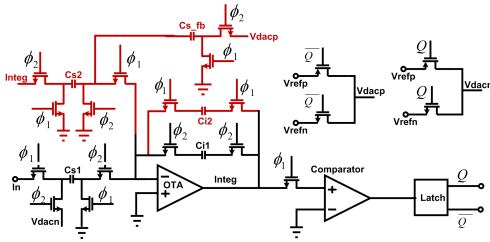


Fig. 4. Single ended representation of the fully differential opamp shared DT $\Sigma\Delta$ ADC. The circuit renders 1^{st} order noise shaping when only components in black color are activated, and 2^{nd} order noise shaping when the components in dark red are also activated. Here $C_{S1}=0.67pF$, $C_{S2}=2.02pF$, $C_{S_fb}=0.79pF$, $C_{i1}=4pF$, and $V_{cm}=0.9V$.

$$FOM1 = \frac{Power(W) * 10^{12}}{2^{\frac{SNR(dB)-1.76}{6.02}} * 2 * BW(Hz)} \quad pJ/Conv. \quad (10)$$

III. RESULTS

The performance of proposed AFE is compared in Table I. The linearity for lowest and highest values of input signal to the system can be verified from THD in Table I. The performance of $\Sigma\Delta$ ADC is compared in Table II. The FOM is calculated by the expression (10), which explains the power consumption per sample conversion. The common mode gain is reduced by 20dB for 50Hz and 60Hz line can be verified from Fig. 5. Frequency response of AFE with different gain tuning is plotted in Fig. 6. An ECG signal of amplitude 1mV is fed to the IA and the AGC performance was verified by the output of the PGA as shown in Fig. 7. The resistance plot

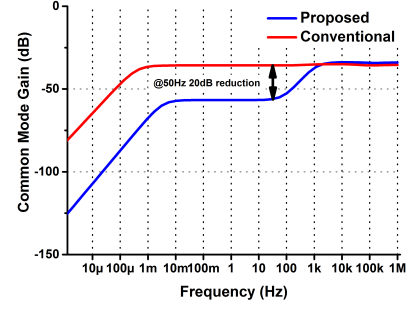


Fig. 5. Comparison between common mode gains of the conventional and the proposed amplifier.

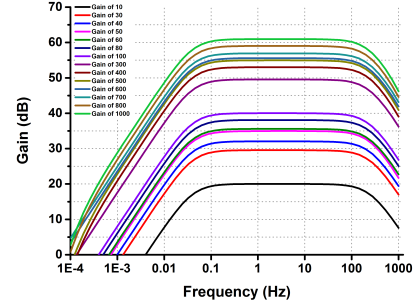


Fig. 6. PGA gain reconfigurability.

of the pseudo resistor is given in Fig. 8. The FFT plot of the output of the ADC for input of $20mV_{pp}$ to AFE is plotted in Fig. 9 for $\Sigma\Delta$ ADC and Fig. 10 for SAR ADC for an input of $0.2mV_{pp}$.

IV. CONCLUSION

An ultra-Low power biomedical signal acquisition and digitization is presented. The AFE does the work of filtering and amplification with a linearity greater than 12bits. The AGC controls the gain of the PGA such that the input to ADC is 100mV. Each block of AFE is designed for minimum power using g_m/I_D methodology and hardware sharing and phase level boosting is also implemented to minimize power consumption of $\Sigma\Delta$ ADC. The required performance is achieved with $1\mu W$ power.

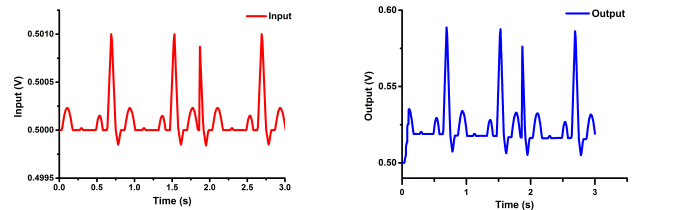


Fig. 7. Input and output ECG plots.

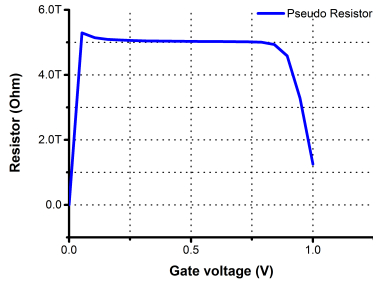


Fig. 8. Resistance plot of pseudo resistor.

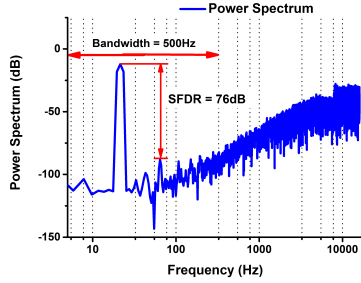


Fig. 9. Full system output power spectrum for a sinewave input of $20mV_{pp}$ processed by AFE, AGC, Sample and Hold and $\Sigma\Delta$ ADC, respectively.

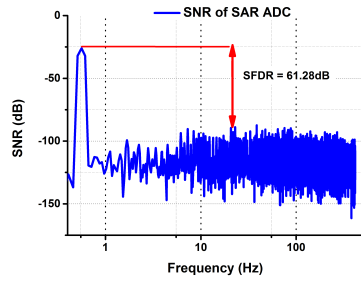


Fig. 10. Full system output Spectrum for a sine wave input of $0.2mV_{pp}$ processed by AFE, AGC, Sample and Hold and SAR ADC.

TABLE I. PERFORMANCE OF THE PROPOSED AFE

Parameter	Value			
	This work	[5],2006	[14],2012	[15],2013
Technology (μm)	0.18	0.35	0.13	0.13
Voltage Supply (V)	1	1	1	1.5
Midband Gain (dB)	20-60	40.2	40	40
Bandwidth (Hz)	0.5-250	0.003-245	0.4-8.5K	19.9K
Input Referred Noise	$6\mu V_{rms}$ for (0.05-250Hz)	$2.7\mu V_{rms}$ for (0.05-250Hz)	$3.2\mu V_{rms}$	$3.7\mu V_{rms}$
NEF	3.32	-	4.5	3.04
Offset(3σ)	$500\mu V$	-	-	-
CMRR @50Hz (dB)	75	61-64	>60	>78
PSRR (dB)	77	62-63	>60	>80
THD	0.057% @ $20mV_{pp}$ 0.067% @ $2mV_{pp}$ 0.1% @ $0.2mV_{pp}$	0.053% @ $5mV_{pp}$ @ 16Hz	1.5% @ $1mV_{pp}$	1% @ $16.5mV_{pp}$
Current Consumption (A)	300n	330n	12.5μ	2.6μ

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TABLE II. PERFORMANCE OF THE $\Sigma\Delta$ ADC

Parameter	Value		
	This work	[12]	[?]
Technology (μm)	0.18	0.18	0.18
Voltage Supply (V)	1	0.9	0.7
Order	2^{nd}	2^{nd}	2^{nd}
Bandwidth (Hz)	500	10k	8k
Fs (MHz)	0.032	5	1.024
Power Consumption (μW)	0.3	200	80
Dynamic Range (dB)	76	83	75
FOM1 (pJ/Conv.)	0.58	0.866	1.087

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