A 1.2V Wide-Band Reconfigurable Mixer for Wireless Application in 65nm CMOS Technology

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Abstract—This paper presents a wideband (WB) reconfigurable down-conversion mixer for multi-standard wireless receivers. The proposed mixer is re-configurable between active mixer and passive mixer modes. Reconfigurability is made through switching the input signal between gate and source terminal of input transistors and enabling/disabling the transimpedance stage at the output. The CMOS transmission gate (TG) switches are designed to provide optimum headroom in this low voltage design. The proposed circuit is designed in UMC 65nm RFCMOS technology with 1.2V supply voltage. From the simulation results, the proposed circuit shows conversion gain of 29.2 dB and 25.5 dB, noise figure of 7.6 dB and 10.2 dB, IIP_3 of -11.9 dBm and 6.5 dBm in active and passive mode respectively. Hence this circuit will be much helpful in multi-standard receiver design in IoT perspective.

keywords- Reconfigurable; passive; active; mixer; multi-standard; receivers;

I. INTRODUCTION

Emerging Internet of Things (IoT) enabled platform demands multi-mode multi-standard transceivers to enhance the performance through seamless connectivity between zigbee, bluetooth, Wi-Fi, UWB and cognitive radio interface. The easiest solution is to put multiple separate radio to above need[1]-[6], however, in real scenario only one of the mode function at a time. So above approach is power hungry, costly and take more area. Therefore, to get a cost effective solution, a re-configurable single radio (that can configure to multi-mode as need basis) would be the best choice. To make the radio re-configurable researchers introduce the RF transceiver front-end with reconfigurable LNA[7]-[8], PA, PLL[9], mixer[10]-[11], and filter[12] etc. Among them, our emphasis is to design a Mixer that can provide reconfigurlibity on the performances like gain, linearity , noise figure and bandwidth selection. Most of proposed reconfigurable mixer have shown gain variability and Bandwidth tuning[13]-[14] through current variation, load tuning etc[10]-[12]. In such designs, multi channel sensing and signal strength adaptablity are the main target and are designed for single standard operation. However, in multi-mode IoT systems, the other performances like noise figure, linearity reconfiguration are need to be incorporated in mixer design.In this regard, we propose a re-configurable down conversion mixer which is switchable between active and passive mode depends on the performance requirement as shown in Fig. 1.

The prime features of the mixer are:

1) Reconfiguration in single circuitry between active and passive modes with gain and noise tunability.
2) Common source topology is used for active mixer with a current source at the bottom. Transmission
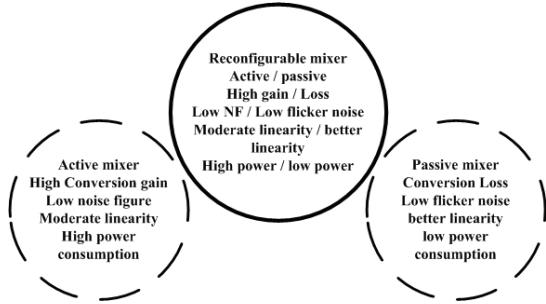

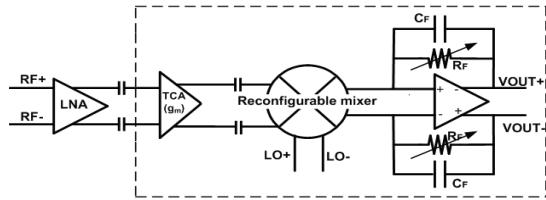Fig. 1. Trade-offs between active and passive mixers .

Fig. 2. Wide-band receiver front end.

gate is used as a resistance to provide optimum headroom. The current commutating passive mixer is designed by using four switching(LO) MOS with resistive degeneration.

3) PMOS switch is used to switch on or off Transimpedance amplifier.

Upto the best of our knowledge, first time one such work is being reported in IoT perspective and detail operation are described in following paragraphs as section II details the proposed architecture and simulation results are explained in Section III.

II. ARCHITECTURE OVERVIEW

The block diagram of wide-band RF front-end (demodulator) is shown in Fig. 2. The first building block in the wide band RF front-end is the LNA. So it is required to design high input impedance g_m stage to avoid loading effect. Simultaneously g_m stage provides high isolation between IF, LO and RF. The differential ended RF input is taken by RF balun using 50 ohm input impedance termination. All the signal paths are fully differential in style to suppress the common mode noise and second order harmonic.

This block consists of two types of mixer in single circuitry. Reconfigurable (Active/Passive) mixer consists of RF transconductance amplifier, switching stage and load stage.
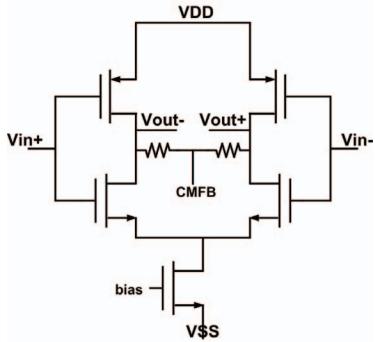
Fig. 3.   Transconductance amplifier.

Fig. 4.   Reconfigurable mixer.

Tranconductance amplifier that converts the RF input voltage into current is DC decoupled to switching stage. Mixer core output is coupled to transimpedance stage. IF voltage is built at the output of transimpedance amplifier after the RF current gets commutated in switching stage and passes to first order RC low pass filtering. TIA offers a virtual node for the g_m stage, resulting in high linearity. TIA power will be switch on or off in passive and active case respectively to save the power consumption. Unlike narrow-band designs, C_{PAR} (parasitic capacitance at the output node of the transconductance stage) is minimized to allow a less stringent noise specification upon the op-amp which favourably gets translated into lower power consumption circuit design.

A. Transconductance Amplifier

Fully differential CMOS transconductor is employed to convert the input RF voltage signal to RF current as shown in Fig. 3. Post which the current signal is fed to the switching stage ensuring that second order nonlinearity is reduced by using fully differential topology. TCA is modeled with a frequency dependent source impedance $Z_S(\omega)$ is desired to minimize the signal loss and enhance its linearity performance according to (1),(2) [5]

$$IIP_2 \approx K_a \frac{Z_L(\omega_1)Z_s(\omega_1 - \omega_2)}{Z_L(\omega_1 - \omega_2)f[Z_L(\omega_{LO} - \omega_1)]} \quad (1)$$

$$IIP_3 \approx K_b \frac{Z_L(\omega_{LO} - \omega_1)Z_s(2\omega_1 - \omega_2)}{Z_L[\omega_{LO} - (2\omega_1 - \omega_2)]g[Z_L(\omega_{LO} - \omega_1)]} \quad (2)$$

Where TIA stage is modeled as the load impedance of mixer $Z_L(\omega)$, ω_1 ω_2 represent the two nearby RF frequencies of input tones, and ω_{LO} represents the LO frequency.

The common mode voltage is designed at VDD/2 for getting maximum swing. By setting this common mode voltage, current can be minimized and parasitic capacitance at the output nodes of transconductor is optimized to the smallest possible value thereby increasing the output impedance, for the purpose of improving the NF. Transconductance stage gain also reduces the overall noise of front end receiver. Common mode feedback for the tranconductance stage needs to be carefully designed for proper operating point.

B. Common Source Reconfigurable Mixer

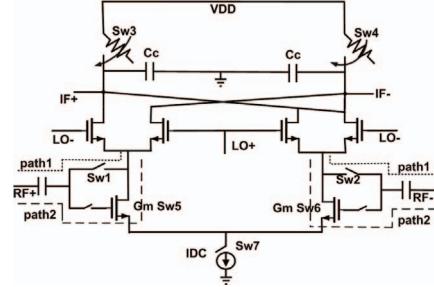In this embodiment, modulator circuit is reconfigured between active and passive modes by switching between the output load, DC power supply and Gm stage (Gm MOS of active case) and current source shown in Fig. 4. Common source configuration is chosen because of compatibility with cases.

In passive mode, the frequency mixer or modulator circuit is simply composed of four NMOS transistors characterized by resistance (Ron) when switched on. Accordingly, in order to make the common-source input stage configuration suitable for both active and passive mode topologies, switch (Sw1-2) are implemented using PMOS which have been added between the gate and drain of the common source transistor (Gm MOS)as shown in Fig. 4. TCA differential output current is applied at the drain of the transistor Mp1 and Mp2 (PMOS switch 1-2) to route to the mixer core for mixing in the current domain. Vlogic high or low is given to Mp1 and Mp2 to configure reconfigurable mixer to operate in an active/passive mode as shown in Fig. 5(a). Specifically when there is no current flowing through the mixer core, Vlogic is set to zero, thus causing input signal to flow directly through the switching stage as shown in path 1 to mix with LO signal. Width of PMOS is chosen to provide degeneration resistance, thus turning the overall mixer topology into a passive mode as shown in Fig. 6(a). Transistors thus operate as switch 1-2 as well as degeneration resistance R_{deg}(switch 1-2 resistance), thereby increasing linearity of passive mixer [6]. Capacitor Cc is a high-frequency compensation capacitor used to suppress the noise at higher frequency. The output signal is supplied from the mixer core without any load and directly coupled with transimpedance amplifier. The voltage conversion gain of passive mixer is

$$VCG = \frac{2}{\Pi} * g_m * Z_F \quad (3)$$

where Z_F is the feedback impedance of transimpedance amplifier, C_F parallel with R_F and g_m is the transconductance of transconductance amplifier.

Resistive switches 3-4 designed using transmission gate, made of PMOS and NMOS switch, are fully turned off ensuring that output current of switching quard directly goes to the transimpedance amplifier without any coupling capacitor. Switches 5-7 designed using NMOS will also be off when this circuit operates in passive mode.

In active mode, input stage of the frequency mixer or modulator circuit have a configuration that is a common source topology. This topology is chosen to provide better gain and low noise figure. Double balance gilbert cell architecture is used in active configuration when there is current flowing
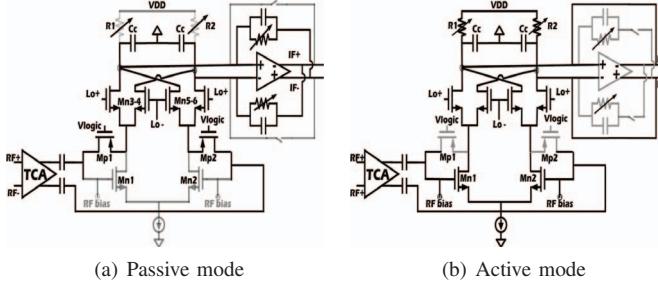
(a) PMOS switch   (b) Resistive switch

Fig. 5. Switch implementation using MOS

(a) Passive mode   (b) Active mode

Fig. 6. Reconfigurable mixer in passive and active mode

(a) Schematic of TIA stage

(b) Schematic of OTA

Fig. 7. Transimpedance amplifier

Fig. 8. Simulated conversion gain reconfigurable mixer vs RF frequency.

through input(Gm) MOS Mn1 and Mn2 (Sw 5-6). The bias voltage can be selected to control parameters of input stage or switching operation of Gm MOS switch 5-6 as shown in path 2. The Gm of MOS Mn1 and Mn2 can be changed by changing the value of bias voltage, thus varying the gain of mixer. The optimum value of bias voltage is so desired so that mixer consumes a minimal amount of current. Switch 7 has been designed using NMOS which is biased in saturation region to provide current source. Thus turning the overall topology into an active mode as shown in Fig. 6(b).

Transmission gate is used as a resistive switch connected between VDD and IF output as shown in Fig. 5(b). W/L of PMOS and NMOS is chosen so that some voltage drop occurs across it and act as a resistance. Transmission gate total resistance is $Rtol = R_PMOS||R_NMOS$. As it is connected to VDD so it acts as resistive load and Capacitor Cc is provided to act as a low pass filter in active mode operation of reconfigurable mixer. Gain of active mixer can be tuned by changing the resistance of transmission gate. The output of active mixer is directly passed to the output stage without going to TIA.

C. Transimpedance Amplifier

A simplified schematic of transimpedance amplifier is shown in Fig. 7(a). TIA consists of an operational transconductance amplifier with a feedback $R_F C_F$. R_F and C_F value is set according to IF frequency. A two stage miller compensated OTA topology is chosen for TIA design as shown in Fig. 7(b). First stage to provide high gain and second stage for high swing. So that structure can obtain both, high output swing and low input referred noise. Transimpedance amplifier is used to convert current to voltage output in passive mode operation. The TIA stage serves as load and anti-aliasing filter for the passive mixer. The TIA is designed in such a way so that very low impedance is provided at the passive mixer output. TIA input impedance is given by

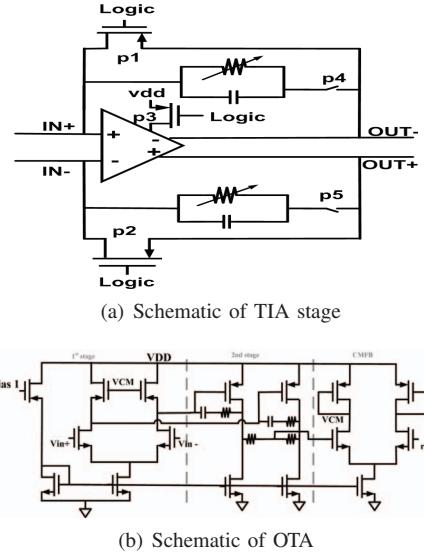$$Z_{in}(f) = \frac{2}{A(f)} * \frac{R_F}{1 + 2\Pi R_F C_F} \qquad (4)$$

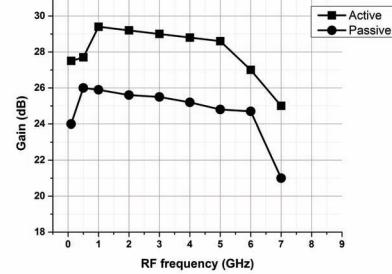Where $A(f)$ is the open loop gain of the OTA. Due to high gain OTA bandwidth is limited and high frequency components suffer high impedance. In order to filter out high frequency components C_F is inserted. This is done for all signal current to flow into feedback $R_F C_F$ from the mixer core. The TIA draws a total of 3.3mA from the supply. In case of active mixer operation TIA will be switched off to save power. In case of active mixer operation TIA will be switched off by switching off p3 switch to save power and p1, p2 will be on. p4 and p5 also implemented using MOS and switch on or off in case of passive and active respectively. The gain of the TIA can be tuned by changing the value of R_F and it provides another degree of freedom to configure the gain of the downconverter.

III. SIMULATION RESULTS

Based on the qualitative description of the building blocks, using their insights related to operation, the RF front-end demodulator is simulated in CMOS 65nm process. The voltage conversion gain plot is shown in Fig. 8 with respect to RF frequency at 5MHz IF. The voltage conversion gain is close to 29.2dB and 25.5dB for acive and passive case respectively.

The simulated double side band noise figure at 2.45GHz is shown in Fig. 9. In addition, the corner frequency is less than 100KHz in passive mode operation. Simulated noise figure for active and passive is 7.6dB and 10.2dB @ 5MHz respectively.

TABLE I. SIMULATION RESULTS AND COMPARISON

Parameters	Active (This work)	Passive (This work)	[2]	[3]	[5]	[6]	[4]	[10]	[11]	[12]
Gain (dB)	29.2	25.5	14.5	13	21	22.5-25	35	9-24	1.2-17	3.5-20.5
Noise figure (dB)	7.7	10.2	6.5	13.7	10.6	7.7-9.5	10	NA	≥ 11	≥ 8
IIP3 (dBm)	-11.9	6.57	NA	≥ 10.8	9	≥ 7	11	3.5 to -12	8.6	≤ 8.5
1dB-CP (dBm)	-24.5 @ 5MHz	-14 @ 5MHz	-13.8	NA	NA	-12	-25.8 @ .1MHz	-4 to -19	-3.7	NA
power(mW)	9.36	9.24	14.4	8.04	9.9	10(mixer + TIA)	20.25	2.4 to 18	5.9	5.6-9.6
Bandwidth(GHz)	1 to 5.5	.5 to 5.1	1 to 10.5	900M, 1.8-2.5G	.7 to 2.3	1.55 to 2.3	.7 to 2.5	2 to 10	1 to 12	.7 to 2.3
CMOS Technology	65nm	65nm	65nm	65nm	180nm	180nm	130nm	130nm	130nm	180nm
Power supply	1.2V	1.2V	1.2	1.2	1.8	2	1.5	1.2	1.2	1.8

Fig. 9. Simulated noise figure and conversion gain vs IF frequency.

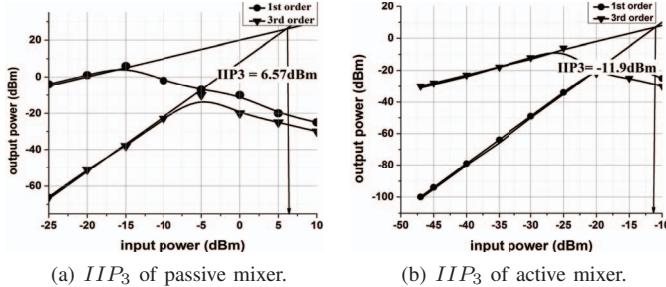(a) IIP_3 of passive mixer. (b) IIP_3 of active mixer.

Fig. 10. Simulated linearity of reconfigurable mixer

The two tone linearity test result is shown in Fig. 10(a) for 2.4GHz LO frequency. Due to high conversion gain at low IF, the output compression point of the OPAMP, limits the input referred linearity of the circuit. 1dB-compression point of the circuit is limited by the output swing and varies with IF frequency. The simulated IIP_3 in case of passive is 6.57dBm and IIP_3 of active is shown in Fig. 10(b). IIP_3 of active is -11.9dBm.

IV. CONCLUSION

In this paper, a wide band Reconfigurable mixer is simulated in 65nm technology. A new concept of reconfiguration between Active / passive downconversion mixer is presented. This is an important design guideline (both topology in single circuitry) for modern baseline deep sub-micron CMOS processes. Wide band mixer comsumes 9.24mW and 9.36mW in passive and active case repectively. Reconfigurable mixer is simulated in the frequency range .5GHz to 7GHz. IIP_2 is > 65 for both cases. The analytical results shows close to simulted results. With the exception of few very stringent standard, the architechture is suitable for both cases.

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