Energy aware ultra-low power SAR ADC in 180nm CMOS for biomedical application

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ABSTRACT

Power consumption is one of the main design constraints in today's integrated circuits. For systems powered by batteries, such as implantable biomedical devices, ultra-low power consumption is paramount. In these systems, analog-to-digital converters (ADCs) are key components as the interface between the analog world and the digital domain. This thesis addresses the design challenges, strategies, as well as circuit techniques of ultra-low-power ADCs for medical implant devices.

In this thesis four architectures of SAR ADC is implemented with different energy efficiency. In first architecture, conventional SAR ADC was designed in 180nm CMOS technology with a 1-V power supply and a 1-kS/s sampling rate for monitoring bio potential signals, the ADC achieves a signal-to-noise and distortion ratio of 57.16 dB and consumes 43 nW power, resulting in a figure of merit of 73 fJ/conversion-step. In second architecture, Split capacitor SAR ADC was designed in 180nm CMOS with same resolution and sampling speed. ADC achieves a signal-to-noise and distortion ratio of 54.88 dB and consuming 14.71nW power with a substantial (37%) improvement in power consumption. In third architecture, monotonic SAR ADC was designed in 180nm CMOS with same resolution and sampling speed with 81% improvement in switching energy. In fourth architecture, signal adaptive ADC is designed in which the reference is scaled according to input signal level, it helps to achieve better resolution. ADC achieves an SNR of 54dB working at sampling speed of 1KS/s.

Nomenclature

ADC	Analog to Digital Converter
BWC	Binary-Weighted Capacitor
CMOS	Complementary Metal-Oxide Semiconductor
DAC	Digital to Analog Converter
DFF	D Flip Flop
DFT	Discrete Fourier Transform
DNL	Differential Non Linearity
DSP	Digital Signal Processing
ENOB	Effective Number of Bits
FFT	Fast Fourier Transform
FOM	Figure of Merit
IC	Integrated Chip
INL	Integral Non Linearity
LSB	Least Significant Bit
MSB	Most Significant Bit
NMOS	N Type CMOS Transistor
PMOS	P Type CMOS Transistor
RMS	Root Mean Square
SAR	Successive Approximation Register
SFDR	Spurious-Free Dynamic Range
SINAD	Signal to Noise and Distortion Ratio
SNR	Signal to Noise Ratio
S/H	Sample and Hold
TWC	Two-Stage Weighted Capacitor

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Chapter 1

INTRODUCTION

1.1 Motivation

In the last Decade, there has been a growing demand for the design of wireless sensing device for biomedical applications. These devices are utilized for monitoring and recording bio-potential signals such as electrocardiogram (ECG), electroencephalography (EEG), and electromyography (EMG), to name a few.

Wearable monitoring systems provide tremendous benefits but they have many design challenges e.g. low power consumption, self-sustainability, light weight, affordability. Most crucial among previously mentioned issues are low power and self-sustainability. A typical biomedical wearable sensor consists of AFE, ADC and power module as shown in fig 1. To make the system self-sustainable an energy harvesting module has to be incorporated. For example [1][2] presents an ECG acquisition and processing system on chip (SoC) with energy harvesting module to make it self-sustainable. Although the above system fulfils the processing requirement but it suffers from a major drawback of high AFE power consumption (4.8µW) [1] which leads to fast drainage of battery.

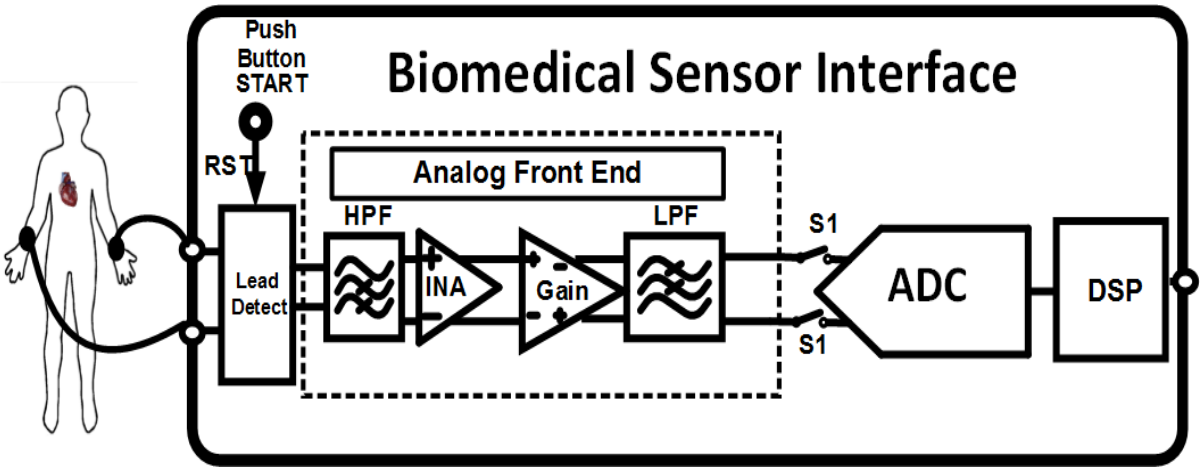


Figure 1. Bio-medical sensor interface

A detailed system level architecture of ECG acquisition unit is shown in fig 2. It consist of AFE which includes Instrumentation amplifier followed by two PGA, a mixed signal AGC and a 10 bit SAR ADC. The system is powered by RF energy harvesting circuit. The AFE combined with ADC consumes a total power of 343nW [3].

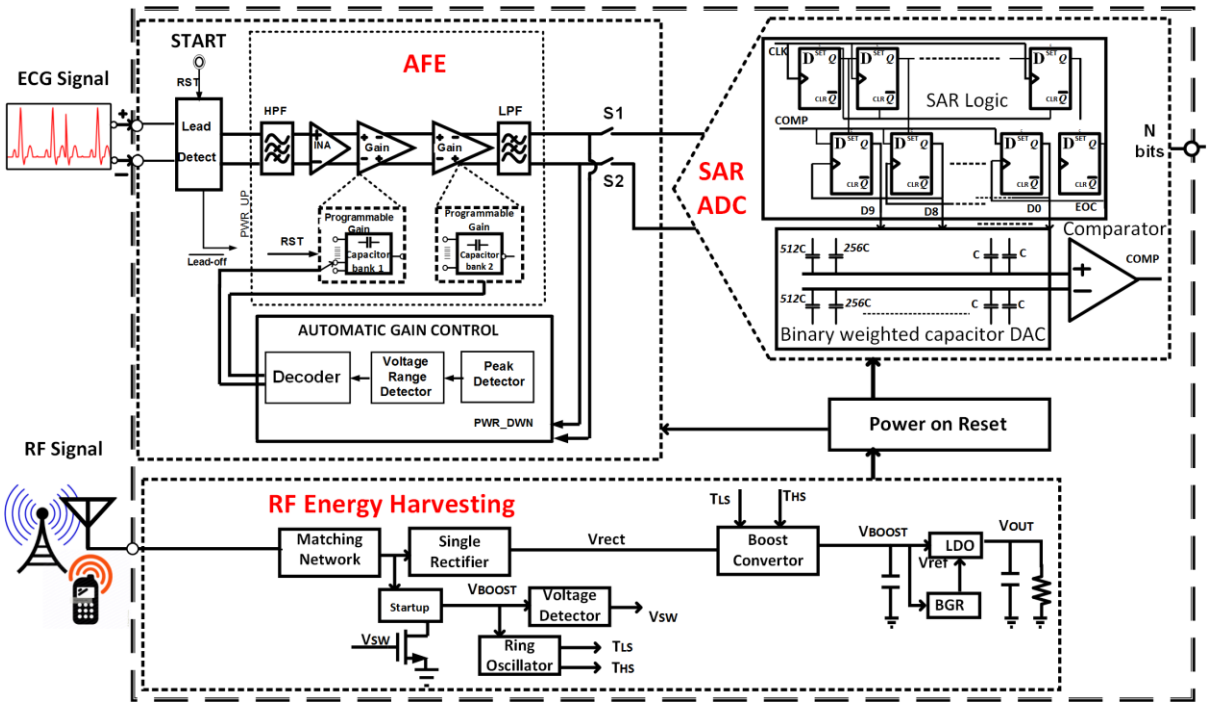


Figure 2 Full system Architecture

1.2 ADC Architecture Overview

There are many different architecture of ADC's proposed depending upon the applications it is going to be used. ADC's can be broadly classified as follows

- Flash ADC
- SAR ADC
- Sigma-delta ADC
- Pipeline ADC
- Folding ADC

Figure 1-1 shows the resolution and sampling frequency for all ADCs published in key technical conferences in this field (ISSCC and VLSI) between 1997 and 2016 [1]. The plot shows the trend that increasing sampling frequency goes with decreasing resolution. Of the classical architectures, ΣΔ converters dominate the high resolution and low sampling frequency region, flash and folding ADCs have the highest sampling frequency but with the lowest resolution, successive-approximation-register (SAR) converters are used for low-to-medium speed and medium-to-high resolution applications, and pipelined converters are used for applications that require medium-to-high speed and resolution.

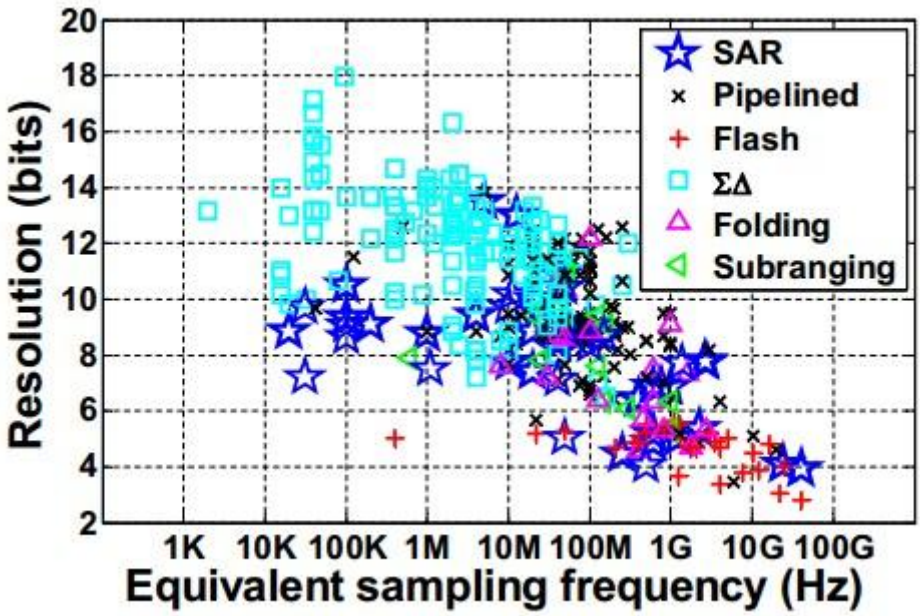


Figure 3. A plot of the resolution versus the input sampling frequency for recent published analog-to-digital converters in ISSCC and VLSI (data adopted from [1]).

The flash topology as shown in Fig 4, along with its folding and interpolating variants, has been the choice for high speed and low-resolution applications. It is able to achieve the highest throughput, but it suffers from a number of drawbacks due to its high level parallelism. Since the number of comparators grows exponentially with the resolution, these ADCs require excessive power and area for resolutions above 8 bits. The large number of comparators also gives rise to other problems such as large input loading and kickback noise. Large input loading limits the speed of the ADCs, and kickback noise can affect the accuracy of references or the analog input. The ensuing difficulty motivates the use of other ADC architectures.

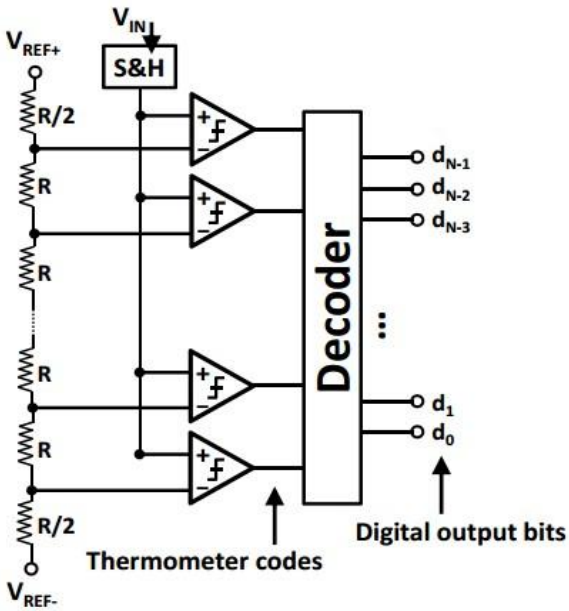


Figure 4 Flash ADC

Sigma-delta converters as shown in Fig 5 are traditionally used for high resolution, low bandwidth digital audio applications. Bandwidth is typically in the kilohertz range and resolution can be as high as 18 bits. Sigma-delta converters trade off speed for resolution, and sample the input many times faster than the Nyquist rate in order to perform noise shaping. Because the internal circuits have to run at speed much faster than the sampling rate, the power consumption can be significantly higher compared to Nyquist rate ADCs.

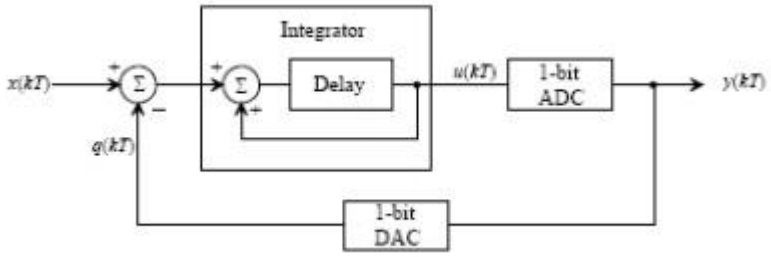


Figure 5 Sigma delta ADC

Pipelined ADCs as shown in Fig 6 are traditionally used for medium-to-high speed and resolution applications. One advantage of pipelined ADCs is that the hardware requirement scales linearly with the number of bits. By adding another pipelined stage, we can potentially increase the resolution of the overall pipelined ADC by the resolution of that extra stage. The parallelism enables high throughput at the cost of extra power consumption and latency. For example, a six-stage pipelined ADC would have a latency of at least six clock cycles between the analog input and the digital output.

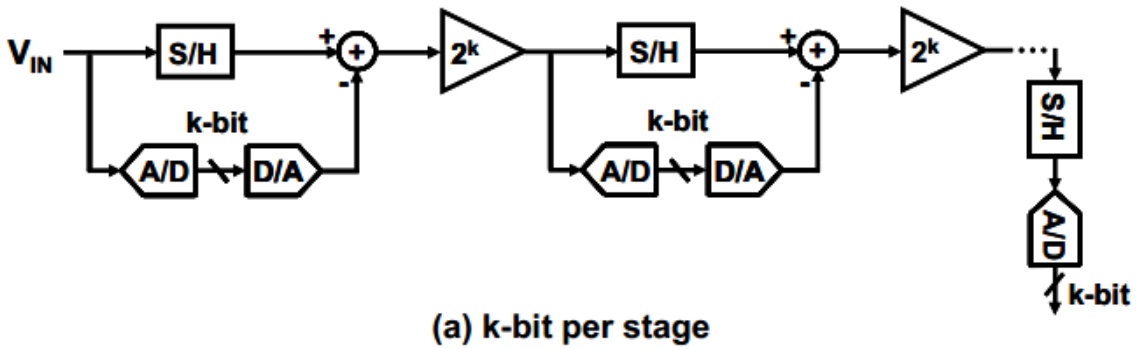


Figure 6 K-bit per stage Pipeline ADC

1.3 Review of SAR ADC for biomedical application

Most of the bio-potential signals are in low frequency range and exhibit limited dynamic range as shown in fig 7. SAR ADC is more preferable in comparison to other ADC architectures which is evident if we go through recent publication, there we can observe that that a lot work is published in various journals and conference regarding implantable biomedical devices with SAR ADC as preferred data converter because of its low power footprint [5].Conversion of the low-frequency analog signals does not need high speed, but requires ultra-low-power operation (e.g., in nW range). Trading speed for lower power at such slow sampling rates is not a straightforward task. The major challenge is how to efficiently reduce the unnecessary speed and bandwidth for ultra-low-power operation using inherently fast devices in advanced CMOS technologies. Moreover, the leakage currents contribute to a significant portion of the total power consumption [6].

Various energy efficient switching schemes like merged capacitor and inverted merged capacitor has been published in recent years [7-10]. Although these methods lower the switching energy, they make the SAR logic much more complicated due to increase number of capacitor and switches, yielding high digital power consumption.

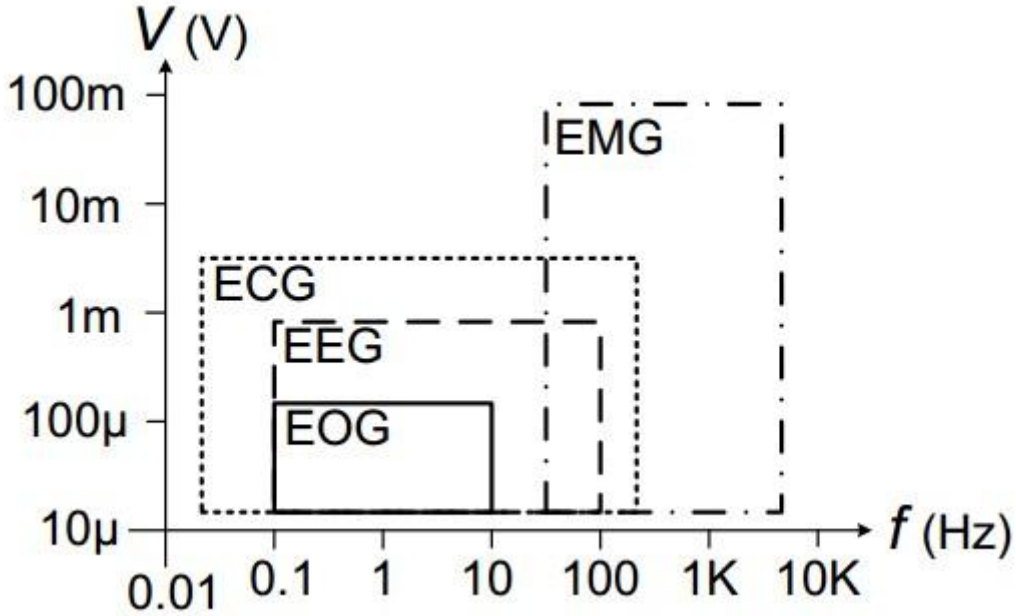


Figure 7 Voltage and frequency ranges of four classes of bioelectric signals, where EOG, EEG, ECG and EMG refer to the electrooculogram, the electroencephalogram, the electrocardiogram, and the electromyogram, respectively [11].

Chapter 2

Successive Approximation Register ADC

This chapter presents a literature review of SAR ADC. First, successive approximation algorithm is explained and different architectures of SAR ADC are investigated. In the following, the operations of the sub-modules of the SAR ADC are described.

2.1 Successive Approximation Algorithm

The algorithm used in the successive approximation (initially called feedback subtraction) ADC conversion process can be traced back to the 1500s relating to the solution of a certain mathematical puzzle regarding the determination of an unknown weight by a minimal sequence of weighing operations. In this problem, as stated, the objective is to determine the least number of weights which would serve to weigh an integral number of pounds from 1 lb to 40 lb using a balance scale. One solution put forth by the mathematician Tartaglia in 1556, was to use the series of weights 1 lb, 2 lb, 4 lb, 8 lb, 16 lb, and 32 lb. The proposed weighing algorithm is the same as used in modern successive approximation ADCs. The algorithm is shown in Fig 8 where the unknown weight is 45 lbs. The balance scale analogy is used to demonstrate the algorithm [12].

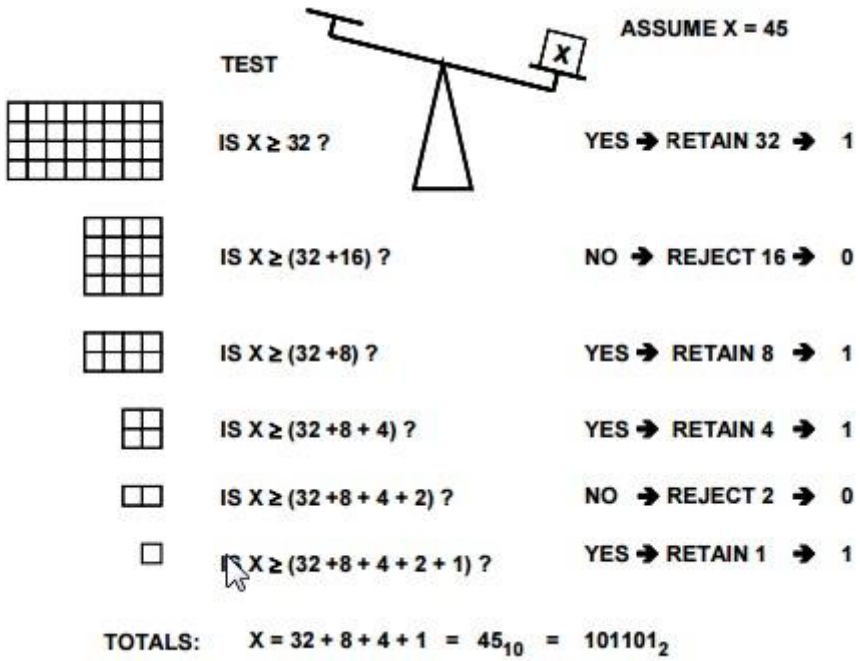


Figure 8 Successive Approximation ADC Algorithm

SAR ADC uses the same binary search algorithm to determine the digital output of the corresponding analog input as shown in fig 9. Binary search resolves the output one bit at a time. It generates the first bit by comparing the input to the mid-full-scale-level of the current search range. Depending on the comparison outcome, it eliminates half of the search range and continues the same process until the entire conversion is completed. Instead of using one clock cycle per conversion, it requires N clock cycles and thus, N comparisons to complete a conversion.

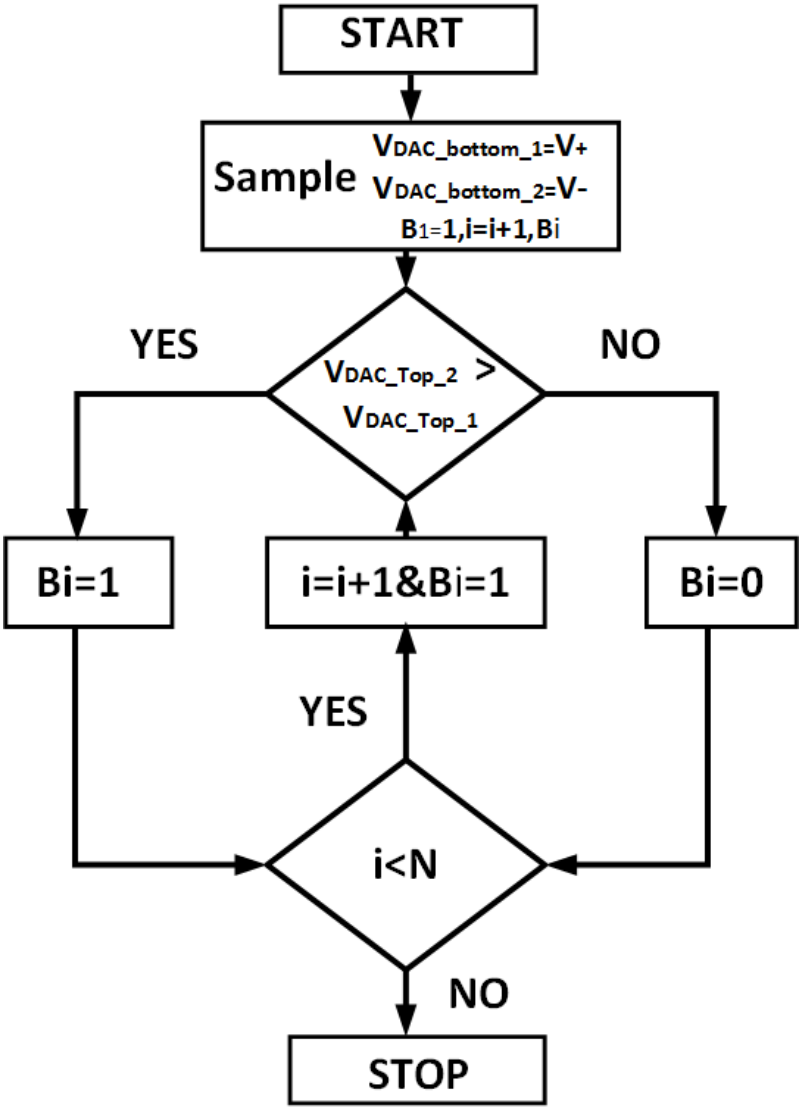


Figure 9 Flowchart of SAR algorithm

Figure 10 shows an example of a 5-bit quantization of input 6.2 using binary successive approximation search. The solid black lines represent the mid decision level of the current search range and the solid red line indicates the location of the input level. In the beginning of the process, the search range is from 0 to 31. During the first comparison, VIN (equal to 6.2) is compared with the mid-full-scale level of the initial search range. Since 6.2 is less than 16, the ADC outputs a ’0’ and the search range becomes the lower half of the previous search range. The search process continues for a total of five clock cycles

to produce the final binary output equal to 00110. The last search reduces the range of uncertainty to one LSB, resulting in quantization error within ±0.5LSB.

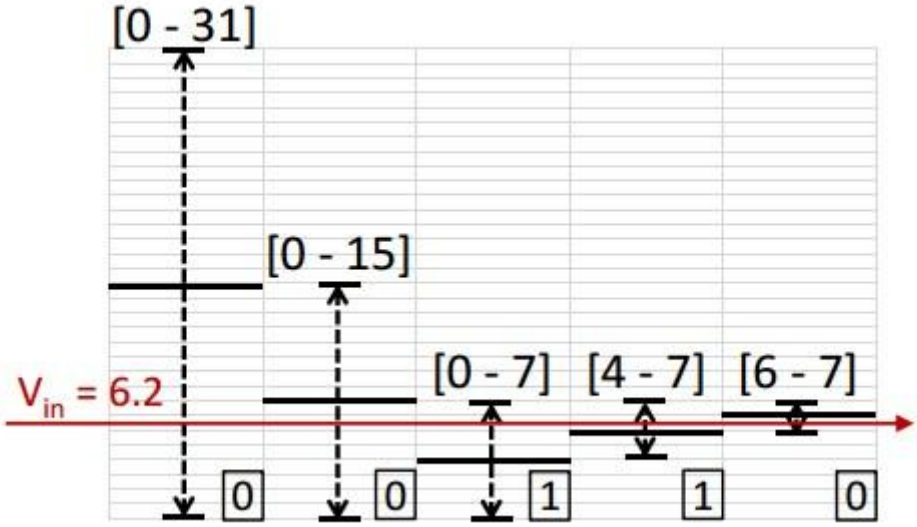


Figure 10 A example of 5-bit quantization using a binary search algorithm [9].

2.2 The SAR Architecture

SAR ADC executes the conversion in multiple clock cycles using the information of the previous determined bit. Fig 11 illustrate the basic block diagram of SAR ADC. It consist of four basic building blocks: sample and hold (S&H), comparator, DAC and SAR logic. The S&H samples one instance of the continuous analog input signal during the first clock period and holds the value for the remaining conversion process. The comparator resolves each bit by comparing V_{Hold} *with* V_{DAC}. The SAR control reconfigures and updates the DAC according to the output bits of the comparator.

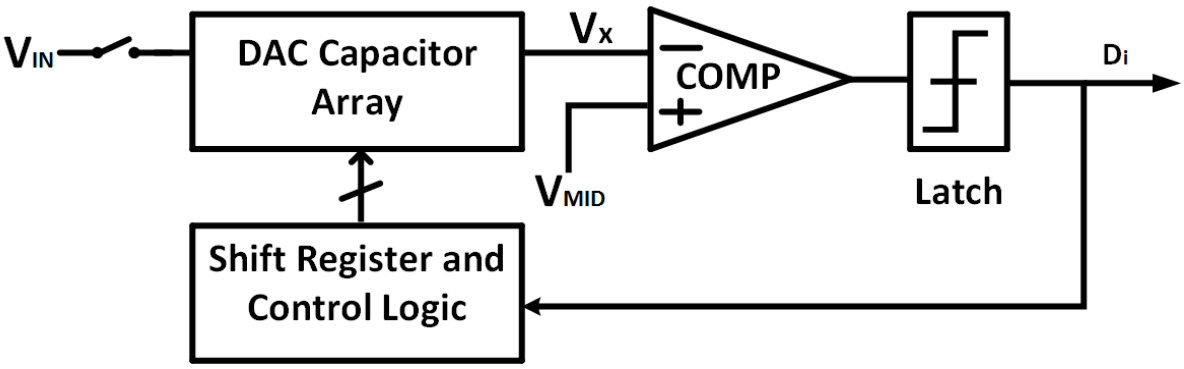


Figure 11 Block diagram of SAR ADC

The DAC for the SAR ADC can be implemented in many ways (R-2R, capacitive, current steering, hybrid of R-C). For the realization of a fast, successive-approximation A/D converter in MOS technology, conventional voltage driven R-2R techniques are cumbersome since diffused resistors of proper sheet resistance are not available in the standard single channel technology. A complex thin-fdm process must be used. Furthermore, these approaches require careful control of the "ON" resistance ratios in the MOS switches over a wide range of values [13].

An effective way of implementation the DAC is charge redistribution or capacitor array scheme. It merges the sample/hold function together with the capacitive DAC to perform subtractions in the charge domain using capacitors. Compared to the conventional voltage driven R-2R techniques, the capacitor arrays are more easily fabricated with less mismatch errors and save more power based on charge-redistribution techniques.

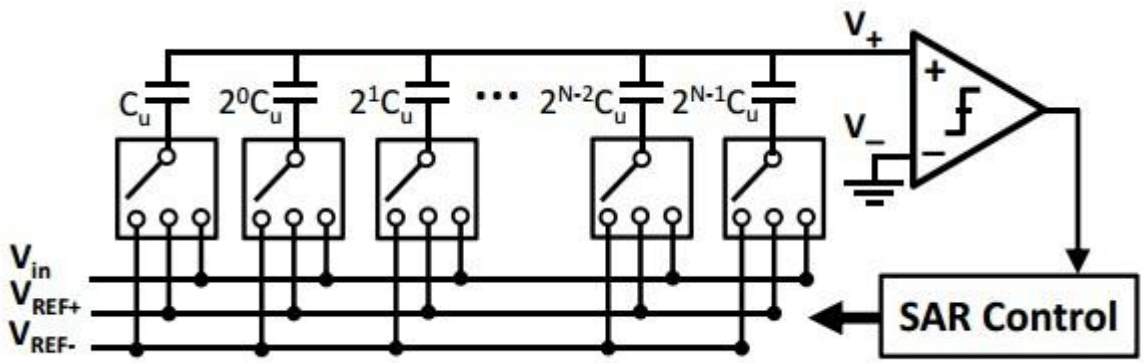


Figure 12 .Schematics of the charge redistribution SAR implementation

The conventional single ended SAR consists of an N-bit binary-weighted capacitive DAC, a comparator and a SAR control logic block. Each capacitor within the DAC can be re-configured to connect to either the input or the positive/negative reference voltages. The total capacitance sums up to C_{Tot}, where

$$C_{Tot} = \sum_{i}^{N-1} 2^{i}.C_{u} + C_{u} = 2^{N}.\ C_{u} \qquad (2.1)$$

During the sample and hold phase, the DAC array samples the input signal by connecting the bottom plates of the array to the input and the top plate of the array to ground (Fig 13(a)). The total charge stored in the array is

$$Q_{Tot} = (0-V_{in}).C_{Tot} = -V_{in}.C_{Tot} \qquad (2.2)$$

After the sampling phase, we enter the conversion phase. During the first step, we connect the most-significant-bit (MSB) capacitor to V_{REF} + and the remaining capacitors to V_{REF} − as shown in Fig 13

(b). For simplicity, in our example, we assume $V_{REF}+ = V_{REF}$ and $V_{REF} - = 0$. Using the superposition principle, the voltage on the top plate of the array, V+, becomes.

$$V_{+} = -V_{in} + \frac{2^{N-1}.C_u}{C_{Tot}}.V_{REF} = -V_{in} + \frac{1}{2}V_{REF} \tag{2.3}$$

The first term represents the contribution of input sampling and the second term represents the contribution from the MSB capacitor. By comparing V+ directly to ground, we can determine the first output bit d_{N-1} and set the configuration for the next bit calculation. If $d_{N-1} = 1$, $2^{N-1}C_u$ stays connected with V_{REF}; if = $d_{N-1} = 0$, $2^{N-1}C_u$ is switched to ground for the remaining cycles. In both cases, $2^{N-2}C_u$ is switched to V_{REF}. The two different configurations can be shown in Fig 13(c) and Fig 13(d), respectively. The top plate voltages of the two configurations become Equations 2.4 and 2.5. The process of comparing and reconfiguring continues until we reach the last bit.

$$V_{+} = -V_{in} + \frac{(2^{N-1} + 2^{N-2})C_u}{C_{Tot}}.V_{REF} = -V_{in} + \frac{3}{4}V_{REF} \tag{2.4}$$

$$V_{+} = -V_{in} + \frac{(2^{N-2})C_u}{C_{Tot}}.V_{REF} = -V_{in} + \frac{1}{4}V_{REF} \tag{2.5}$$

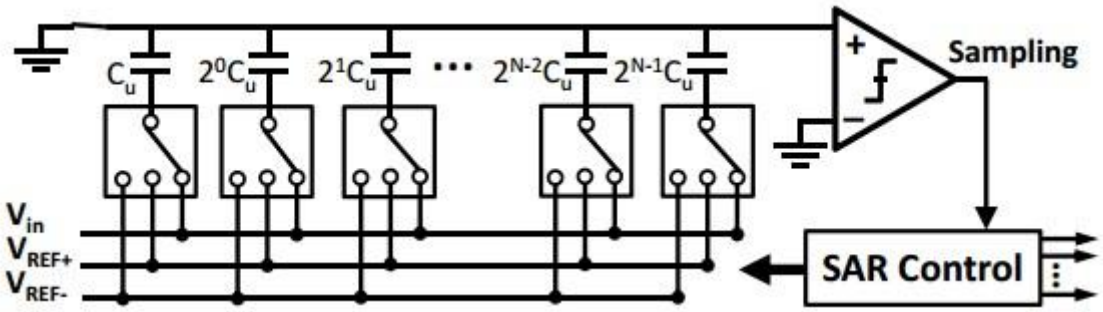
At the end of the conversion, the ADC converts the input into binary-weighted bit sequences, [d_{N-1}, d_{N-2}, ... d_0], and the final voltage on V_+ is

$$V_{+} = -V_{in} + \sum_{i=0}^{N-1} 2d_i.\frac{2^i C_u}{C_{Tot}}.V_{REF} - \frac{C_u}{C_{Tot}}.V_{REF} \tag{2.6}$$

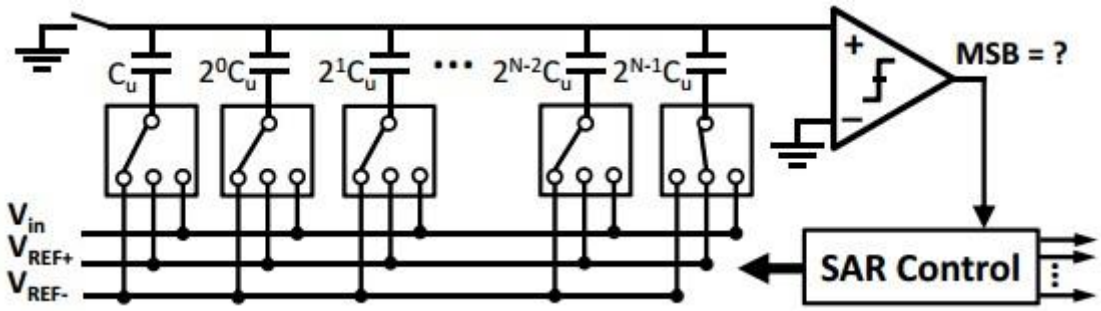
This voltage represents the quantization error of the entire conversion process. Note that both the top and bottom plates of the DAC can have parasitic capacitances contributed from non-ideal layout/wiring, channel capacitances of MOS switches and gate capacitance of comparators. The parasitic capacitances on the bottom plate are driven by low impedance reference supplies, $V_{REF}+$ and $V_{REF}-$. Typically, these do not affect the conversion process as long as the reference voltages are completely settled. The parasitic capacitance on the top plate, on the other hand, attenuates the amplitude of sampled input. The attenuation factor can be calculated as

$$\beta = \frac{C_{Tot}}{C_{Tot} + C_P} \tag{2.7}$$

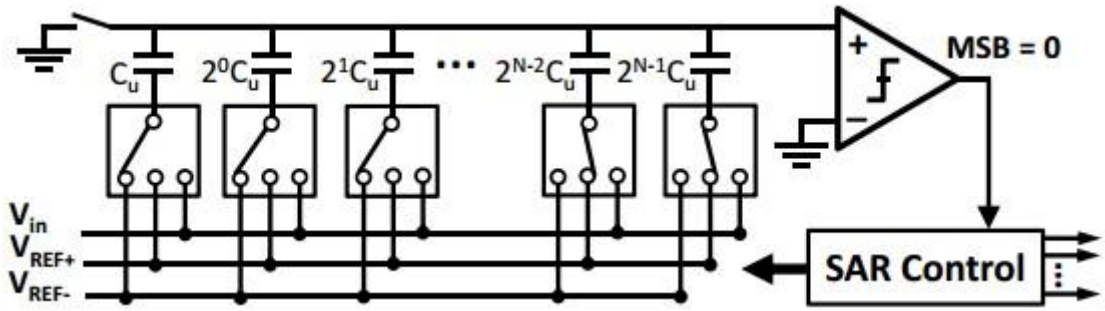
Where $C_P$is the total parasitic capacitance on the top plate. This attenuation reduces the effective signal power, but does not change the polarity of the comparison result, which is the only relevant information for determining the correct output bits. The bottom-plate sampling essentially enables this feature. In the sampling phase, the top plate is pre-charged to ground before the node becomes floating and remains floating until the end of the conversion phase. During the conversion, the voltage on the top plate moves but returns to a voltage that is near zero at the end of the process. As a result, the total charge on C_P is the same at the beginning and at the end of the process and therefore, from the perspective of charge, capacitor C_P does not cause any charge error. Therefore, it does not affect the overall accuracy of the conversion process [9].



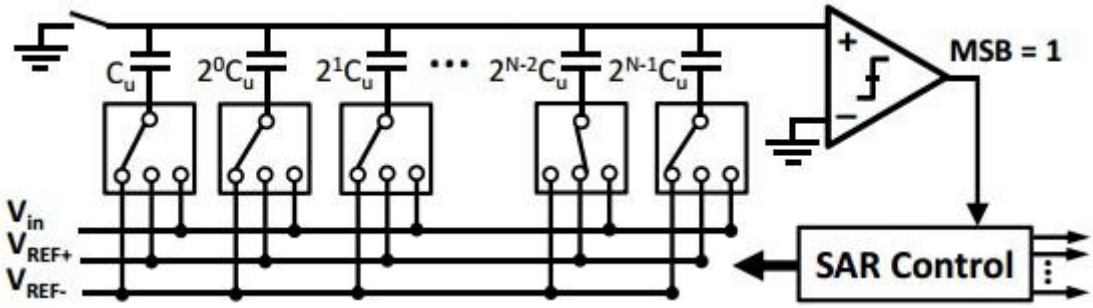
(a) Sample and hold phase.



(b) Conversion phase, step 1.



(c) Conversion phase, step 2a.



(d) Conversion phase, step 2b.

Figure 13 Switching scheme of a conventional SAR ADC.

2.3 Fully Differential vs. Single Ended

From the input signal point-of-view, an ADC can be either a single ended signal or a fully differential signal. A fully differential analog signal path has been chosen due to several advantages with respect to the single ended one.

In single-ended all signals are referred to the common ground. The dynamic range is subjected to DC offset and noise through the signal path that can decrease it. In fully differential, the two differential inputs are 180º out of phase, the difference in voltage between these two signals is considered. In this way the dynamic range is doubled with respect to the single ended signal, and a maximum noise rejection is achieved. Doubling the dynamic range leads to a V_{LSB} doubled, that leads to more relaxed constraints for the design of the comparator. The differential architecture allows a good dynamic common mode rejection. Moreover fully differential topology can reduce the effects of charge injection caused by parasitic capacitances, hence the precision improves.

Chapter 3

A 43-nW 10-bit 1-kS/s SAR ADC in 180nm CMOS for Biomedical applications

This Chapter presents an ultra-low power 10-bit, 1-KS/s successive approximation register (SAR) analog-to-digital converter (ADC) for biomedical applications. To achieve the Nano-watt range power consumption, an ultra-low-power design technique has been utilized, inflicting maximum simplicity on the ADC architecture & low transistor count. ADC was designed in 180nm CMOS technology with a 1-V power supply and a 1-kS/s sampling rate for monitoring bio potential signals, the ADC achieves a signal-to-noise and distortion ratio of 57.16 dB and consumes 43 nW, resulting in a figure of merit of 73fJ/conversion-step.

3.1 Circuit Implementation

Key building blocks in SAR ADC are Control Logic, Comparator and Capacitor Array. The design considerations of the building blocks are described in the following subsections.

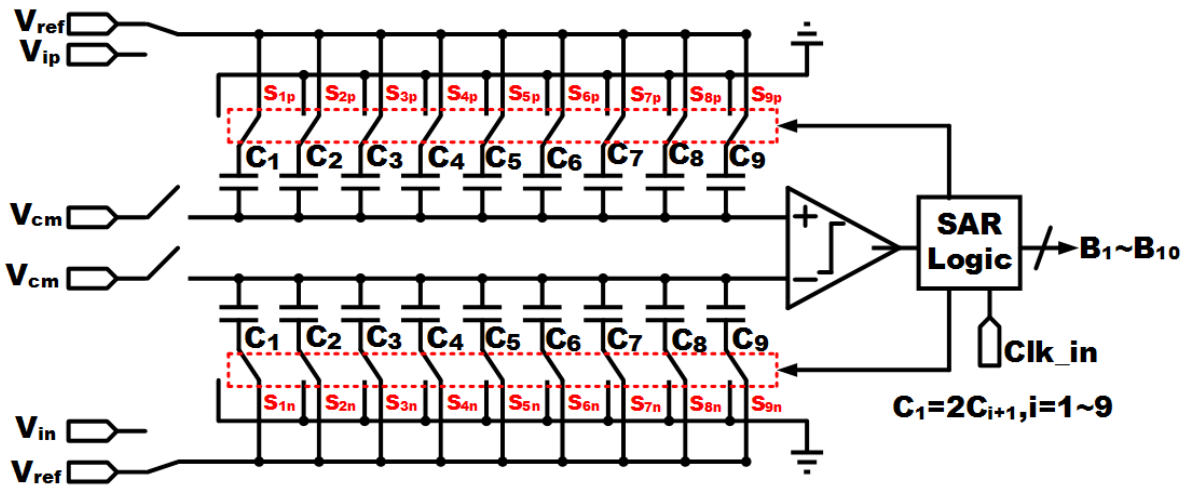


Figure 14 10 bit SAR ADC circuit diagram

3.1.1 DAC Control Logic

The proposed system architecture utilizes the synchronous SAR logic. It encompasses a ring counter and code register [14]. It generates the sample signal and the switch control signals for the DAC. Fig 15 shows the schematic and fig 16 shows the timing diagram for DAC control logic.

In the first clock cycle foremost D flip flop in ring counter is set and all other flip flops are reset. This operation provides the Sample signal. In second clock cycle MSB is set. In each clock cycle one of the output of ring counter sets the flip flop in code register. The output of the current flip flop in code register is used as a clock for the previous flip flop to register the comparator output. At the end of the conversion an EOC signal is generated to read the digital output. To reduce power dissipation transmission gate based Sets-reset D flip flop are used. In order to decrease the leakage power while maintaining the speed, high V_T (threshold) transistors are used in the noncritical paths and low *VT* transistors in the critical path. To reduce the dynamic power further current starved architecture is used in designing the logic gates.

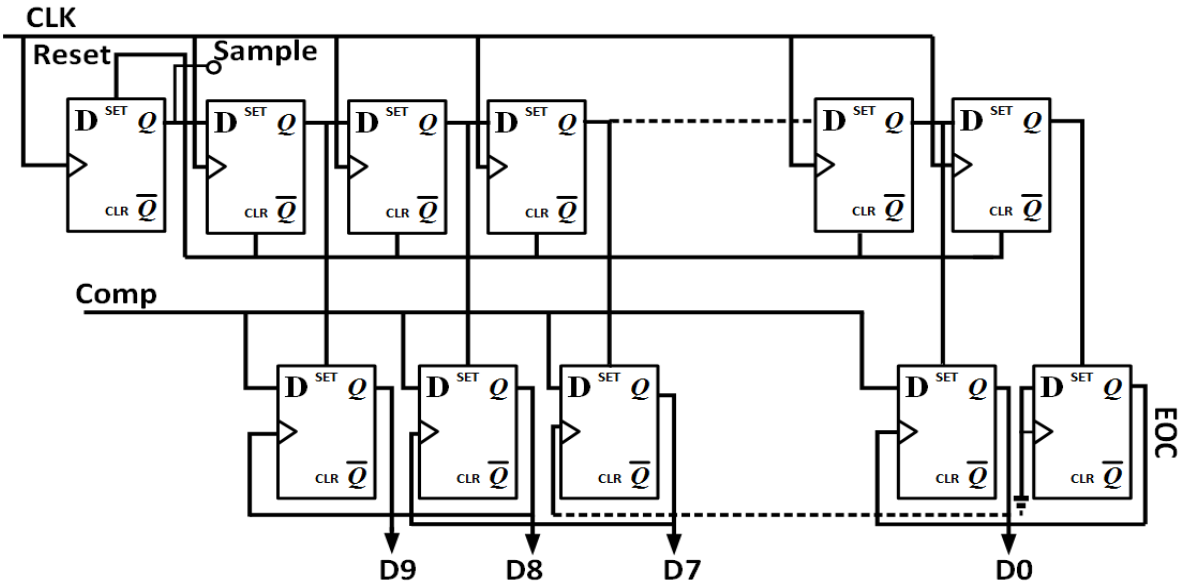


Figure 15 SAR Control Logic

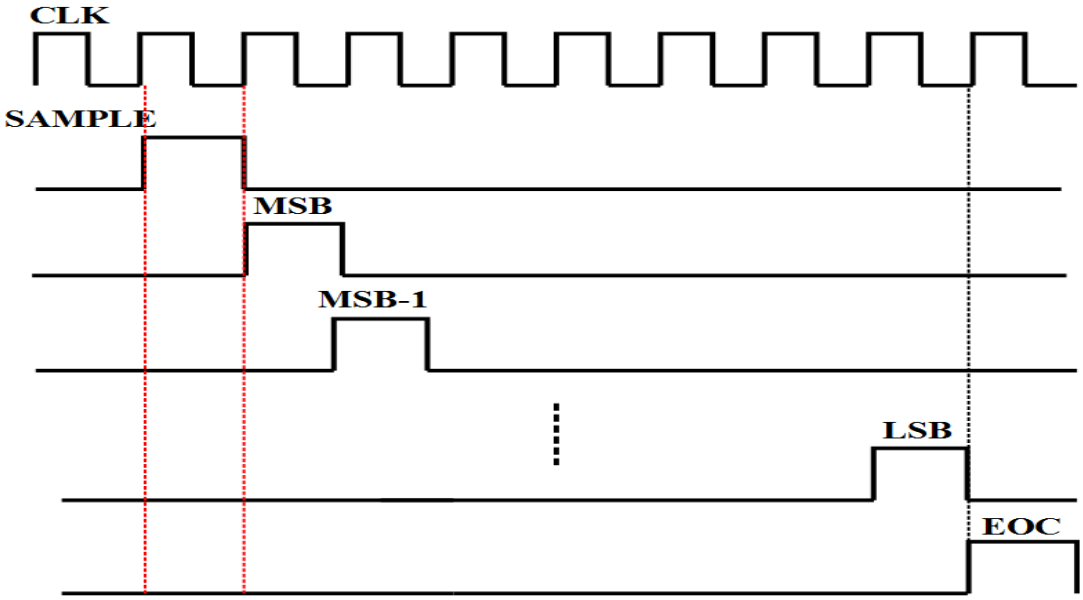


Figure 16 Timing Sequence of the synchronous SAR Control Logic

3.1.2 Comparator

Dynamic latched comparator is employed for the low power consumption. It consist of a pre amplifier circuit followed by two stage latched comparator with NAND type SR latch at the output as shown in Fig 17. The preamplifier boost the input signal and attenuates the latch offset by its gain as expressed by equation (3.1). The schematic for pre amp is shown in Fig 18

$$V_{Offset_{Tot}}{}^2 = V_{Offset_{AMP}}{}^2 + \frac{V_{Offset_{latch}}{}^2}{A_{preamp}} \tag{3.1}$$

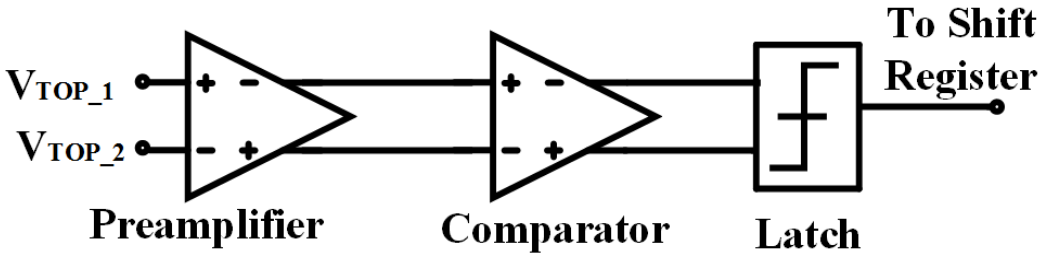


Figure 17 Comparator with single stage pre-amplifier and regenerative latch

Increasing the gain of pre-amp reduces the offset at the input, however increasing gain reduces the speed of comparator. So speed-gain trade-off exist in pre-amp design. The preamp output is fed to energy efficient two stage latched comparator [15]. First stage of the latched comparator is a voltage amplifier and second stage is a latch as shown in Fig 19. During reset phase when clock signal is low F_n and F_p nodes are raised to VDD and latch stage is turned off. When clock goes from low to high tail transistor in first stage is turned ON and the nodes F_n and F_p starts discharging depending upon the input voltage. When either node voltages F_n and F_p goes below V_{th} of second stage input transistor, amplification starts occurring and the output voltage increases and positive feedback system is activated . It evidently generates output level of high and low voltage in the regeneration phase. The output is finally latched into NAND type SR latch to be feed to shift register.

The transistors are sized to meet the prerequisites focusing on least power utilization. The transistors are of minimum size with two fold length to counter the leakage problem. For enhancing the performance in terms of offset voltage and delay, input transistors are sized three times the minimum size.

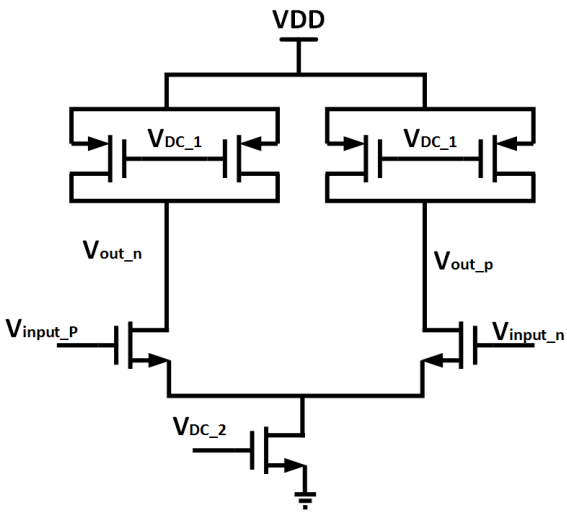


Figure 18 Preamplifier Schematic

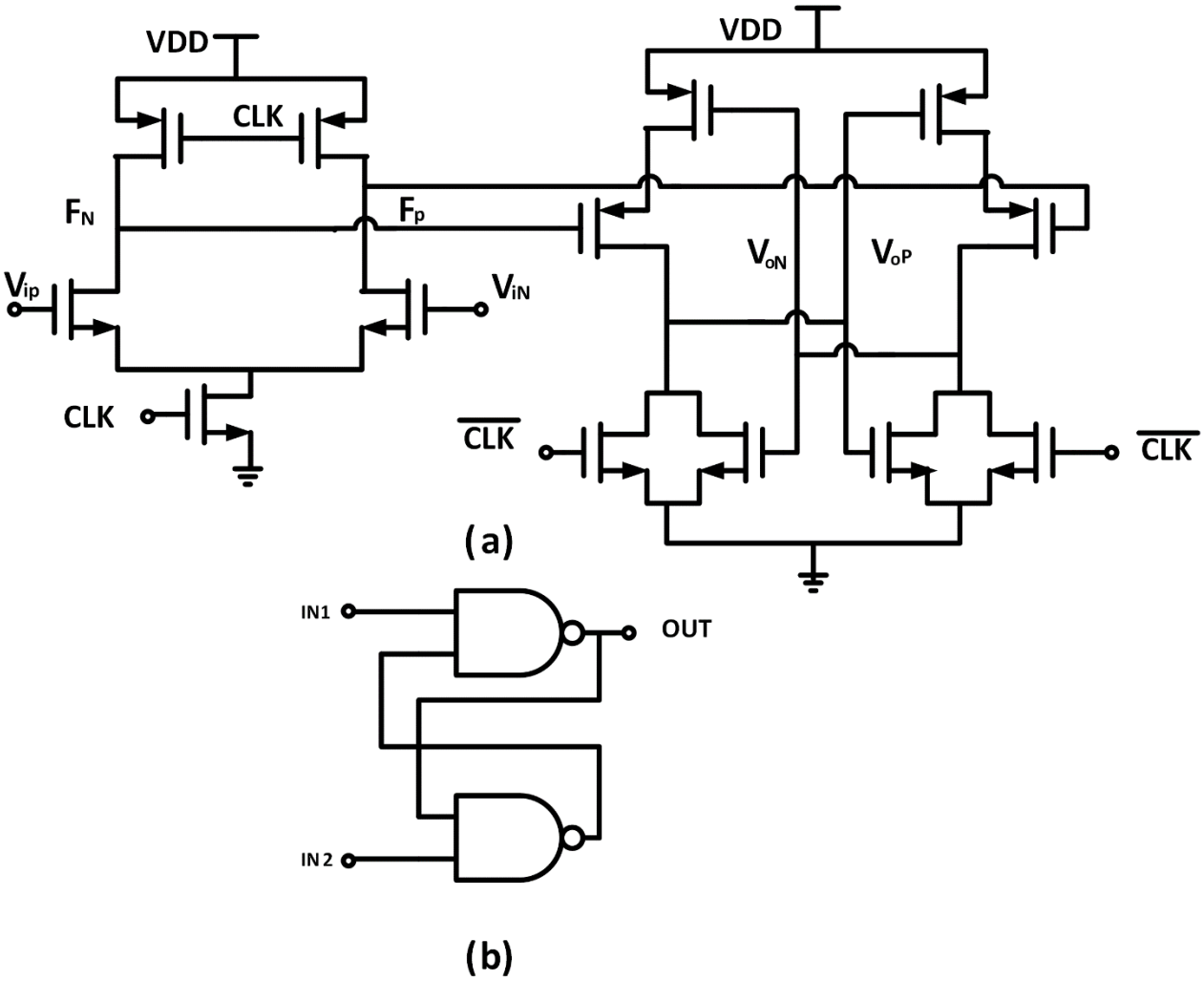


Figure 19 (a) Schematic of two stage dynamic latched comparator
(b) Regenerative latch

3.1.3 Capacitive DAC

The capacitive DAC in SAR ADC serves dual purpose, it samples the input voltage and it generates an error voltage between the input and current digital estimate. DAC is implemented using binary weighted capacitor to achieve better linearity [5]. Unit capacitor in DAC should be kept as small as possible in order to reduce power dissipation. It value is determined by KT/C noise and mismatch parameter. Aside from above limiting factor, sampling leakage is also an additional major concern because of low speed of operation. Consequently a MIM Cap of 20fF is used as a unit capacitor. The layout for the CAP DAC is shown in Fig 20

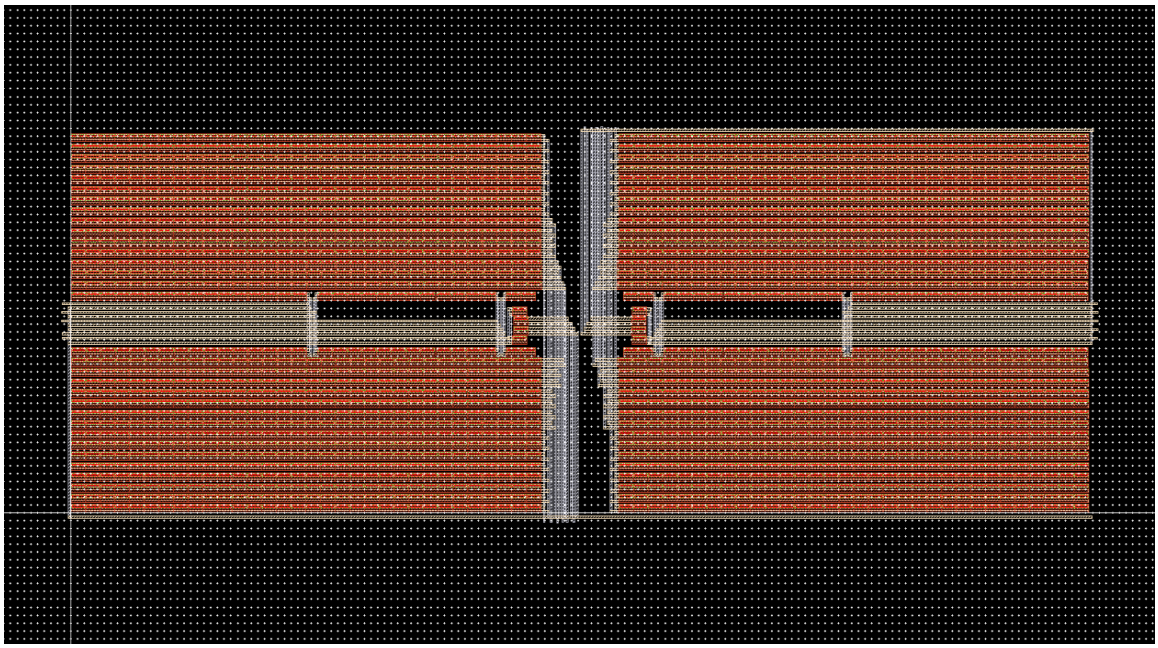


Figure 20 Capacitor DAC layout

3.1.3 Sampling Switch

A transmission gate is employed to sample the input signal on to capacitor plate. The error voltage introduced by Charge injection is relatively small because of large capacitor array. As the operational speed of ADC is relatively small (1 KS/s) smaller size NMOS and PMOS can be used to reduce parasitic and hence limiting charge injection. The ON resistance curve is shown in Fig 21

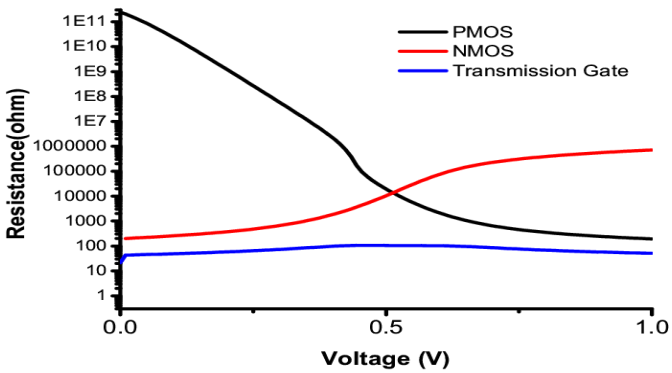


Figure 21 On-Resistance Curve of PMOS NMOS and Transmission gate

3.2 Simulation Results

The ADC has been designed in 180nm CMOS technology. Fig 22 shows the Fast Fourier transform (FFT) of the ADC with input frequency close to 25Hz. SNDR is about 57.16dB providing effective number of bit (ENOB) 9.17. The total measured power of ADC is 43nW at 1V supply power which gives the figure of merit (FOM) of 73 fJ/Conversion step. The power distribution cycle for the ADC is shown in fig 23. The possible switching procedure for 3 bit ADC with the quantitative energy dissipation of each switching phase is shown in Fig 24. Fig 25 show the top plate voltages of DAC during conversion. Table I shows performance comparison of designed ADC.

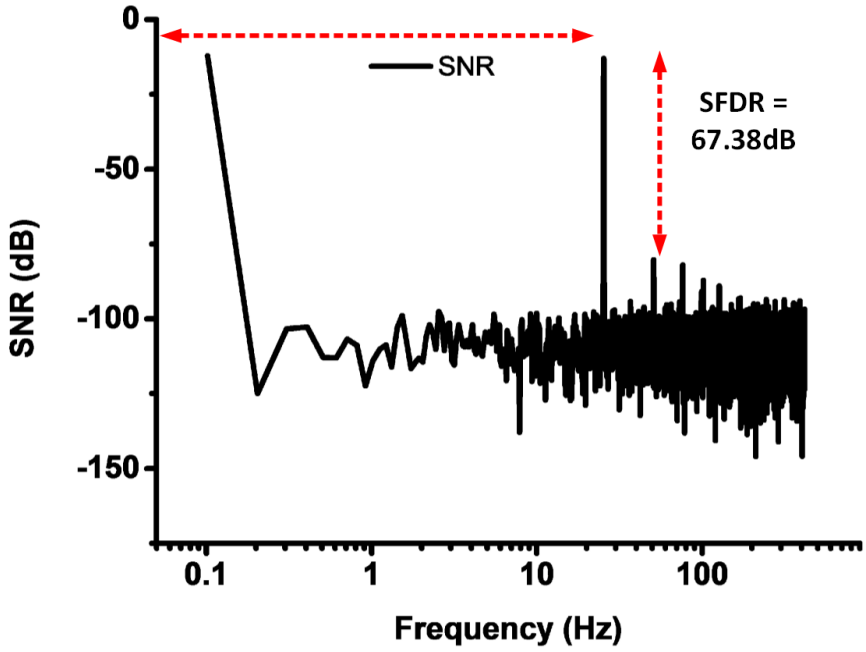


Figure 22 Power spectral Plot for SAR ADC for input at 25 Hz

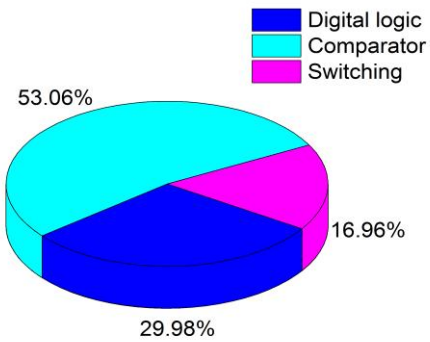


Figure 23 Power consumption circle

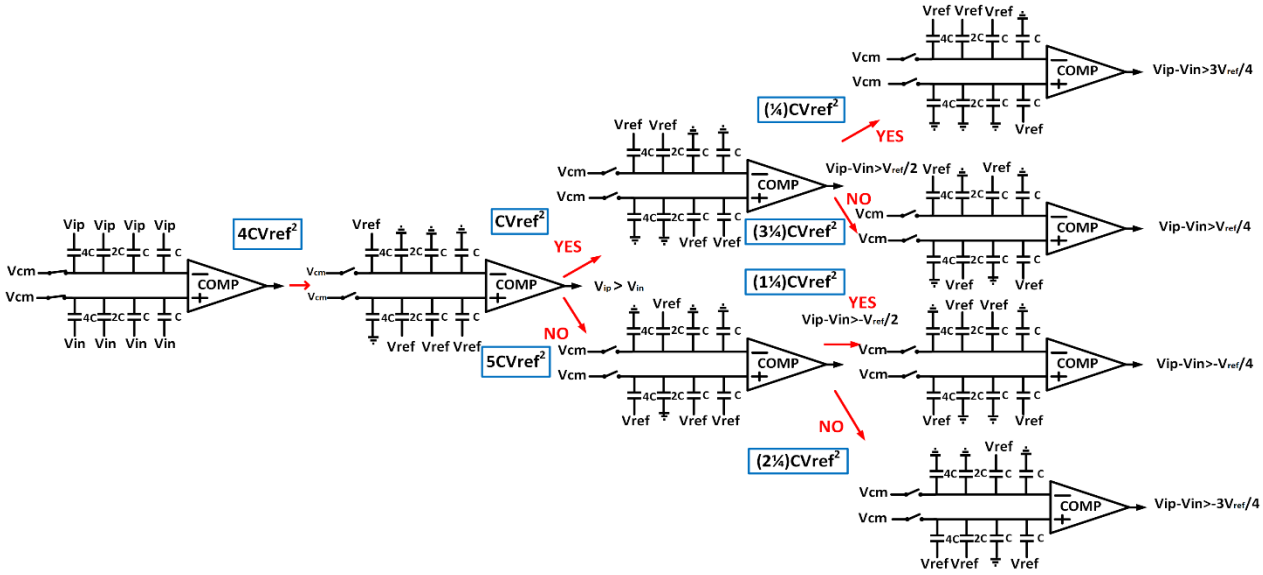


Figure 24 Switching procedure and energy dissipation in a 3 bit SAR ADC

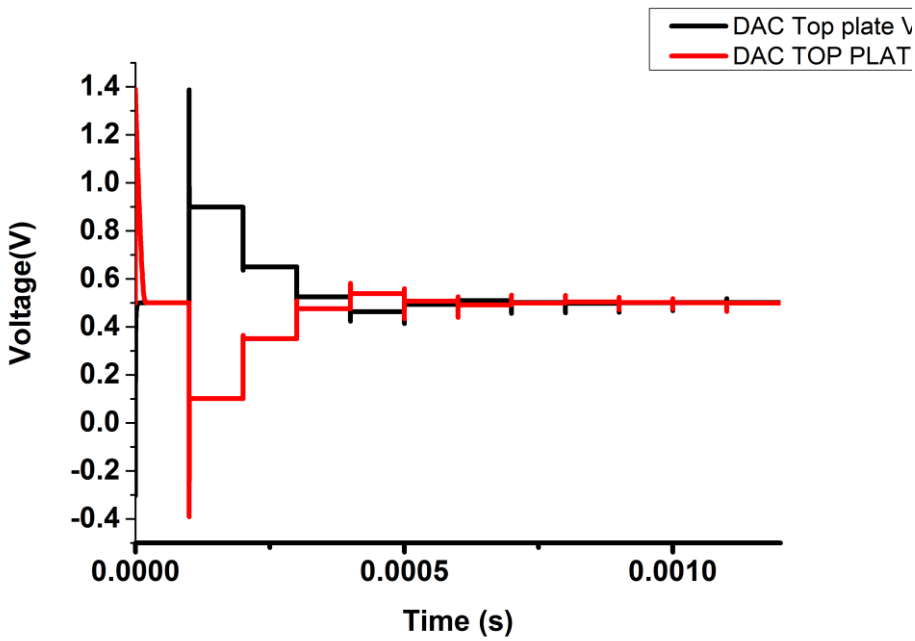


Figure 25 Waveform of Switching procedure

Parameters	This work	[5]	[16]	[17]
Technology (nm)	180	130	180	180
Sampling Rate (KS/s)	1	1	1	4.1
Power(nW)	43	53	120	850
ENOB	9.17	9.12	9.76	6.9
FOM(fJ/conv)	73	94.5	138.4	1700
SNDR(dB)	57.16	53.67	60.53	51.2

Figure 26 ADC comparison table

Chapter 4

A 14.31-nW 10-bit 1-kS/s Split-CAP SAR ADC in 180nm CMOS for Biomedical applications

This Chapter presents an ultra-low power 10-bit, 1-KS/s split capacitor successive approximation register (SAR) analog-to-digital converter (ADC) for biomedical applications. In a SAR design, the input loading and the area/layout complexity of the DAC increase exponentially with the number of bits. To avoid this a split capacitor array with fractional value bridge cap is employed. ADC was designed in 180nm CMOS technology with a 1-V power supply and a 1-kS/s sampling rate for monitoring bio potential signals, the ADC achieves a signal-to-noise and distortion ratio of 54.88 dB and consumes 14.31 nW, resulting in a figure of merit of 31.88fJ/conversion-step.

4.1 Circuit Implementation

Key building blocks in SAR ADC are Control Logic, Comparator and Capacitor Array. The design considerations of the building blocks are described in the following subsections

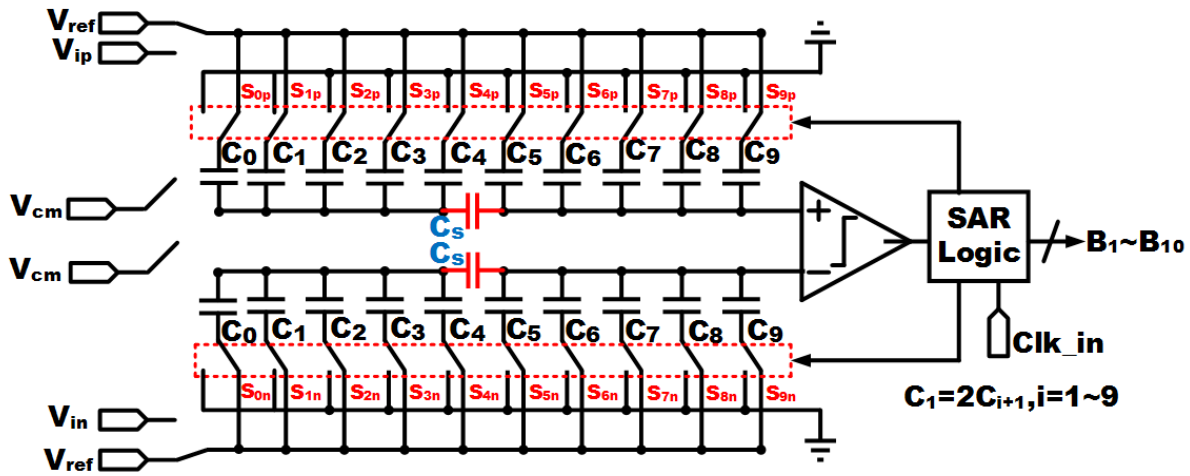


Figure 27 Schematic of Split array DAC SAR ADC.

4.1.1 Capacitive DAC

As the resolution increases the size of the MSB capacitor becomes a major concern. For example if the unit capacitor value is 0.5pF and a 16 bit DAC is designed then the MSB capacitor needed to be

$$C_{MSB} = 2^{N-1} * 0.5pF = 16.384nF$$

The area required by the MSB capacitor will be huge. One method to reduce the size of the capacitors is to use a split array. In split array DAC a bridge capacitor is used to connect two split capacitor arrays

which have the same scaling. The left array is the lower weight side (LSB-side) and the right array is the higher weight side (MSB-side). The bridge capacitor has a fractional value equal to (32/31)C which is determined by the resolution of the LSB-side capacitor array.

$$C_{atten} = \frac{Sum\ of\ \ the\ LSB\ array\ \ capacitors}{Sum\ of\ the\ MSB\ array\ capacitors} \cdot C$$

During the sampling mode, all the capacitors in the LSB-side and MSB-side arrays are connected to the analog input signal $V_{IN.}$ Switches SC1 and SC2 are connected to an ac ground (a dc bias voltage determined by the comparator input common mode voltage). The total input load capacitance is equal to 31C, which is about 8 times smaller than the binary-weighted capacitor array. The area reduction is also 8 times. However, the bridge capacitor being fractional causes poor matching with the other capacitors. Parasitic capacitance at node Q affects the charge coupling ratio of the LSB-side array and the bridge capacitor. Both above problems degrade the DAC linearity and thus the overall ADC linearity performance [18] [19].

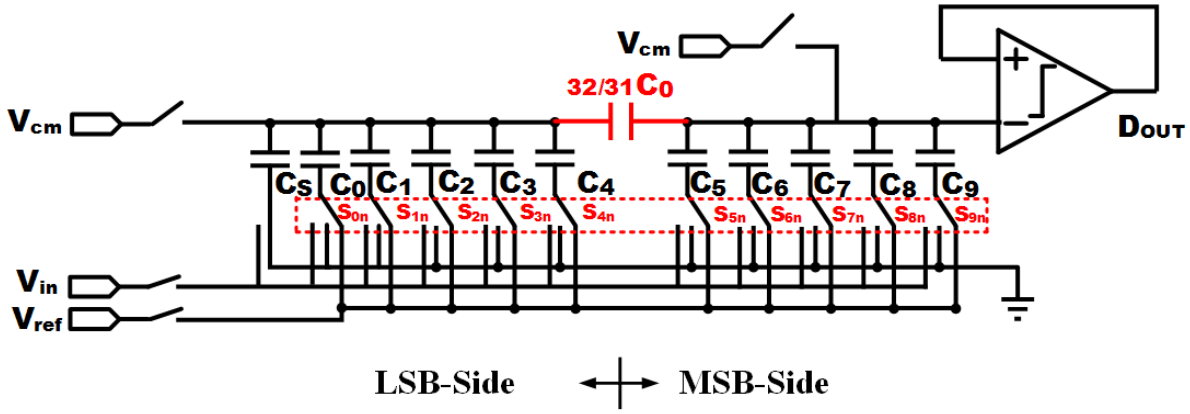


Figure 28 Split Array with Fractional Bridge Capacitor

The fractional-value bridge capacitor can be replaced with a unit capacitor in Figure 2.3. The dummy capacitor is removed from the LSB-side array so that the total weight of the LSB-side array keeps the same as the lowest bit in the MSB-side array. However, due to the lack of the dummy capacitor, 1LSB gain error occurs [18].

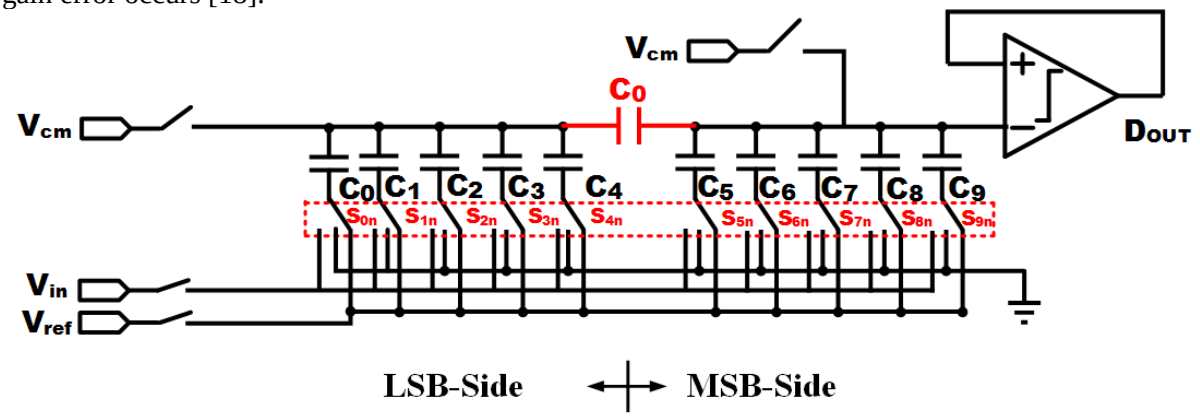


Figure 29 Split Array with Unit Bridge Capacitor

4.1.2 DAC Control Logic

The proposed system architecture utilizes the synchronous SAR logic. It encompasses a ring counter and code register as shown in Fig 24. In the first clock cycle foremost D flip flop in ring counter is set and all other flip flops are reset. This operation provides the Sample signal. In second clock cycle MSB is set. In each clock cycle one of the output of ring counter sets the flip flop in code register. The output of the current flip flop in code register is used as a clock for the previous flip flop to register the comparator output. At the end of the conversion an EOC signal is generated to read the digital output. To reduce power dissipation transmission gate based Sets-reset D flip flop are used. In order to decrease the leakage power while maintaining the speed, high VT (threshold) transistors are used in the noncritical paths and low VT transistors in the critical path. To reduce the dynamic power further current starved architecture is used in designing the logic gates [14].

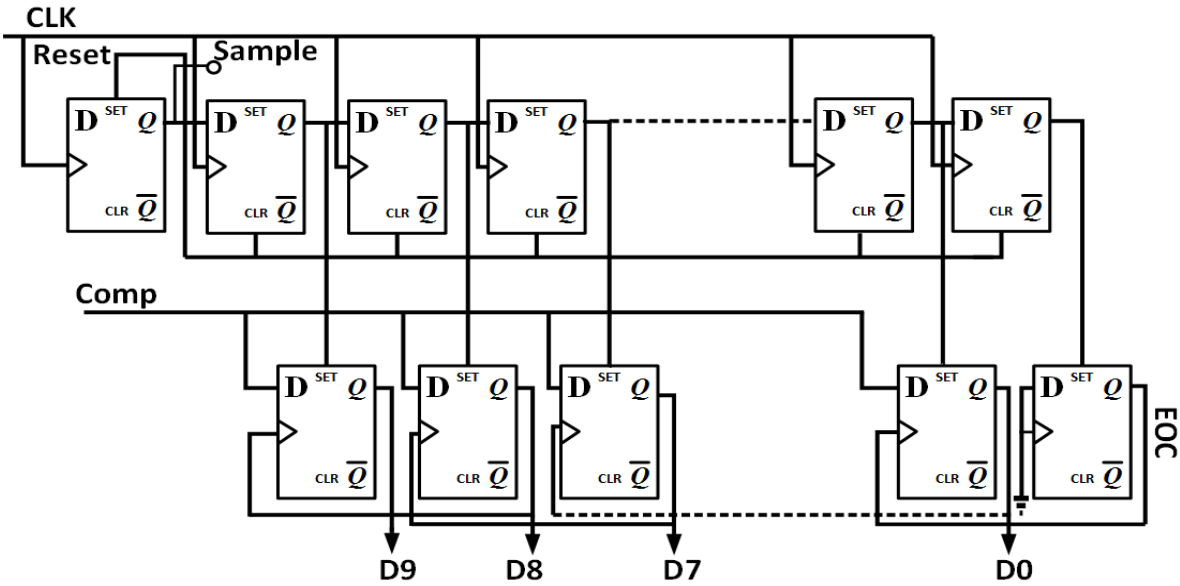


Figure 24 SAR Control Logic

4.1.2 Comparator

Dynamic two stage comparator is employed for low power consumption. The first stage is an amplifier and the second stage is a latch. During the reset phase when clock signal is low, PMOS transistors in the first stage charge F nodes to VDD and turn off the latch stage. In this phase, the output nodes are reset to zero through NMOS switches in the latch stage. This architecture is power efficient and fast due to low capacitance at F nodes which are mainly drain diffusion capacitances of NMOS and PMOS transistors connected to these nodes. When clock goes from low to high tail transistor in first stage is turned ON and the nodes F_n and F_p starts discharging depending upon the input voltage as shown in Fig 30. When either node voltages F_n and F_p goes below V_{th} of second stage input transistor,

amplification starts occurring and the output voltage increases and positive feedback system is activated . It evidently generates output level of high and low voltage in the regeneration phase. The output is finally latched into NAND type SR latch to be feed to shift register.

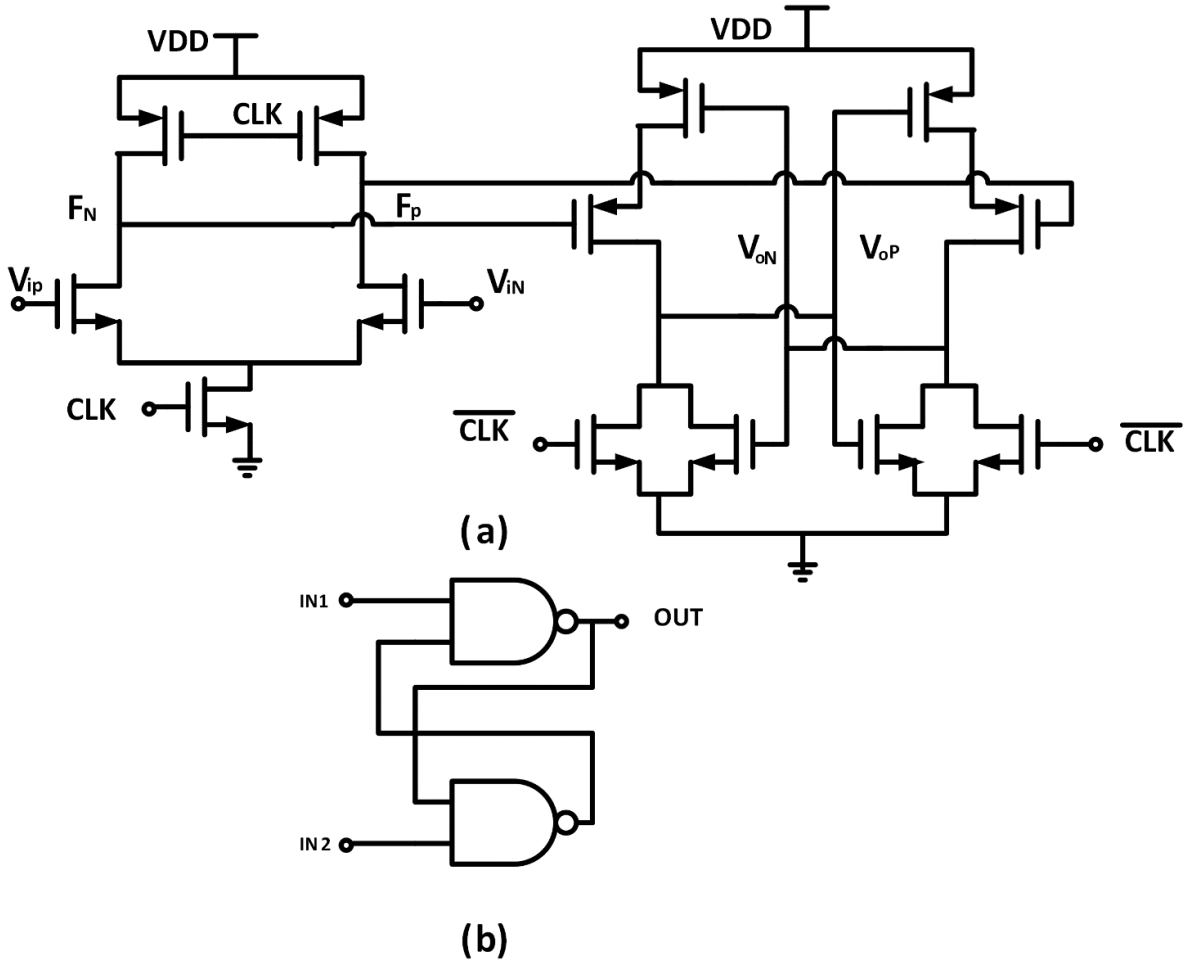


Figure 30 (a) Schematic of the two stage dynamic latched comparator (b) Latch

4.2 Simulation Results

The ADC has been designed in 180nm CMOS technology. Fig 31 shows the Fast Fourier transform (FFT) of the ADC with input frequency close to 250Hz. SNDR is about 54.88dB providing effective number of bit (ENOB) 8.84. The total measured power of ADC is 14.31nW at 1V supply power which gives the figure of merit (FOM) of 31.8 fJ/Conversion step. The power distribution cycle for the ADC is shown in Fig 32. The transient simulation is shown in Fig 33. Table II shows performance comparison of designed ADC.

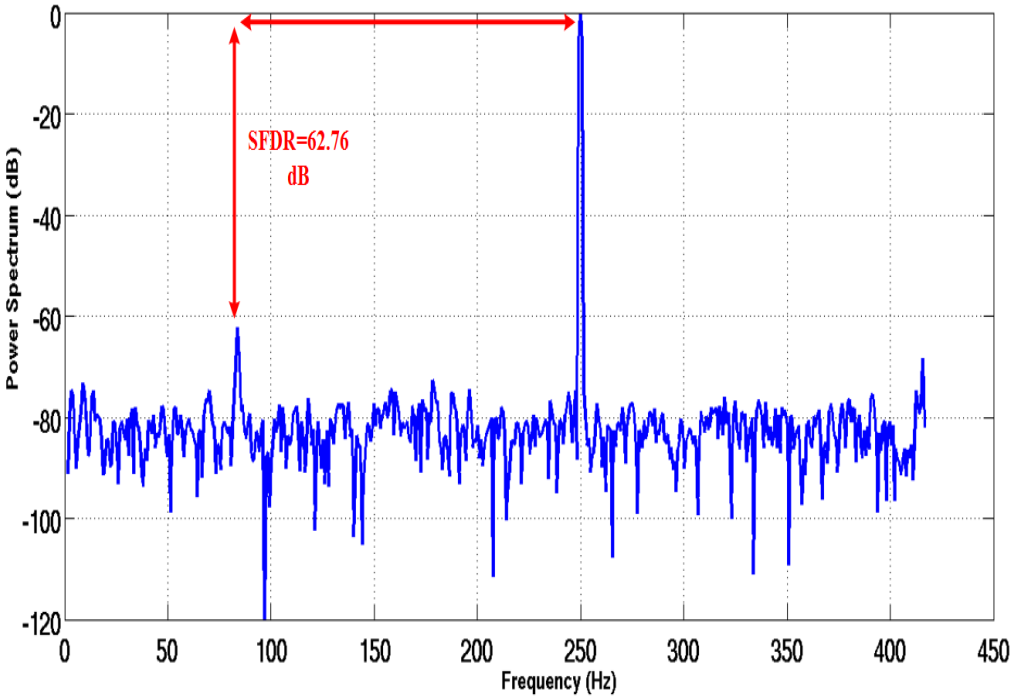


Figure 31 Power Spectrum Plot of Split Array SAR ADC

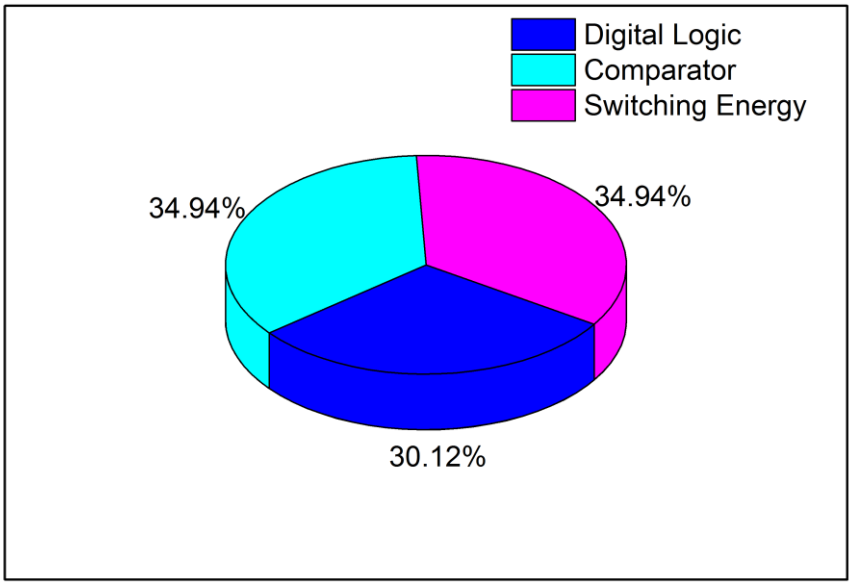


Figure 32 Power circle Distribution of Split array SAR ADC

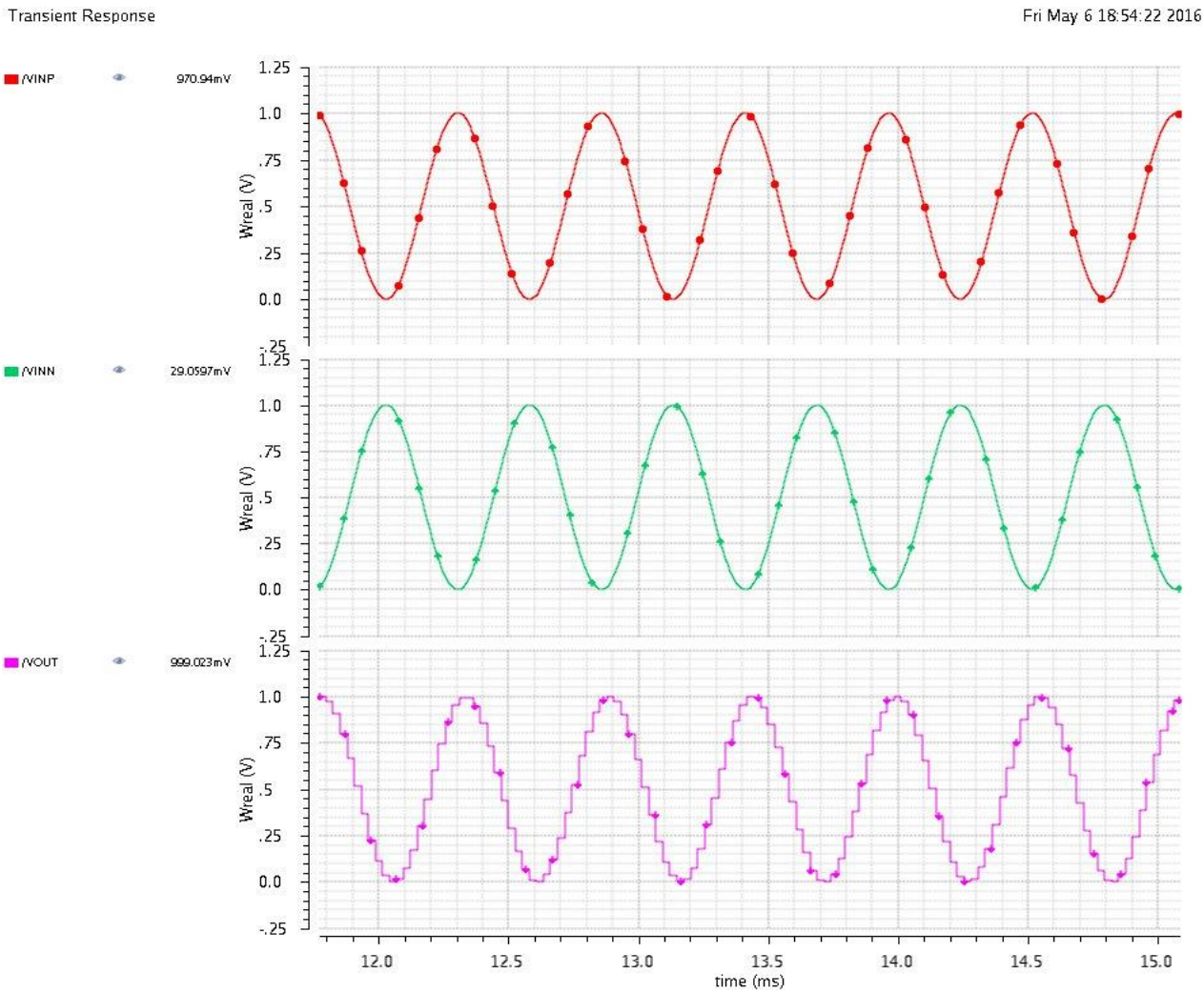


Figure 33 Transient plot of input and output of ADC

Parameters	This work	[5]	[20]	[21]
Technology (nm)	180	130	180	65
Sampling Rate (KS/s)	1	1	1	100MS/s
Power(nW)	14.31	53	43	1.46mW
ENOB	8.84	9.12	9.17	8.53
FOM(fJ/conv)	31.8	94.5	73	39
SNDR(dB)	54.88	53.67	57.17	51.2

Table II ADC comparison table

Chapter 5

A 320-nW 10-bit 1.23-kS/s Monotonic capacitor switching procedure SAR ADC in 180nm CMOS for Biomedical applications

This Chapter presents a low-power 10-bit 1.23-KS/s successive approximation register (SAR) analog-to digital converter (ADC) that uses a monotonic capacitor switching procedure. Compared to converters that use the conventional procedure, the average switching energy and total capacitance are reduced by about 81% and 50%, respectively. In the monotonic switching procedure, the input common-mode voltage gradually converges to ground. An improved comparator diminishes the signal-dependent offset caused by the input common-mode voltage variation. The system is designed in UMC in 180nm CMOS technology with 1V supply voltage and a 1-kS/s sampling rate. The system achieves a signal-to-noise and distortion ratio of 55.16dB and consumes 320 nW, resulting in a figure of merit of 540 fJ/conversion-step.

5.1 Circuit Implementation

In SAR ADCs, the primary sources of power dissipation are the digital control circuit, comparator, and capacitive reference DAC network. Digital power consumption becomes lower with the advancement of technology. Technology scaling also improves the speed of digital circuits. On the other hand, the power consumption of the comparator and capacitor network is limited by mismatch and noise.

Recently, several energy-efficient switching methods have been proposed to lower the switching energy of the capacitor network. The split capacitor method [22] reduces switching energy by 37%, and the energy-saving method [23] reduces energy consumption by 56% as shown in Fig 34. Although these methods reduce the switching energy of capacitors, they make the SAR control logic more complicated due to the increased number of capacitors and switches, yielding higher digital power consumption. The proposed monotonic switching method reduces power consumption by 81% without splitting or adding capacitors and switches [24]. The total capacitance in the DAC capacitor network is reduced by 50%. In addition, the switching method improves the settling speed of the DAC capacitor network. Table III summarizes the features of the four methods. Proposed architecture schematic is shown in Fig 36.

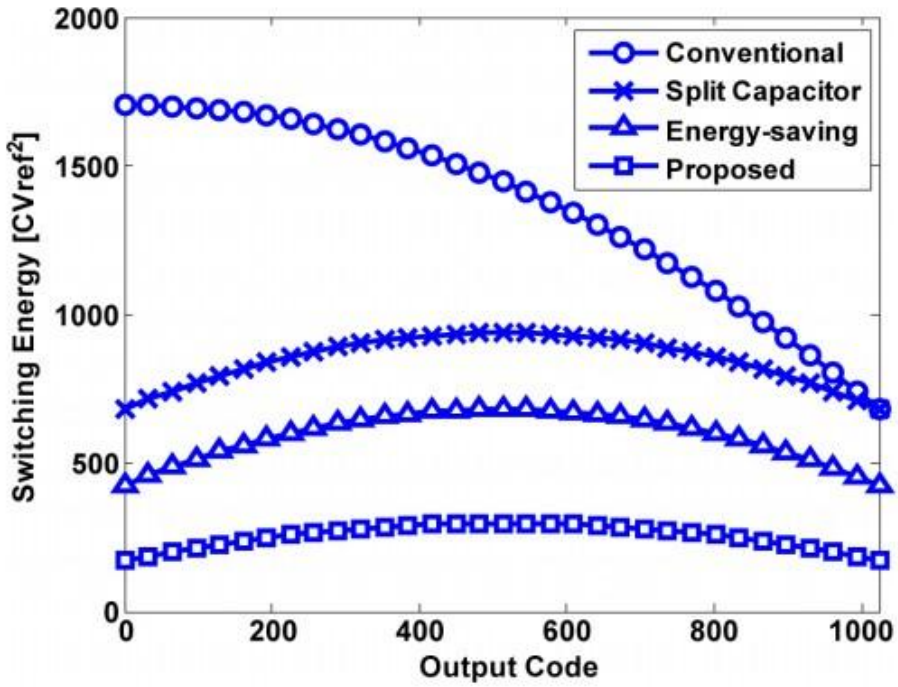


Figure 344 Switching energy verses output code

Switching procedure	Conventional	Split capacitors	Energy Saving	Monotonic
Normalized Switching power	1	0.63	0.44	0.19
No of switches	4N+10	8N+6	8N+2	4N
No of Capacitors	2N+2	4N	4N+2	2N
No of unit capacitors	2^N	2^N	2^N	2^{N-1}

Table III Comparison of switching procedures

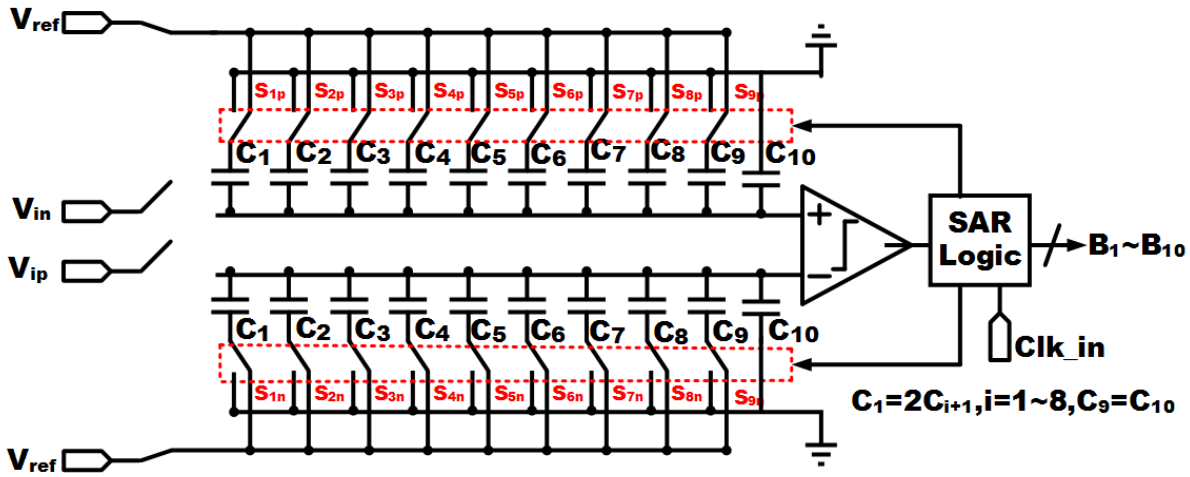


Figure 35 The proposed SAR ADC architecture

Key building blocks in SAR ADC are Control Logic, Comparator and Capacitor Array. The design considerations of the building blocks are described in the following subsections

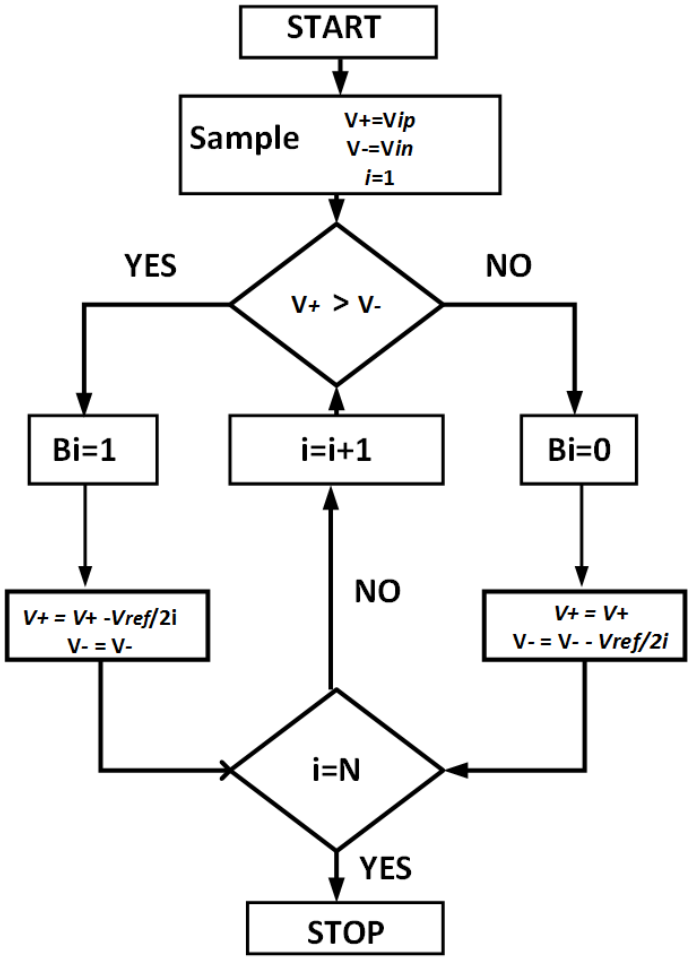


Figure 36 Flow chart of the proposed ADC

The proposed ADC samples the input signal on the top plates via transmission gate switches. At the same time, the bottom plates of the capacitors are reset to V_{ref}. Next, after the ADC turns off the transmission gate switches, the comparator directly performs the first comparison without switching any capacitor. According to the comparator output, the largest capacitor C_1 on the higher voltage potential side is switched to ground and the other one (on the lower side) remains unchanged. The ADC repeats the procedure until the LSB is decided. For each bit cycle, there is only one capacitor switch, which reduces both charge transfer in the capacitive DAC network and the transitions of the control circuit and switch buffer, resulting in smaller power dissipation. The flow chart of the proposed successive-approximation procedure is shown in Fig. 37.

5.1.1 Comparator

A dynamic latched comparator is used. The schematic for dynamic latched comparator is shown in Fig 38. During the conversion phase, the input voltages of the comparator approach ground. For proper function within the input common-mode voltage range from half to ground, the comparator uses a p-type input pair. Because a dynamic comparator does not consume static current, it is suitable for energy efficient design.

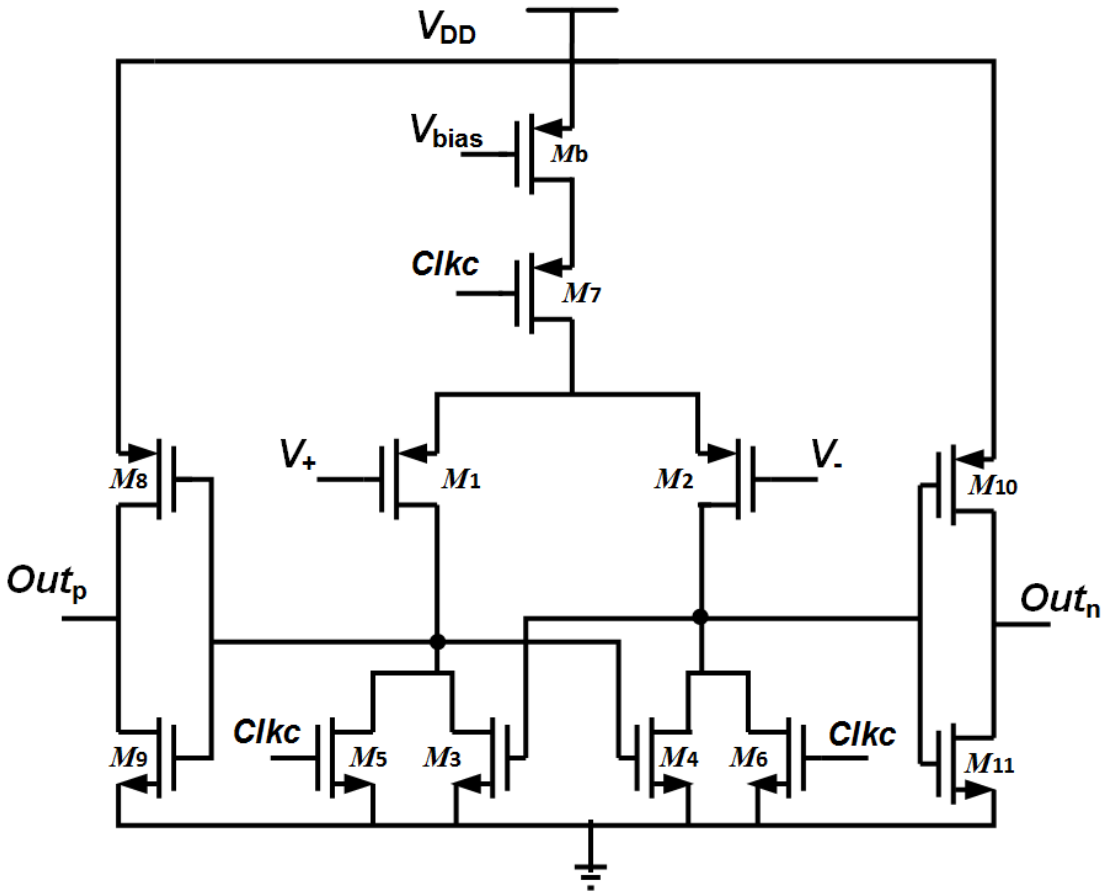


Figure 37 Dynamic Comparator

When *Clkc* is high, the comparator outputs Out_p and Out_n are reset to high. When *Clkc* goes to low, the differential pair. M_1 and M_2, compares the two input voltages. Then, the latch regeneration forces one output to high and the other to low according the comparison result. The offset voltage of this comparator can be expressed as [25]

$$V_{os} = \Delta V_{TH1,2} + \frac{(V_{GS} - V_{th})}{2}\left(\frac{\Delta S_{1,2}}{S_{1,2}} + \frac{\Delta R}{R}\right)$$

Where $\Delta V_{TH1,2}$ is the threshold voltage offset of the differential pair $M_1$and M_2, (V_{GS} -V_{TH}) is the effective voltage of the input pair, $\Delta S_{1,2}$ is the physical dimension mismatch between $M_1$and M_2, and ΔR is the loading resistance mismatch induced by $M_1 - M_6$. The first term is a static offset which does not affect the performance of a SAR ADC. The second term is a signal-dependent dynamic offset. The effective voltage of the input pair varies with the input common-mode voltage. The dynamic offset degraded the performance.

5.1.2 Capacitor Array

In monotonic capacitor SAR ADC the total capacitance is reduced by 50%. DAC is implemented using binary weighted capacitor to achieve better linearity. Unit capacitor in DAC should be kept as small as possible in order to reduce power dissipation. It value is determined by KT/C noise and mismatch parameter. Aside from above limiting factor, sampling leakage is also an additional major concern because of low speed of operation. Consequently a MIM Cap of 50fF is used as a unit capacitor. The layout of capacitive DAC is shown in Fig 39.

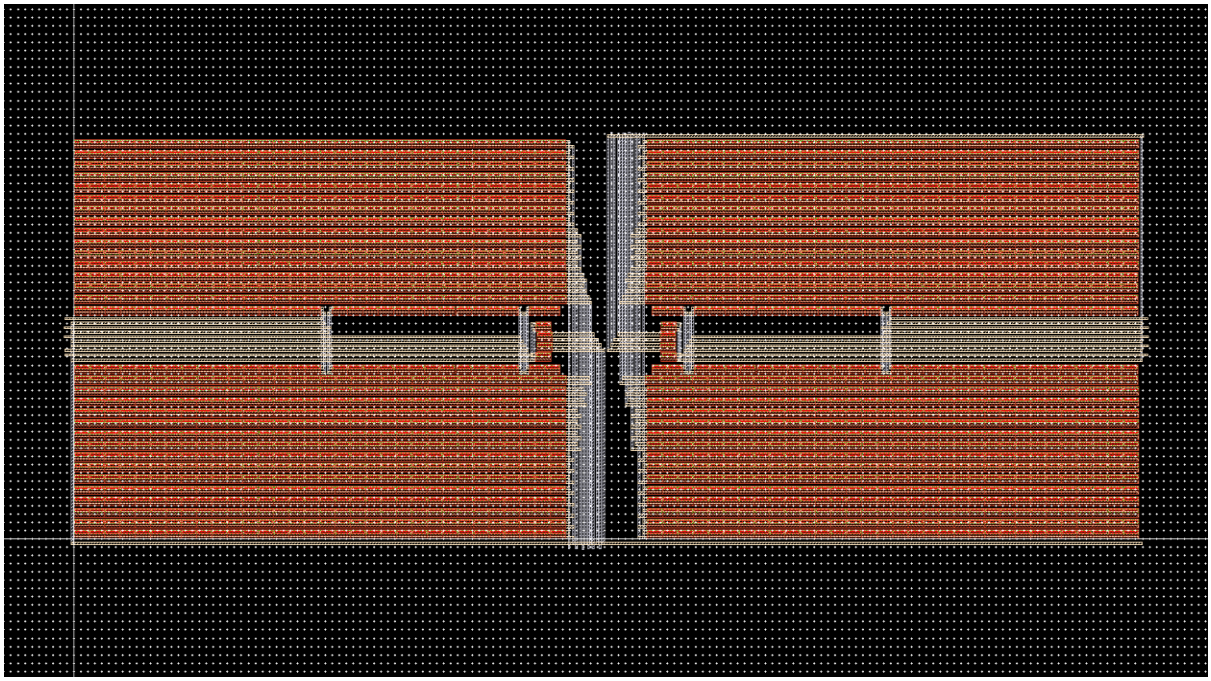


Figure 38 Capacitor DAC layout

5.1.3 SAR Control Logic

The SAR control logic block has two important aims. It sets the switches in function of the current state of the conversion and stores the digital output at the end of the conversion. The Successive Approximation Register has been implemented in Verilog. The code is then synthesized, it means compiled and mapped into the desired technology. The block diagram for the SAR Control logic is shown in Fig 40.

5.1.3.1 Verilog Code

In the first clock the system is reset, Data_N and Data_P are all <11111 11111>. After that the input is sampled on the top plates for 5 consecutive clock cycle. After sampling the input the track goes active high. Depending upon the comparator result the Data_P are set to < 01111 11111> if Comp ==1 or <11111 11111> if Comp == 0 and for Data_N reverse happens. It goes till the last bit is resolved. After the conversion is finished EOC signal goes high and the all the output bits are latched on Bit_Out register. The timing diagram is shown in Fig 41. The code is shown in appendix A

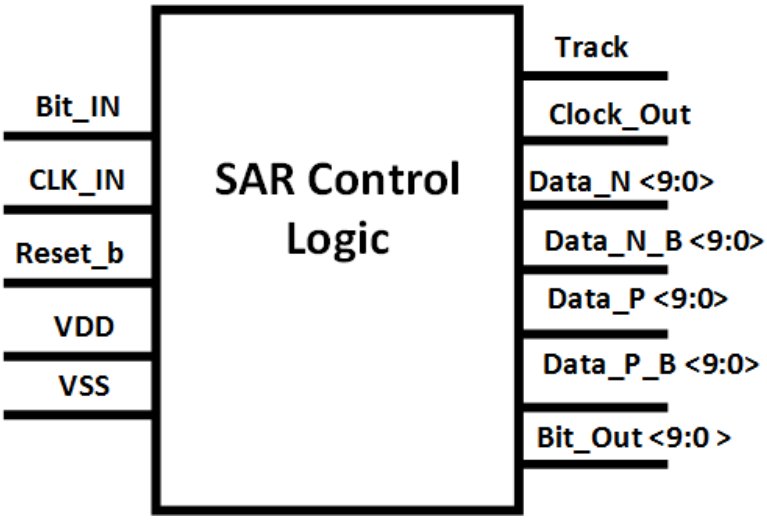


Figure 39 SAR logic block diagram

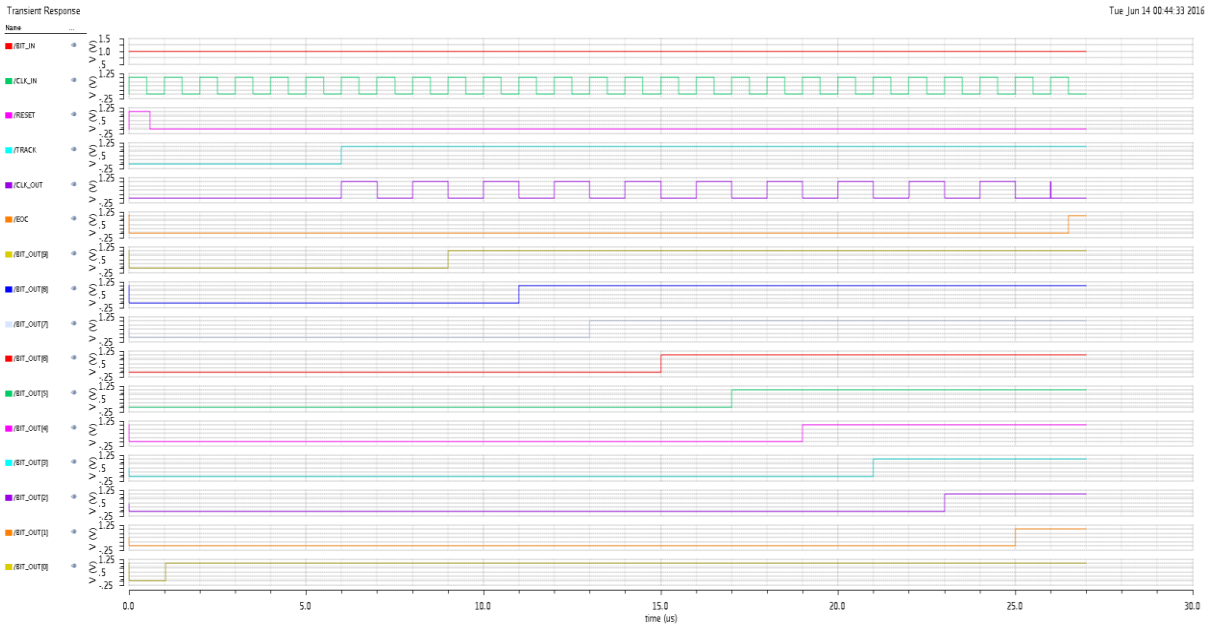


Figure 40 Timing Diagram of SAR logic Block

5.2 Simulation Results

The ADC has been designed in 180nm CMOS technology. Fig 42 shows the Fast Fourier transform (FFT) of the ADC with input frequency close to 250 Hz. SNDR is about 55.16 dB providing effective number of bit (ENOB) 8.86. The total measured power of ADC is 320nW at 1V supply power which gives the figure of merit (FOM) of 540 fJ/Conversion step. The possible switching procedure for 3 bit ADC with the quantitative energy dissipation of each switching phase is shown in Fig 44. Fig 45 show the top plate voltages of DAC during conversion. Table IV shows performance comparison of designed ADC.

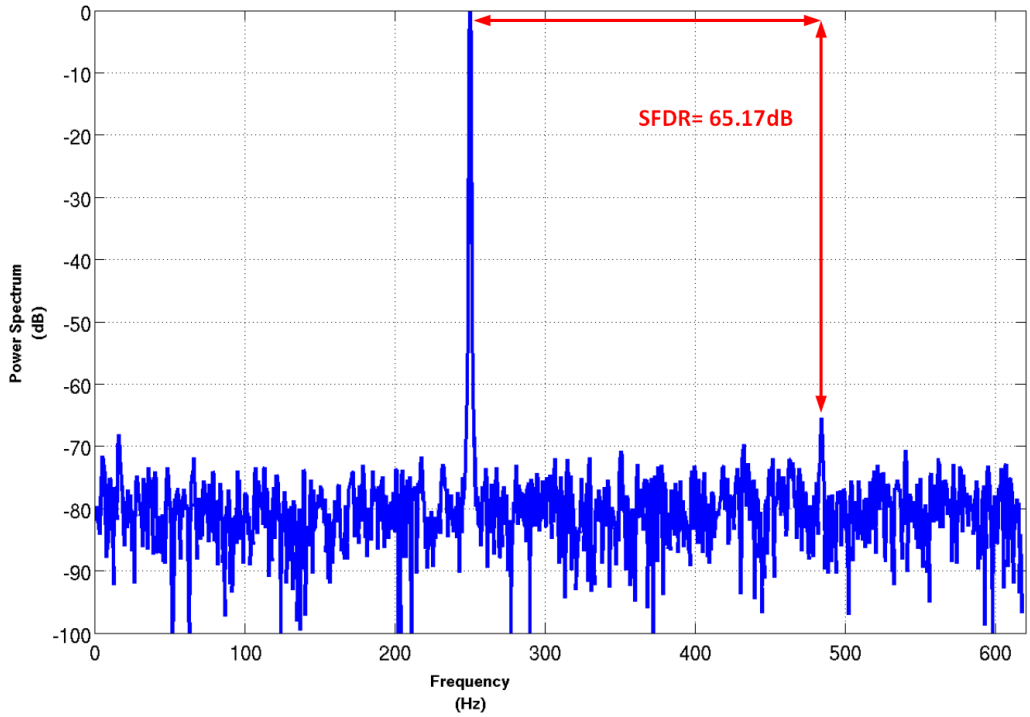


Figure 41 Power Spectrum of Monotonic SAR ADC

Parameters	This work	[24]	[26]	[21]
Technology (nm)	180	130	130	65
Sampling Rate (KS/s)	1.234	50MS/s	50MS/s	100MS/s
Power(nW)	320	0.826mW	0.92mW	1.46mW
ENOB	8.86	9.18	8.48	8.53
FOM(fJ/conv)	540	39	52	39
SNDR(dB)	55.16	54.4	56.5	51.2

Table IV ADC comparison table

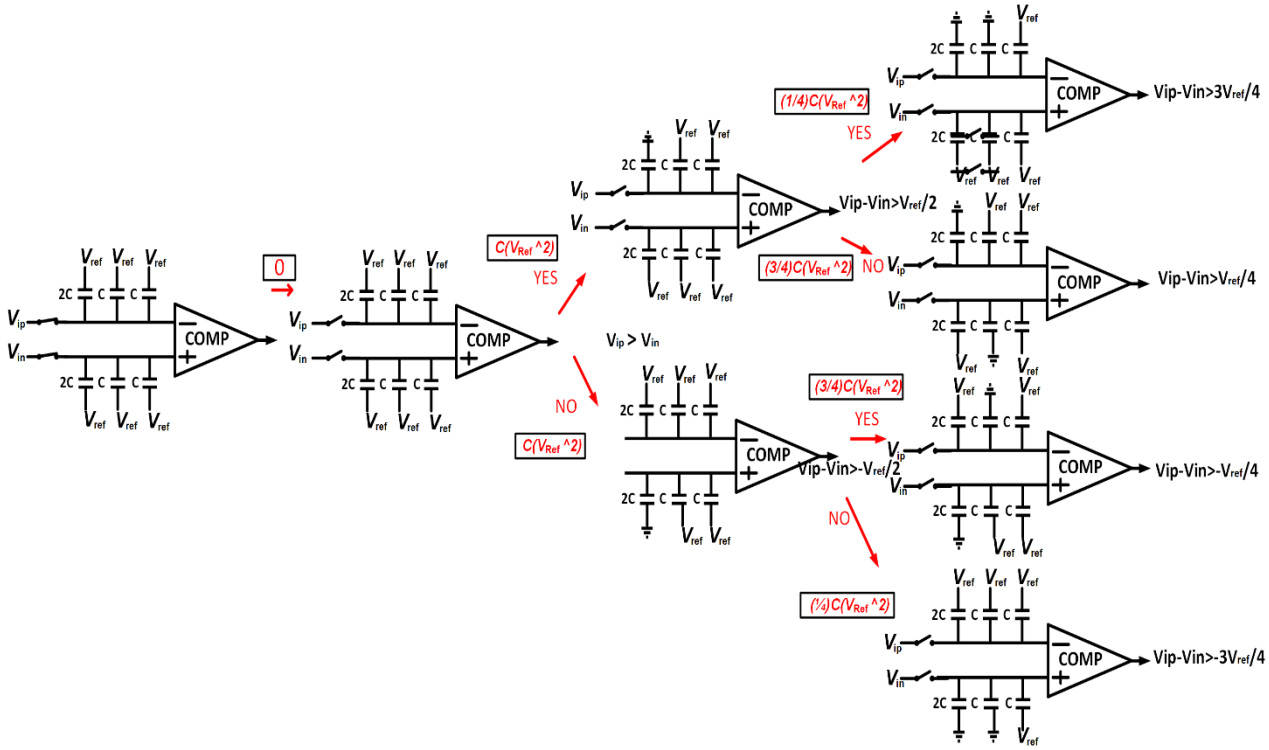


Figure 42 Switching procedure for Monotonic SAR ADC

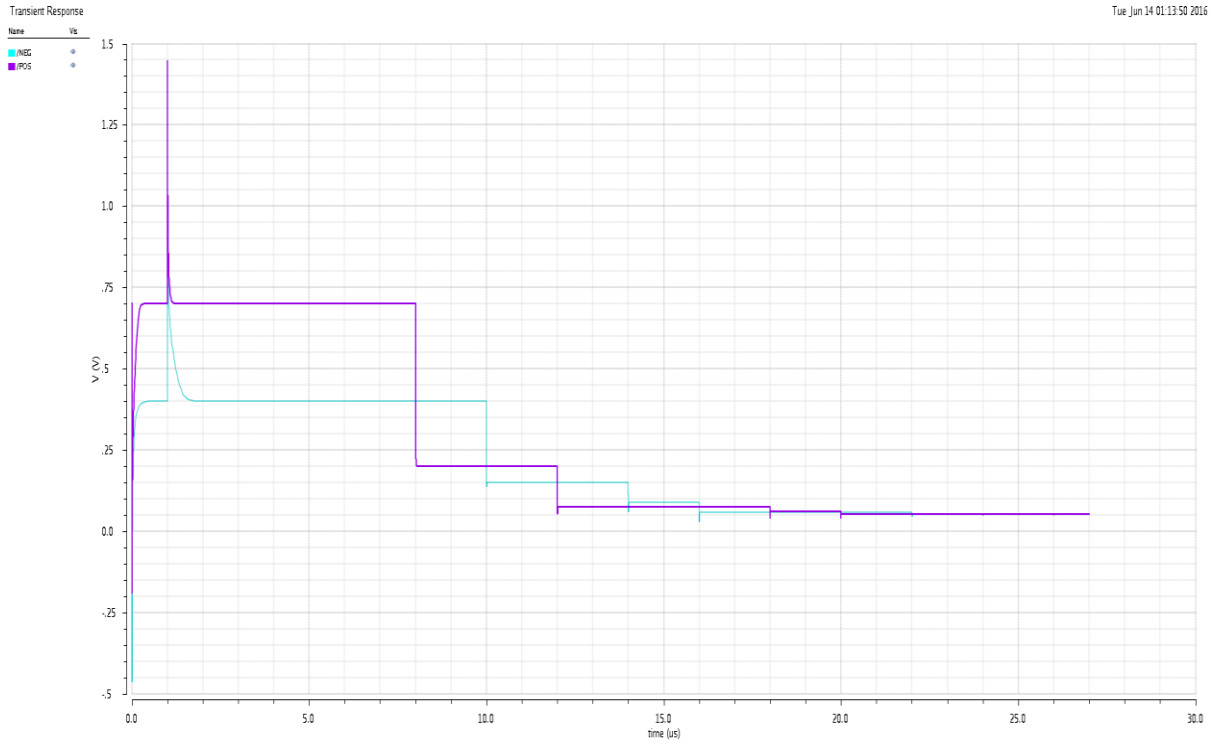


Figure 43 Waveform of Monotonic switching procedure

Chapter 6

A signal adaptive 10-bit 1-kS/s SAR ADC in 180nm CMOS for Biomedical applications

This Chapter presents a signal adaptive 10-bit, 1-KS/s successive approximation register (SAR) analog-to-digital converter (ADC) for biomedical applications. To make ADC signal adaptive a reference scaling technique is adopted. ADC was designed in 180nm CMOS technology with a 1-V power supply and a 1-kS/s sampling rate for monitoring bio potential signals, the ADC achieves a signal-to-noise and distortion ratio of 54 dB and consumes 50 nW, resulting in a figure of merit of 122fJ/conversion-step.

6.1 Circuit Implementation

Key building blocks in SAR ADC are Control Logic, Comparator and Capacitor Array. The design considerations of the building blocks are described in the following subsections. In conventional SAR ADC we take two reference voltage V_{refp} (VDD) and V_{refn} (GND). But if our input signal is not approaching the rail to rail swing then effectively we are always losing some bits. In this paper we have designed an SAR ADC in which the reference voltages V_{refp}, V_{refn} are scaled according to input voltage. If the input signal peak to peak value is low then reference voltage are scaled down and vice versa.

6.1.1 Sampling Switch

A basic sampling circuit consists of a switch and a capacitor. When the switch is on, the input voltage is connected to the top-plate of the sampling capacitor. When the switch is off, the top-plate node of the capacitor is isolated, and the capacitor holds the sampled voltage value. As the reference voltage is scaling so transmission gate is employed for sampling input voltage and reference voltage so that the On-resistance can be made input independent. A transmission gate is employed to sample the input signal and reference voltage on to capacitor plate. The error voltage introduced by Charge injection is relatively small because of large capacitor array. As the operational speed of ADC is relatively small (1 KS/s) smaller size NMOS and PMOS can be used to reduce parasitic and hence limiting charge injection. Fig 46 shows the ON resistance curve.

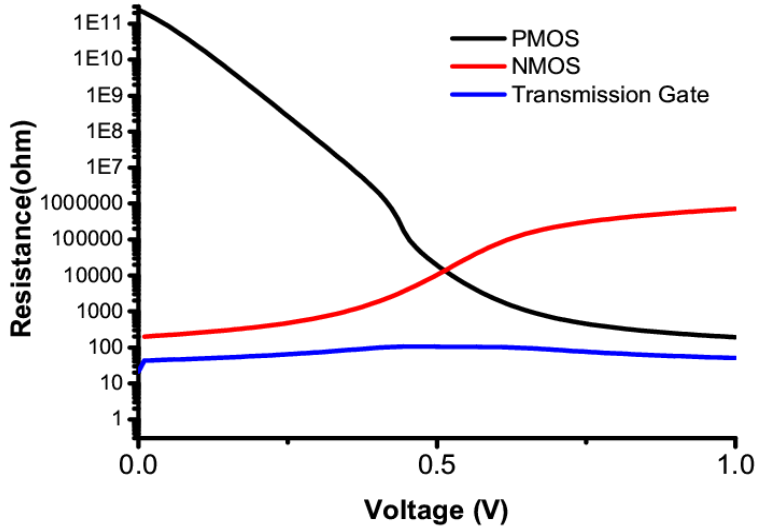


Figure 44 On-Resistance Curve of PMOS NMOS and Transmission gate

6.1.2 DAC Control Logic

The proposed system architecture utilizes the synchronous SAR logic. It encompasses a ring counter and code register [14]. It generates the sample signal and the switch control signals for the DAC. Fig 47 shows the schematic and Fig 48 shows the timing diagram for DAC control logic.

In the first clock cycle foremost D flip flop in ring counter is set and all other flip flops are reset. This operation provides the Sample signal. In second clock cycle MSB is set. In each clock cycle one of the output of ring counter sets the flip flop in code register. The output of the current flip flop in code register is used as a clock for the previous flip flop to register the comparator output. At the end of the conversion an EOC signal is generated to read the digital output. To reduce power dissipation transmission gate based Sets-reset D flip flop are used. In order to decrease the leakage power while maintaining the speed, high VT (threshold) transistors are used in the noncritical paths and low VT transistors in the critical path. To reduce the dynamic power further current starved architecture is used in designing the logic gates.

6.1.3 Comparator

Dynamic two stage comparator is employed for low power consumption. The first stage is an amplifier and the second stage is a latch. During the reset phase when clock signal is low, PMOS transistors in the first stage charge F nodes to VDD and turn off the latch stage. In this phase, the output nodes are reset to zero through NMOS switches in the latch stage. This architecture is power efficient and fast due to low capacitance at F nodes which are mainly drain diffusion capacitances of NMOS and PMOS transistors connected to these nodes. When clock goes from low to high tail transistor in first stage is

turned ON and the nodes F_n and F_p starts discharging depending upon the input voltage. When either node voltages F_n and F_p goes below V_{th} of second stage input transistor, amplification starts occurring and the output voltage increases and positive feedback system is activated . It evidently generates output level of high and low voltage in the regeneration phase. The output is finally latched into NAND type SR latch to be feed to shift register. Fig 49 shows the schematic of comparator and latch.

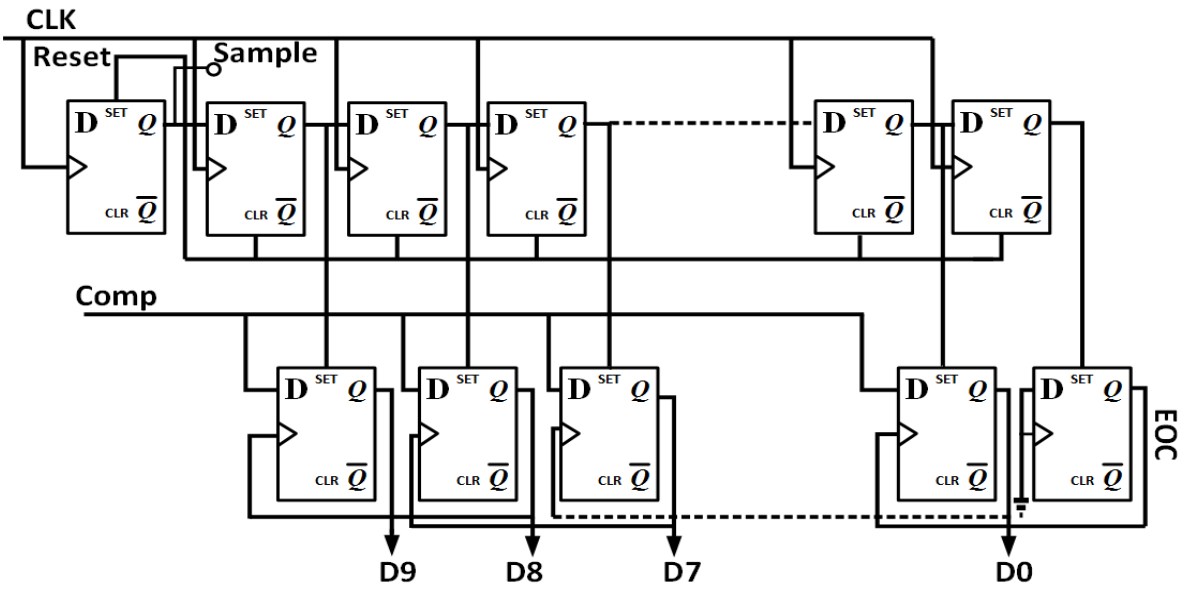


Figure 45 SAR Control Logic

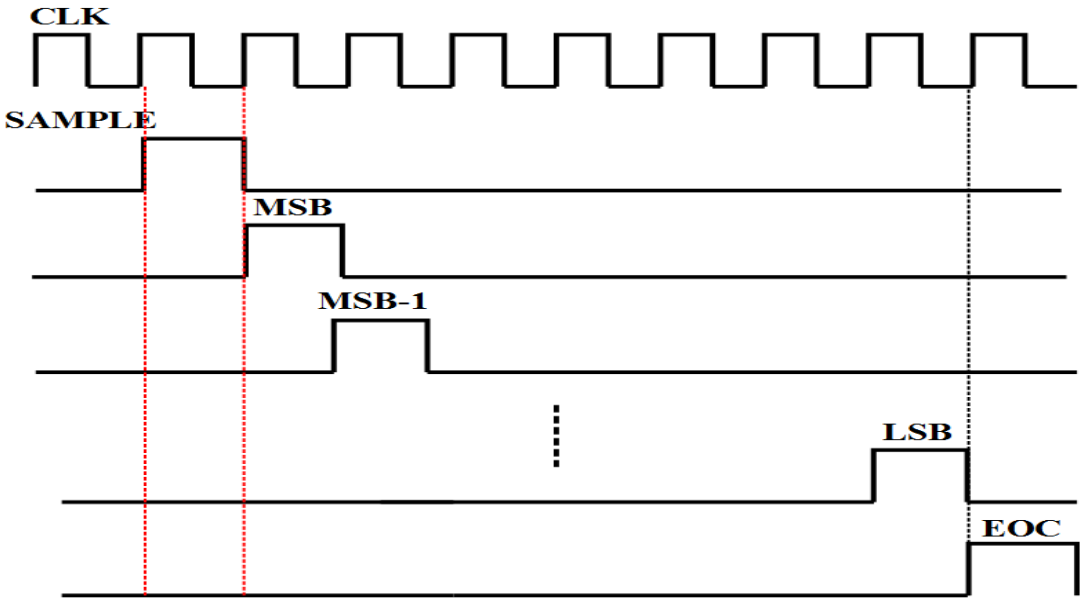


Figure 46 Timing Sequence of the synchronous SAR Control Logic

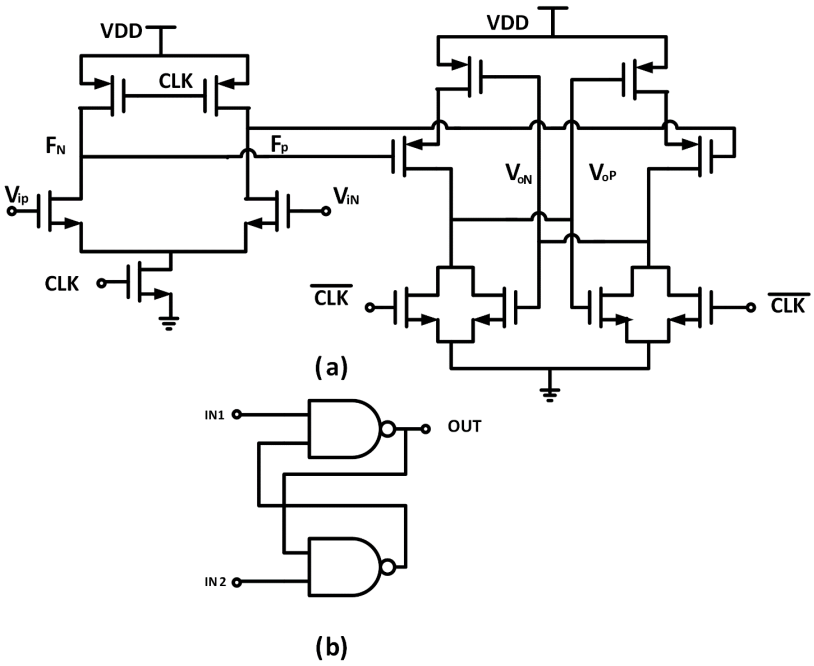


Figure 47 (a) Schematic of the two stage dynamic latched comparator (b) Latch

5.1.2 Capacitor Array

In monotonic capacitor SAR ADC the total capacitance is reduced by 50%. DAC is implemented using binary weighted capacitor to achieve better linearity. Unit capacitor in DAC should be kept as small as possible in order to reduce power dissipation. It value is determined by KT/C noise and mismatch parameter. Aside from above limiting factor, sampling leakage is also an additional major concern because of low speed of operation. Consequently a MIM Cap of 20fF is used as a unit capacitor. Fig 50 shows the layout of capacitive DAC.

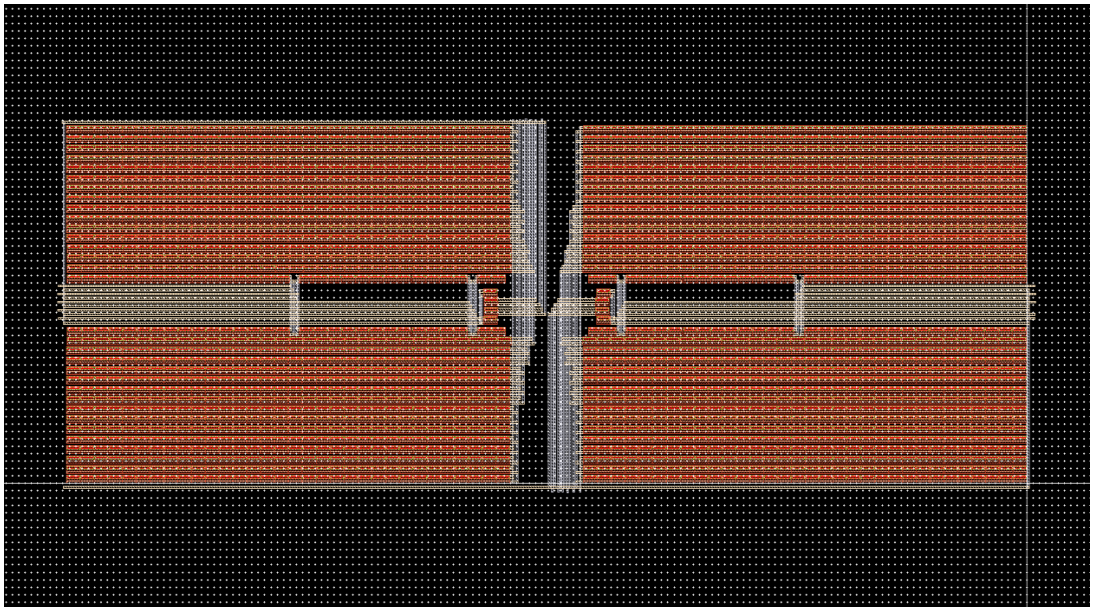


Figure 48 Capacitor DAC layout

5.2 Simulation Results

The ADC has been designed in 180nm CMOS technology. Fig 51 shows the Fast Fourier transform (FFT) of the ADC with input frequency close to 250Hz. SNDR is about 54dB providing effective number of bit (ENOB) 8.67. The total measured power of ADC is 50nW at 1V supply power which gives the figure of merit (FOM) of 122 fJ/Conversion step. Fig 52 shows the power consumption distribution.

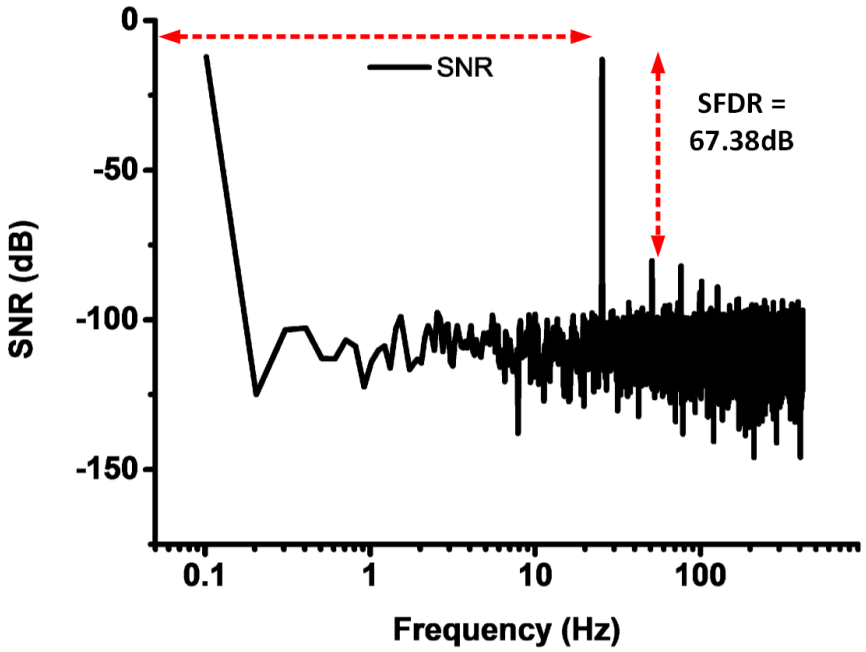


Figure 49 Power spectral Plot for SAR ADC

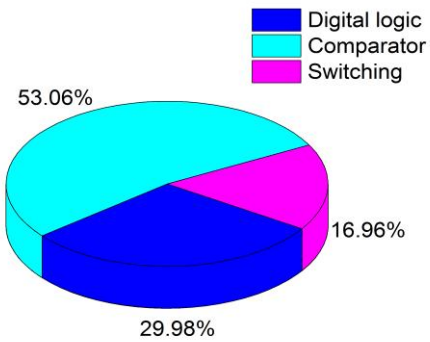


Figure 50 Power consumption circle

Chapter 7

Conclusion and Future Work

6.1 Conclusion

In this work, a 10-bit 1kS/s 1V SAR ADC for biomedical application is designed in transistor level in UMC 180nm CMOS technology and it achieves a very low power with good performance.

Four main approaches regarding the design of successive approximation register (SAR) are explored here taking in consideration of energy efficiency. In first design conventional charge redistribution binary weighted SAR ADC is designed. To minimize power, this ADC: 1) combines the capacitive DAC with S/H circuit; 2) uses the binary-weighted capacitor array for the DAC; 3) utilizes the dynamic latch comparator. In second design split capacitor array SAR ADC is designed which decreased the area foot print by 50% and achieves power saving of 37% in comparison to conventional architecture. In third design to reduce the Switching power a monotonic capacitor switching procedure is adopted which reduces the power consumption by 81% without splitting or adding the capacitors and switches. The total capacitance in the DAC capacitor network is reduced by 50%. In addition, the switching method improves the settling speed of the DAC capacitor array. In fourth design a scaling of reference voltage with respect to the input signal power is done. It improves the resolution of input signal.

6.2 Future work

Although this prototype SAR ADC is able to achieve the good FoM for 1KS/s sampling rate with 10b ENOB, there are still many opportunities for improvement.

1. In this work, to minimize the power, input offset cancellation schemes are avoided during the design of comparator. In real chip measurement, the input offset error has to be cancelled otherwise the comparator will cause a large offset error which directly affects the ADC's performance.
2. There are other energy efficient switching techniques such as merged capacitor, inverted merged capacitor which achieves a staggering 98% reduction in switching power. New switching techniques like these can be explored and implemented.
3. Noise shaping SAR ADC can be implemented which achieves high resolution with much less hardware.
4. Redundancy is still an underused technique, particularly in the analog and mixed-signal domains.

APPENDICES I

Verilog HDL code for SAR Logic

```
// Created by ihdl
module SAR_DAC
(bit_in,clk_in,reset_b,track,clk_out,clk_out_b,data_n,data_n_b,data_p,data_p_b,bit_out,vdd,vss,bit_o
ut_reg,EOC);
parameter IDLE = 5'b00000;
parameter STAGE1 = 5'b00111;
parameter STAGE2 = 5'b01001;
parameter STAGE3 = 5'b01011;
parameter STAGE4 = 5'b01101;
parameter STAGE5 = 5'b01111;
parameter STAGE6 = 5'b10001;
parameter STAGE7 = 5'b10011;
parameter STAGE8 = 5'b10101;
parameter STAGE9 = 5'b10111;
parameter STAGE10 = 5'b11001;
input bit_in,clk_in,reset_b;
input vdd,vss;
output clk_out,clk_out_b;
output [9:0] data_n_b;
output [9:0] data_p_b;
output reg track;
output reg [9:0] data_n;
output reg [9:0] data_p;
output reg [9:0] bit_out;
output reg [9:0] bit_out_reg;
output reg EOC;
reg [4:0] cycle_count;
wire [4:0] Q;
assign clk_out = ((cycle_count == 5'd6) || (cycle_count == 5'd8) || (cycle_count == 5'd10) || (cycle_count
== 5'd12) || (cycle_count == 5'd14) || (cycle_count == 5'd16) || (cycle_count == 5'd18) || (cycle_count
== 5'd20) || (cycle_count == 5'd22) || (cycle_count == 5'd24)) ? 1'b1 : 1'b0;
assign data_p_b = ~ data_p;
assign data_n_b = ~ data_n;
assign clk_out_b = ~clk_out;
always @ (posedge clk_in or negedge reset_b)
begin
if(~reset_b)
begin
cycle_count <= 5'b0000;
track <= 1'b0;

end


else
begin
cycle_count <= cycle_count + 1'b1;
if(cycle_count >= 5'd5 && cycle_count <=5'd25)
begin
```

```
track <= 1'b1;
end
else if(cycle_count >5'd25)
begin
track <= 1'b0;
cycle_count <= 1'b0;

end
//cycle_count <= cycle_count + 1'b1;
end
end
assign Q = cycle_count;
//////////////////////////////////////////
always @ (posedge clk_in or negedge reset_b)
begin
if(~reset_b)
begin
data_n <= 10'b0;
data_p <= 10'b0;
end
else if(Q == 5'd1)
begin
data_n <= 10'b1111111111;
data_p <= 10'b1111111111;
end
else
case(Q)
IDLE:
begin
data_n <= 10'b1111111111;
data_p <= 10'b1111111111;
end
STAGE1:
begin
if (bit_in ==0)
data_n <= {1'b0,data_n[8:0]};
else
data_p <= {1'b0,data_p[8:0]};
end
STAGE2:
begin
if (bit_in ==0)
data_n <= {data_n[9],1'b0,data_n[7:0]};
else
data_p <= {data_p[9],1'b0,data_p[7:0]};
end
STAGE3:
begin
if (bit_in ==0)
data_n <= {data_n[9:8],1'b0,data_n[6:0]};
else
data_p <= {data_p[9:8],1'b0,data_p[6:0]};
end
STAGE4:
begin
```

```
if (bit_in ==0)
data_n <= {data_n[9:7],1'b0,data_n[5:0]};
else
data_p <= {data_p[9:7],1'b0,data_p[5:0]};
end
STAGE5:
begin
if (bit_in ==0)
data_n <= {data_n[9:6],1'b0,data_n[4:0]};
else
data_p <= {data_p[9:6],1'b0,data_p[4:0]};
end
STAGE6:
begin
if (bit_in ==0)
data_n <= {data_n[9:5],1'b0,data_n[3:0]};
else
data_p <= {data_p[9:5],1'b0,data_p[3:0]};
end
STAGE7:
begin
if (bit_in ==0)
data_n <= {data_n[9:4],1'b0,data_n[2:0]};
else
data_p <= {data_p[9:4],1'b0,data_p[2:0]};
end
STAGE8:
begin
if (bit_in ==0)
data_n <= {data_n[9:3],1'b0,data_n[1:0]};
else
data_p <= {data_p[9:3],1'b0,data_p[1:0]};
end
STAGE9:
begin
if (bit_in ==0)
data_n <= {data_n[9:2],1'b0,data_n[0]};
else
data_p <= {data_p[9:2],1'b0,data_p[0]};
end
STAGE10:
begin
if (bit_in ==0)
data_n <= {data_n[9:1],1'b0};
else
data_p <= {data_p[9:1],1'b0};
end
endcase
end
always @ (posedge clk_in or negedge reset_b)
begin
//buffer <= bit_in;
if(~reset_b)
begin
bit_out_reg <= 10'b0000000000;
```

```
end
else
case(Q)
IDLE:
begin
bit_out_reg <= 10'b0000000000;
end
STAGE1:
begin
bit_out_reg[9:0] <= {bit_in,bit_out_reg[8:0]};
end
STAGE2:
begin
bit_out_reg[9:0] <= {bit_out_reg[9],bit_in,bit_out_reg[7:0]};
end
STAGE3:
begin
bit_out_reg[9:0] <= {bit_out_reg[9:8],bit_in,bit_out_reg[6:0]};
end
STAGE4:
begin
bit_out_reg[9:0] <= {bit_out_reg[9:7],bit_in,bit_out_reg[5:0]};
end
STAGE5:
begin
bit_out_reg[9:0] <= {bit_out_reg[9:6],bit_in,bit_out_reg[4:0]};
end
STAGE6:
begin
bit_out_reg <= {bit_out_reg[9:5],bit_in,bit_out_reg[3:0]};
end
STAGE7:
begin
bit_out_reg <= {bit_out_reg[9:4],bit_in,bit_out_reg[2:0]};
end
STAGE8:
begin
bit_out_reg <= {bit_out_reg[9:3],bit_in,bit_out_reg[1:0]};
end
STAGE9:
begin
bit_out_reg <= {bit_out_reg[9:2],bit_in,bit_out_reg[0]};
end
STAGE10:
begin
bit_out_reg <= {bit_out_reg[9:1],bit_in};
end
endcase
end
always @ (posedge clk_in or negedge reset_b)
begin
if(~reset_b)
begin
bit_out <= 10'b0000000000;
EOC <=1'b0;
```

```
end
else if(Q == 5'b11001)
begin
bit_out <= {bit_out_reg[9:1],bit_in};
EOC <=1'b1;
end
end
/*ways @ (posedge clk_in or negedge reset_b)
begin
if(~reset_b)
begin
track <= 1'b0;
end
else if(cycle_count >= 5'd5 && cycle_count <=5'd25)
begin
track <= 1'b1;
end
else if(cycle_count >5'd25)
begin
track <= 1'b0;
cycle_count <= 1'b0;
end
else
track <= 1'b0;
if(cycle_count == 5'd25)
begin
EOC <=1'b1;
end
else
EOC <=1'b0;
end*/
endmodule
```

APPENDICES II

Matlab code for SNR calculation

```
clear all;clc;
f=importdata('test1dac.csv');
fre=f.data(:,1);
vol=f.data(:,2);
vol(1:2)=0;
y=max(vol);
%n1=find(vol == max(vol));
vol_normalized=vol/y;
psd=(vol_normalized).^2;
n1=find(psd == max(psd));
signal_power=psd(n1-1)+psd(n1)+psd(n1+1);
noise_power=sum(psd)-signal_power;
snr=10*log10(signal_power/noise_power)
plot(fre,10*log10(psd));
```

APPENDICES III

Matlab modelling for 10-bit SAR ADC

```
clc
clear all
close all
n = 0:192e-3:(65536*16*192e-3); %Time index
vinp1 = 0.8*sin(2*pi*101*n/(192*10^3));
vinn1 = 0.8*sin(2*pi*101*n/(192*10^3)).*-1;
vinp = vinp1;
vinn = vinn1;
for(i=1:length(n))
outtemp2 = 0;
vintemp2 = 0; vintemp3 = 0;
vintemp4 = 0;
vinp = vinp1(i);
vinn = vinn1(i);
vref = 2^-1*2;
if(vinp >= vinn)
bit(1) = 1;
vinptemp = vinp - vref;
vintemp1 = vinn1(i);
else
bit(1) = 0;
vintemp1 = vinn - vref;
vintemp = vinp;
end
for(k=2:10)
vref = 2^-k*2;
if(vinptemp >= vintemp1)
bit(k) = 1;
vintemp2 = vintemp1 - vref;
vinptemp1 = vintemp2;
else
bit(k) = 0;
vintemp4 = vintemp1 - vref;
vintemp1 = vintemp4;
end
end
count = 9;
for(j=1:10)
outtemp = outtemp2 + bit(j).*2^count;
outtemp2 = outtemp;
count = count -1;
end
outtemp1 = outtemp/512;
dacout(i) = outtemp1;
k =2;j=1;
end
figure(1)
plot(1:65536,dacout(1:65536));
figure(2)
plot(1:65536,vinp1(1:65536));
figure(3)
plot(1:65536,vinn1(1:65536));
```

APPENDICES IV

Elaboration of ADC specification

1 Resolution

Resolution of ADC is the number of output bits that ADC generate, it indicates the minimum input voltage that ADC can generate the code. The smallest step is known as least significant bit ($V_{LSB} = V_{REF}/2^N$).

2 Signal to Noise Ratio (SNR)

It is the ratio of rms (root mean square) of full-scale input to rms of quantization error [11].

$$\text{SNR} = 20\,\frac{VIN(\max)}{Verror} = 20\log\frac{2^N(LSB)/2\sqrt{2}}{LSB/\sqrt{12}} = 6.023\text{N} + 1.76.$$

3 Signal to Noise and Distortion Ratio (SINAD)

It is the ratio of rms (root mean square) of full-scale input to rms of all other spectral component (including random errors and distortion).

$$\text{SINAD} = 20\log_{10}\left(\frac{A_{Signal}}{A_{Noise}+A_{\boldsymbol{HD}}}\right)$$

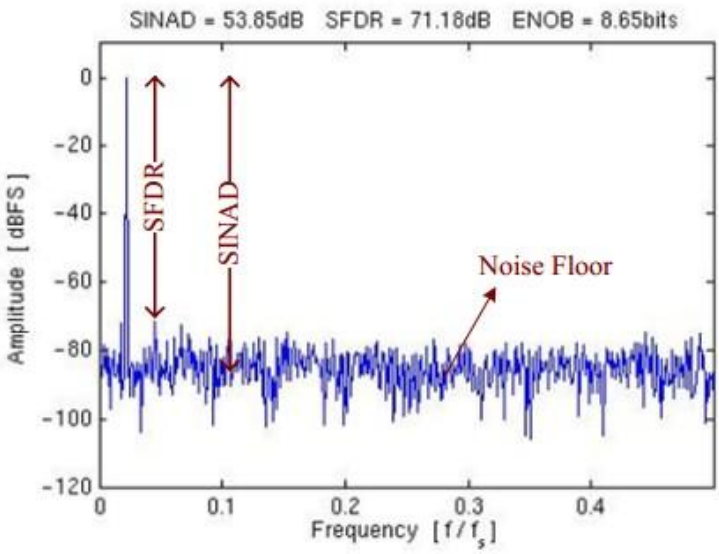
4 Spurious Free Dynamic Range (SFDR)

It is the ratio of input signal to largest spur.

5 Effective Number of Bits (ENOB)

ENOB is obtained from SINAD. It is the actual resolution obtained from ADC.

$$\text{ENOB} = \frac{(SINAD-1.76)db}{6.023db}$$

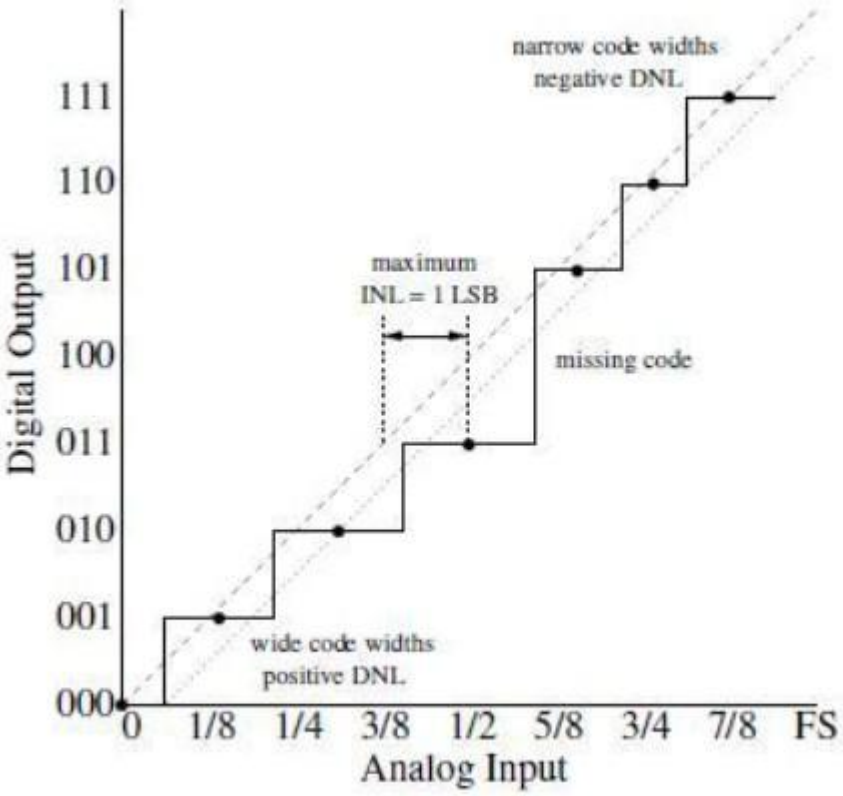


1. Integral Nonlinearity (INL)

INL is the difference between the data convertors output values and a reference straight line drawn through the first and last output values. INL defines the linearity of the overall transfer curve.

2. Differential Nonlinearity (DNL)

DNL is the deviation of the code transition from the ideal one (1LSB). Non-ideal components causes the analog increment to differ from their ideal values.



References

[1] Yanqing Zhang; Fan Zhang; Shakhsheer, Y.; Silver, J.D.; Klinefelter, A.; Nagaraju, M.; Boley, J.; Pandey, J.; Shrivastava, A.; Carlson, E.J.; Wood, A.; Calhoun, B.H.; Otis, B.P., ”A Batteryless 19 µW MICS/ISM-Band Energy Harvesting Body Sensor Node SoC for ExG Applications,” in Solid-State Circuits, IEEE Journal of , vol.48, no.1, pp.199-213, Jan. 2013

[2] Wu, C.-C.; Kuo, W.-C.; Wang, H.-J.; Huang, Y.-C.; Chen, Y.-H.; Chou, Y.-Y.; Yu, S.-A.; Lu, S.-S., ”A pliable and batteryless real-time ECG monitoring system-in-a-patch,” in VLSI Design, Automation and Test (VLSI-DAT), 2015 International Symposium on , vol., no., pp.1-4, 27-29 April 2015

[3] Pravanjan patra Kunal yadav, nagveni vamsi ., ” A 343nW Biomedical Signal Acquisition System Powered by Energy Efficient (62.8%) Power Aware RF Energy Harvesting Circuit,” in 2016 IEEE International Symposium on Circuits and Systems (ISCAS), montreal, 2016,

[4]B. Murmann, “ADC Performance Survey 1997-2013,”http://www.stanford.edu/~murmann/adcsurvey.html.

[5] Dai Zhang; Bhide, A.; Alvandpour, A., ”A 53-nW 9.1-ENOB 1-kS/s SAR ADC in 0.13m CMOS for Medical Implant Devices,” Solid-State Circuits, IEEE Journal of , vol.47, no.7, pp.1585,1593, July 2012 doi: 10.1109/JSSC.2012.2191209.

[6] Guan-Ying Huang; Soon-Jyh Chang; Chun-Cheng Liu; Ying-Zu Lin, ”A 1-W 10-bit 200-kS/s SAR ADC With a Bypass Window for Biomedical Applications,” Solid-State Circuits, IEEE Journal of , vol.47, no.11, pp.2783,2795, Nov. 2012.

[7] C.-C. Liu, S.-J. Chang, G.-Y. Huang, and Y.-Z. Lin, “A 0.92mW 10-bit 50- MS/s SAR ADC in 0.13µm CMOS process,” in Symposium on VLSI Circuits, pp. 236–237, June 2009.

[8] V. Hariprasath, J. Guerber, S.-H. Lee, and U.-K. Moon, “Merged Capacitor Switching Based SAR ADC with Highest Switching Energy-Efficiency,” *Electronics Letters*, vol. 46, pp. 620–621, April 2010.

[9] Albert Hsu Ting Chang, “Low-Power High-Performance SAR ADC with Redundancy and Digital Background Calibration” MIT thesis, pp. http://hdl.handle.net/1721.1/82177

[10] Brian P. Ginsburg, “Energy-Efficient Analog-to-Digital Conversion for Ultra-Wideband Radio” MIT thesis.

[11] Dai Zhang, "Design of Ultra-Low-Power Analog-to-Digital Converters", Linköping Studies in Science and Technology. Thesis, No. 1548, 2012.

[12] Walt Kester, "ADC Architectures II: Successive Approximation ADCs", http://www.analog.com/media/en/training-seminars/tutorials/MT-021.pdf.

[13] J. L. McCreary and P. R. Gray, "All-MOS charge redistribution analog-to-digital conversion techniques. I," in IEEE Journal of Solid-State Circuits, vol. 10, no. 6, pp. 371-379, Dec. 1975. doi: 10.1109/JSSC.1975.1050629

[14] T O Anderson optimum control logic for successive approximation analog to digital convertorhttp://tmo.jpl.nasa.gov/progress report2/XIII/XIIIW.PDF.

[15] van Elzakker, M.; van Tuijl, E.; Geraedts, P.; Schinkel, D.; Klumperink, E.; Nauta, B., ”A 1.9W 4.4fJ/Conversion-step 10b 1MS/s ChargeRedistribution ADC,” Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International , vol., no., pp.244,610, 3-7 Feb. 2008.

[16] Sauerbrey, J.; Schmitt-Landsiedel, D.; Thewes, R., "A 0.5-V I-W successive approximation ADC," Solid-State Circuits, IEEE Journal of , vo1.38, nO.7, pp.1261,1265, July 2003 doi: 1O.1109/JSSC.2003.813217.

[17] Wenliang Geng; Guoxing Wang; Kuan-Ting Lin; Kea-Tiong Tang, "A IO-bit IkS/s-30kS/s successive approximation register analog-to-digital converter for biological signal acquisition," Biomedical Engineering and Informatics (BMEI), 2013 6th International Conference on , vol., no., pp.403,407, 16-18 Dec. 2013.

[18] R. J. Baker, H. W. Li, and D. E. Boyce, CMOS Circuit Design, Layout and Simulation, New York, IEEE Press, 1998.

[19] CHEN, Yanfei, “A Study on Energy-and-Area-Efficient Charge Redistribution Successive Approximation Analog-to-Digital Converters” Keio university.

[20] K. Yadav, P. Patra and A. Dutta, "A 43-nW 10-bit 1-kS/s SAR ADC in 180nm CMOS for biomedical applications," 2015 IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (PrimeAsia), Hyderabad, 2015, pp. 21-25.

[21] Y. Chen, S. Tsukamoto and T. Kuroda, “A 9b 100MS/s 1.46mW SAR ADC in 65nm CMOS,” IEEE Asian Solid-State Circuits Conference Dig. Tech. Papers, 2009, pp. 145-148.

[22] B. P. Ginsburg and A. P. Chandrakasan, "500-MS/s 5-bit ADC in 65-nm CMOS With Split Capacitor Array DAC," in IEEE Journal of Solid-State Circuits, vol. 42, no. 4, pp. 739-747, April 2007.

[23] Y. K. Chang, C. S. Wang, and C. K. Wang, “A 8-bit 500 KS/s low power SAR ADC for bio-medical application,” in IEEE ASSCC Dig. Tech. Papers, Nov. 2007, pp. 228–231.

[24] C. C. Liu, S. J. Chang, G. Y. Huang and Y. Z. Lin, "A 10-bit 50-MS/s SAR ADC With a Monotonic Capacitor Switching Procedure," in IEEE Journal of Solid-State Circuits, vol. 45, no. 4, pp. 731-740, April 2010.

[25] S. Jiang, M. A. Do, K. S. Yeo, and W. M. Lim, “An 8-bit 200-MSample/s pipelined ADC with mixed-mode front-end S/H circuit,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 55, no. 6, pp. 1430–1440, Jul. 2008.

[26] C. C. Liu, S. J. Chang, G. Y. Huang, and Y. Z. Lin, “A 0.92 mW 10-bit 50-MS/s SAR ADC in 0.13 m CMOS process,” in IEEE Symp. VLSI Circuits Dig., Jun. 2009, pp. 236–237.