Reconfigurable low power robust pipeline ADC for Biomedical applications

By

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Under the guidance of

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A Dissertation Submitted to
Indian Institute of Technology Hyderabad
In Partial Fulfilment of the Requirements for
The Degree of Master of Technology

Department of Electrical Engineering
June, 2016

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Approval Sheet

This thesis entitled "Reconfigurable low power robust pipeline ADC for Biomedical applications" is approved for the degree of Master of Technology from IIT Hyderabad.

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Abstract

Demand for high-performance analog-to-digital converter (ADC) integrated circuits (ICs) with optimal combined specifications of resolution, sampling rate and power consumption becomes dominant due to emerging applications in wireless communications, broad band transceivers, digital-intermediate frequency (IF) receivers and countless of digital devices. This research is dedicated to develop a pipeline ADC design methodology with minimum power dissipation, while keeping relatively high speed and high resolution.

Pipeline ADC is a mixed-signal system, which consists of sample and hold amplifier (SHA), sub-ADC, multiplying digital-to-analog Converter (MDAC) and bandgap voltage reference, comparator, switch-capacitor circuits and biasing circuits. This project links all the specifications between the system levels and circuit levels together. With this design flow, if the overall ADC specifications are given, such as resolution, sampling rate, voltage supply and input signal range, all the sub-block circuitry specifications are achieved.

This paper studies all the sub-block circuits of pipeline ADC first, and then come up with all the constraints and limitations for all the circuitry in term of speed and noises. Then a system level speed and power trade off consideration is explored in order to optimize the overall performance.

As verification of the proposed design methodology, a 10-bit pipeline analog-to-digital converter prototype is developed in commercial UMC 180nm CMOS technology: using op-amp sharing pipelined ADC with a switch-embedded dual-input MDAC for different sampling speeds such as 40MHZ, 50MHZ and 60MHZ.

Contents

Chapter 1

Introduction

1.1 Motivation of ADC

In the past three decades, the world has seen a rapid growth and evolution of integrated circuit (IC) technologies to cope up with the ever growing complexities of signal processing systems. These ICs are used in a wide array of application areas like communications, speech processing, sonar, radar, medical imaging, instrumentation, consumer electronics and electronics warfare. Signals encountered in most of the cases are continuous in nature. Obviously, in order to get the advantages of the modern digital signal processing, it is essential to convert these continuous time signals to discrete, binary signals. It is this interface between continuous time domain and discrete time domain, where the role of a high performance Analog to Digital Converter (ADC) comes into play.

ADCs in general can be classified depending on their three major performance metrics, viz: Sampling Speed, Resolution and Power Consumption. The Sampling Speed of an ADC is the measurement of number of samples it can process in a given frame of time. It is generally expressed in Samples Per Second. The Resolution is the measure of its accuracy and is expressed in terms of ENOB or Effective Number of Bits. ENOB is determined from the SNDR (Signal to Noise and Distortion Ratio) data of an ADC. Last but not the least, the Power Consumption of an ADC is a key metric in todays context of low power applications especially in areas like consumer electronics and bio-medical applications.

1.2 Comparison of architectures

To compare different architectures, a figure of merit must be formulated which would give a quantitative measure of an ADC. Although there are number of

performance metrics which characterize an ADC, a suitable figure of merit can be derived using three of its most important metrics. Sampling speed (fsample), resolution (ENOB) and power dissipation (Pdis) of an ADC forms this figure of merit F [9] according to the following equation.

$$F = \frac{Pdis}{Fsamp.2^{ENOB}} \quad (1.1)$$

Flash architecture can work at a very high sampling rate. This architecture is of direct conversion type. An N-bit ash ADC contains 2N - 1 number of comparators, all working in parallel. This parallelism is the key to its very high sampling rate. Although as the resolution requirement of the flash ADC increases, the number of comparators required becomes astronomical and the power and area budget goes beyond manageable limits. Also, mismatched delays occurred at the outputs of the parallel working comparators produce erroneous codes also known as sparkle codes thus reducing the accuracy. Flash ADCs are primarily used in disc drive read channel circuits, Local Area Network (LAN) interfaces, where typically high speed (fsample=500 MHz to 2 GHz) and lower resolution ADCs are required.

In order to alleviate the problems arising from a flash architecture, folding and folding-interpolating architectures are often used. Requirement of comparators are reduced to a great extent by folding the input signal and dividing it into multiple smaller sub-ranges. A folding-interpolating architecture is also capable of very high sampling speed due to its open loop nature of operation.

A $\sum\Delta$ ADC is an oversampled data converter capable of producing very high resolution (~ 20 bits) at a low sampling speed. This architecture contains a modulator followed by a digital filter to produce the high resolution digital output. A very low area and power budget are possible using this architecture due its simplicity. Consequently, these data converters find themselves extensively used in bio-medical applications where highly accurate data is required at essentially low power consumption.

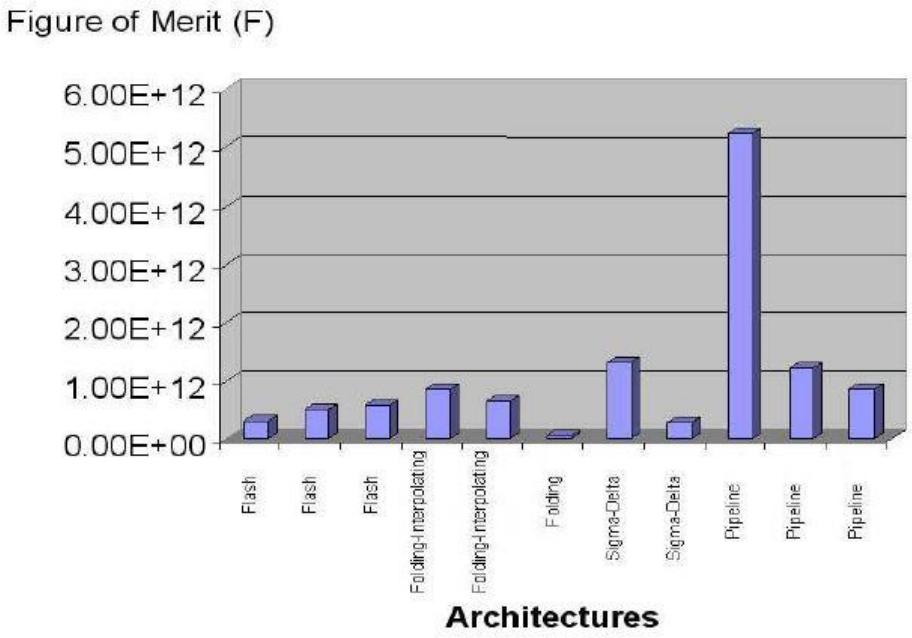


Figure 1.3: Comparison of Figure of Merit of different ADCs

Finally, pipeline architecture can be said as being the most optimized architecture compared to the above mentioned ones. This type of ADC contains several cascaded stages, with each stage converting the incoming signal to a lower resolution digital signal to determine the residue. Then it amplifies the residue to full scale range and feeds it to the next stage for similar processing. Pipeline ADCs are mostly used in radio receivers, medical instrumentations like Ultra-sonography (USG) machines, and consumer electronics like flat-panel TV.

Fig.1.3 displays the Figure of Merit (F) plot of different architectures of ADC. A good trade-off is possible between speed, resolution and power while using pipeline architecture and consequently they produce very high values of F.

ADC Topology	F Conversion	Resolution	Comments
SAR	≤ 4Msps ≤ 1.25Msps	≤ 16-bit ≤ 18-bit	Simple operation, low cost, low power.
Delta-Sigma	≤ 4ksps ≤ 4Msps ≤ 10Msps	≤ 31-bit ≤ 24-bit ≤ 16-bit	Moderate cost.
Pipeline	≤ 200Msps ≤ 250Msps ≤ 550Msps	≤ 16-bit ≤ 14-bit ≤ 12-bit	Fast, expensive, higher power requirements.

1.3 Organization of Thesis

In Chapter 2, each and every block of pipeline ADC is explained. Chapter 3 will highlight the design issues of each block of pipeline ADC. In Chapter 4, the OTA specifications are explained clearly. In Chapter 5, opamp sharing and reconfigurability in terms of sampling rate and resolution is detailed. In chapter 6, Flash ADC architecture is explained. In chapter 7, low power and non opamp based MDAC techniques are explained. Finally in chapter 8, simulation results of all blocks are presented.

CHAPTER 2

Theory of pipeline ADC

Pipeline ADC uses two or more steps of sub ranging. First, a coarse conversion is done. In a second step, the difference to the input signal is determined with a digital to analog converter (DAC). This difference is then converted finer, and the results are combined in a last step. This can be considered a refinement of the successive approximation ADC wherein the feedback reference signals consists of the interim conversion of a whole range of bits (for example, four bits) rather than just the next-most significant bit. By combining the merits of the successive approximation and flash ADCs this type is fast, has a high resolution, and only requires a small die size.

2.1 Working Principle:

Pipeline ADC actually evolves from cyclic ADC [10] which converts the incoming analog signals in a number of time steps. A cyclic ADC has a single processing stage which performs the analog to digital conversion in, say, m number of clock cycles. In a pipeline ADC however, m number of such processing stages are cascaded to perform the conversion. So, in order to understand the working principle of a pipeline ADC, the algorithm working behind it must be grasped. Fig.2.1 shows a typical pipeline ADC block diagram. Basic idea of a pipeline ADC is to pre-process the incoming analog signal before converting it into digital domain.It contains a sub-ADC, a coarse DAC, an analog substractor and an amplifier. Coarse DAC, substractor and the amplifier are collectively called Multiplying Digital to Analog Converter (MDAC).

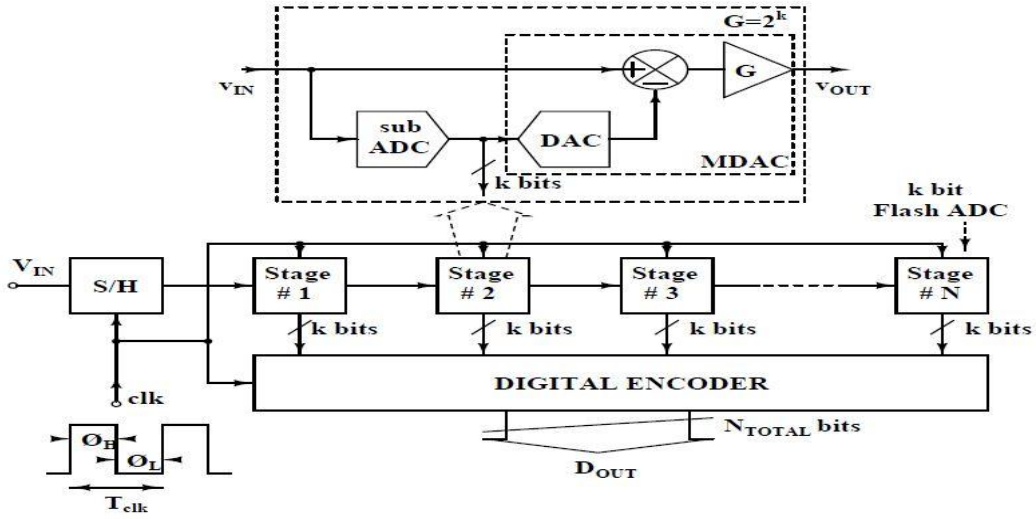


Figure 2.1: Block diagram of a pipeline ADC

The pipeline algorithm can be described as the combination of following set of steps.

Step 1: Input signal VIN is sampled by the Sample-and-Hold amplifier and the held value gets converted to digital output of k bits by the sub-ADC of the 1st pipeline stage. This sub-ADC, which is in principle a ash ADC, contains 2^k-1 number of comparators. These digital output codes are thermometric in nature. Encoders are required to convert these codes to binary codes.

Step 2: Digital output of k bits are actually digital outputs generated from a single stage. An analog signal is then recovered from these k bits using a coarse DAC.

Step 3: The coarse output from this DAC is then subtracted from the original analog input signal to determine the residue. Assuming a full scale voltage of VFS, the residue signal achieves a dynamic range of VFS/2^k .

Step 4: In order to convert this signal to the full scale range, it must be multiplied by an amplifier of gain 2^k.

Step 5: Next stage also works in the similar fashion, thus producing another set of k digital bits. But digital output of subsequent stages are delayed by ixTclk = i/fclk, where i = 1 to N.

Step 6: Once digital output of all the stages are obtained, they are properly aligned and time synchronized in order to generate the final set of digital output.

The principle of sub-ranging ADC can be pushed to the limit of having only one bit per stage. At this point, each flash ADC is nothing more than a simple comparator; also, the data is transferred in a pipeline fashion: when the data is sent to the second stage, another sampled data is fed to the first stage; the result is a latency delay equal to the number of stages. Since the pipeline ADC is pipelining the subranging structure, and the binary search in the sub-ADCs runs just as the mathematic division, the first stage decides the MSBs and the last stage sets the LSBs. The MSBs divide the full reference range, while LSBs divide the sub reference range. The relationship between MSBs and LSBs is revealed in Figure 2.2.

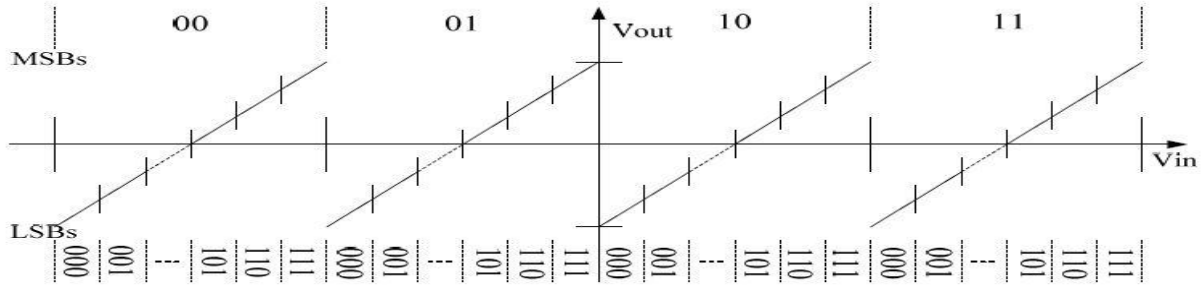


Figure 2.2 Pipeline ADC Transfer Curve.

A Pipeline ADC consists of a cascade of stages, each of which contains a low resolution ADC, DAC and amplifier, which successively convert the analog input into its digital representation, while processing the data in a pipe-lined manner. Pipeline ADCs are commonly used for power-efficient high-speed conversion of wide bandwidth input signals (e.g. 10 to 100 MHz). The ADC sampling frequency is usually the Nyquist frequency or lower using small OSRs (e.g. 2 or 4) and the ADC output code resolution is typically between 8 and 14-bit.

Each stage performs data conversion in sampling and holding modes serially. The sampling and holding modes interleave between two adjacent stages and the

digital output is valid after some clock cycles, called latency time, decided by the number of stages. This process is illustrated in Figure 2.3(a). Because each sample must propagate through the entire pipeline before all its associated bits are available for combining in the digital-error-correction logic, data latency is associated with pipelined ADCs. In the example in Figure 2.3(b), this latency is about seven cycles.

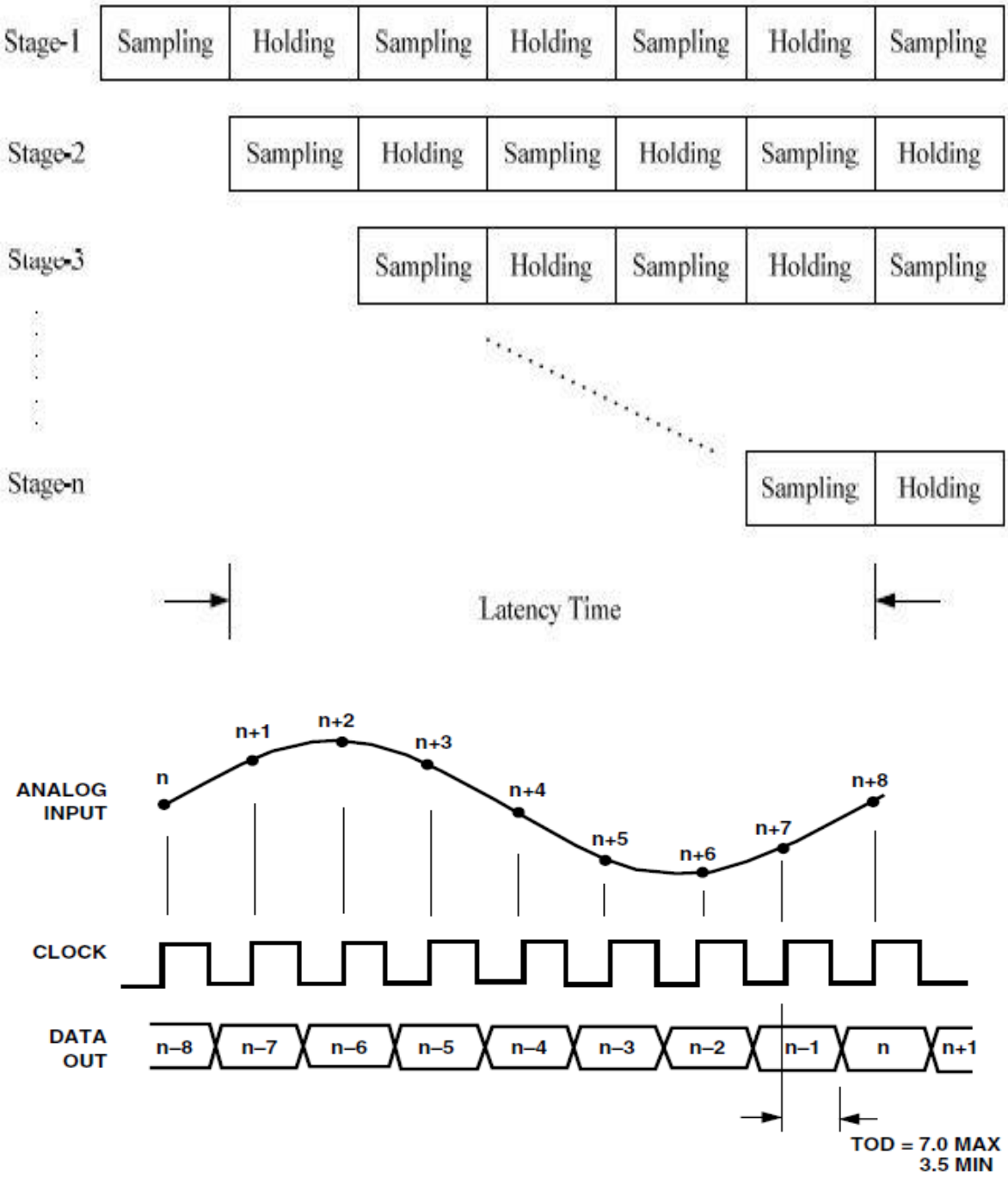


Figure 2.3 (a) Stage Operation Modes in Pipeline ADC (b) data latency in pipeline ADC.

This timing scheme of the pipeline ADC is built up by the sample and hold circuit in each stage. During sampling mode, the switch controlled by the sampling clock is connected to the residue generated from the preceding stage and the signal is sampled on the sampling capacitor. When the hold clock comes, the switch is turned off and the signal stored on the sampling capacitor on one hand is converted to the thermometer codes by the sub-flash ADC, on the other hand, subtracts the estimated analog signal that is re-constructed by the D/A converter, to create the new residue as the input signal of the following stage. The thermometer codes from each stage are encoded to the binary ones and latched and added together to form the final m-bit digital output (where m is the resolution of the pipeline ADC). The detailed pipeline architecture is shown in Figure 2.4.

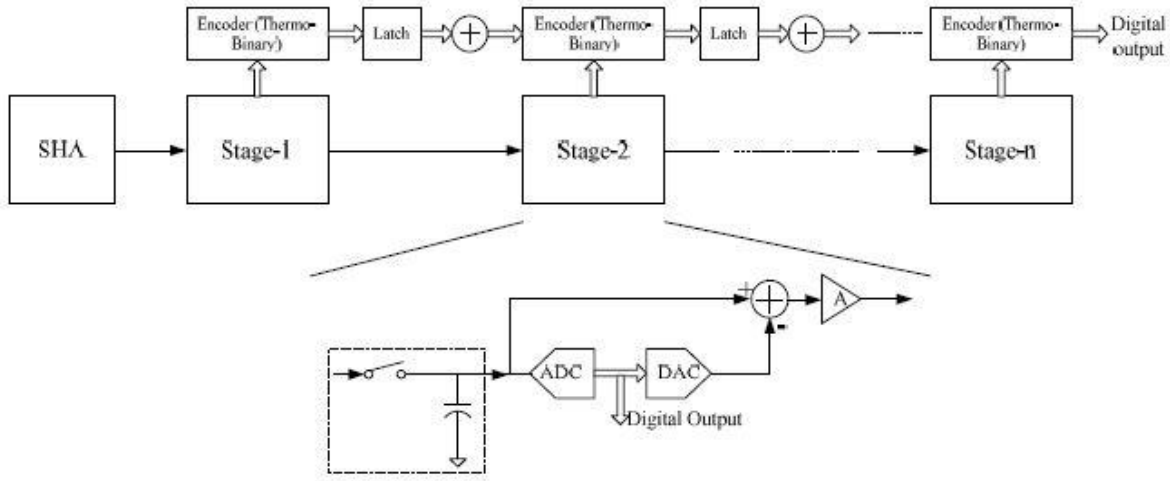


Figure 2.4 Detailed Pipeline ADC Architecture.

2.2 Stage resolution:

The most obvious way to implement the 10-bit resolution would be a two staged pipeline with 5-bit resolution in each stage. This will result in a very low latency, since the signal only has to pass through two stages. However since a predefined latency isn't a big concern in most applications, the advantage of low latency wouldn't compensate for the fact, that the gain bandwidth of the multiplier in each stage has to be very large, in order to realise a multiplication by 32 . Since it is generally hard to realise a high-gain high-speed amplifier, it would be more sensible to reduce the resolution of the stages.

The most well know implementation of a pipelined ADC is with 3-bit stages. This could be done with three 3-bit stages and a small 1-bit ADC at the end. This however still has the issue with the speed requirements of the multiply by 8, even though it is better than the multiply by 32. In relation to area consumption the 5-bit realisation has

smaller overall area consumption, though the individual stage is significantly larger. This is mostly because of the increase in the number of comparators in the subADC component. The overall power consumption will be larger with more stages. It is therefore counterproductive in relation to the implementation of a low power design, to have more stages. To gain more speed the resolution of the stages has to be reduced.

A solution to the multiplier problem is to lower the resolution of each stage to 1.5-bit. Then the 1.5-bit stage is basically a 1-bit converter with some redundancy build into. Digital error correction is used in order to compensate for inaccuracies in the components, and give a larger tolerance. There is only need for a multiply-by-2 with this 1.5-bit structure. This will significantly lower the requirements for the amplifier, and thereby reducing the complexity of the implementation. Each stage will not take up much area on the wafer.

2.3 1.5bit Pipeline-stage structure:

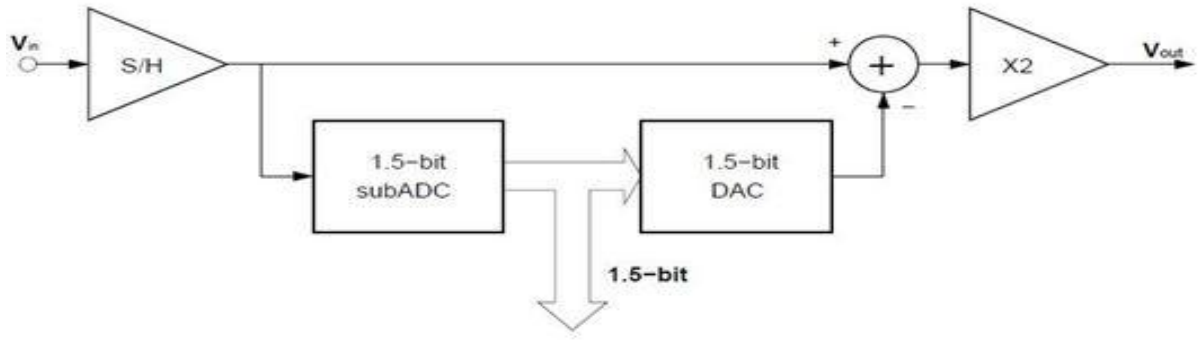


Figure 2.5 Traditional structure of 1.5bit pipeline stage

Traditional structure of 1.5bit pipeline stage is shown in Figure 2.5. This structure contains a S/H, an ADC, a DAC, a substractor and a multiply-by-2 amplifier. The input signal will first be sampled by the S/H, then passed on to the subADC, where the signal will be converted to a 1.5-bit digital signal. This digital signal is the binary output of the stage. Besides being the output signal the 1.5-bit signal is also passed on to a DAC. This DAC converts the signal back into a analog signal. By doing so, the new analog signal is equivalent to what the low resolution subADC detected the incoming signal to be. This new analog signal is then subtracted from the original signal. The residue of the subtraction is then multiplied by a factor of 2 and passed on as a analog output. In turn this means that the signal has to pass all elements, before it is ready for the next stage, within the short period of 1/50*10^6 = 20*ns*.

This traditional structure can be improved by simplifying the structure, and thereby reducing the latency of the stage and also lowering the power consumption. This

is done by combining the S/H circuit, the substractor, the multiplier and the DAC into a Multiplying DAC (MDAC) block which is shown in Figure 2.6.

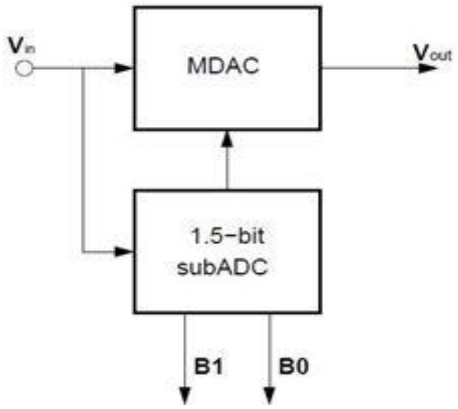


Figure 2.6 New structure of 1.5bit pipeline stage

With this new structure the signal will not have to pass through both the operational amplifier in the S/H and in the multiply-by-2, it also lowers the area consumption of each stage. With this change in structure, it is necessary to add a S/H circuit in front of the first stage in the overall structure, to sample the incoming signal.

2.4 1.5-bit sub-ADC:

The 1.5-bit sub-ADC is based upon the flash converter principle. To realise a 1.5-bit flash converter there will be needed two comparators and some digital logic as shown in Figure 2.7.

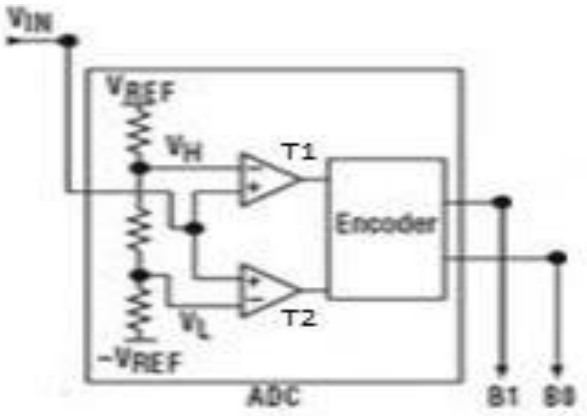


Figure 2.7 1.5 bit sub ADC

2.5 Encoder:

The purpose of the encoder is to translate the output of the two comparators into a 2-bit binary code. Since it is a 1.5-bit converter, there are three different output

combinations, since 2-bit binary can represent 4 states, the logic design will therefore end up with a unknown state. The needed translation can be seen in Table 2.1.

Sub-ADC Input(VIN)	T1	T2	B1	B0
VIN ≤ Vcm-Vref/4	0	0	0	0
Vcm-Vref⁄4 ≤VIN≤ Vcm+Vref⁄4	0	1	0	1
VIN ≥ Vcm+Vref⁄4	1	1	1	0

Table 2.1 Truth table of encoder

2.6 1.5 bit DAC (3:1 mux):

10 bit digitally corrected pipeline ADC has been designed, consisting eight stages generating 1.5 bits and the last stage generating 2 bits. MDACs of these stages with 1.5 bits resolution require three different reference voltages VCM + Vref, VCM and VCM - Vref according to the sub-ADC output. Selecting one of these reference voltages require a 3:1 analog multiplexer as shown in Figure 2.8. Switches used in these circuits are CMOS transmission gate switches, which are capable of reducing distortions caused by charge injection and clock feed-through. Control signals of this MUX are comparator outputs D0 and D1. These outputs are thermometric in nature. So, a truth table can be generated for the 3:1 MUX with three input terminals In1, In2, In3 and two control signals D0, D1 as shown in Table 2.2.

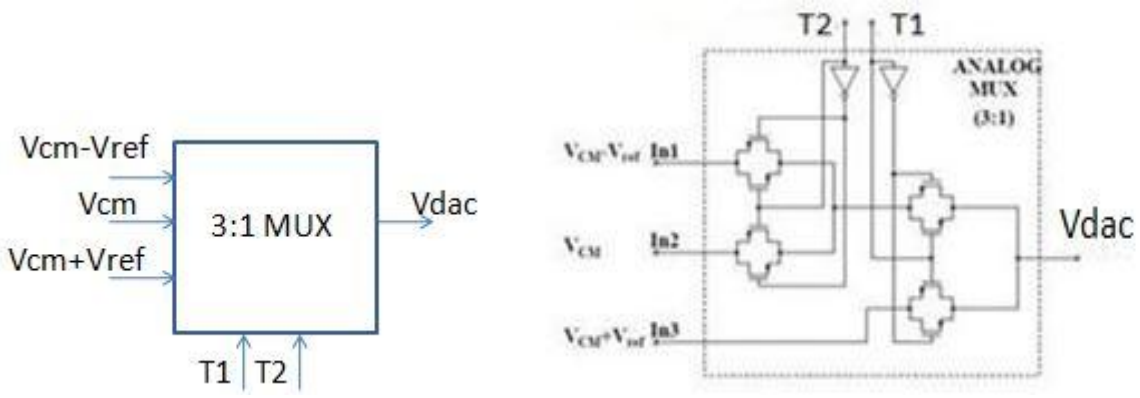


Figure 2.8 3:1 Analog Multiplexer

T1	T2	Vdac
0	0	Vcm-Vref

0	1	Vcm
1	1	Vcm+Vref

Table 2.2 Truth table of 3:1 Multiplexer

2.8 1.5bit MDAC:

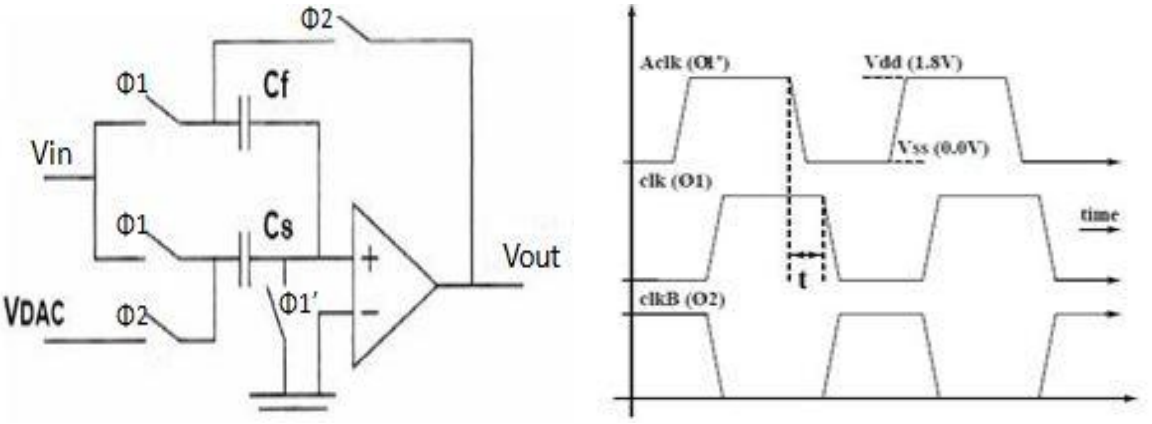


Figure 2.9 Structure of 1.5bit MDAC

The MDAC of above Figure 2.9 is shown single ended for simplicity, although in practice fully differential circuitry is commonly used to suppress common-mode noise. 1.5 bits/stage architecture has one of three digital outputs, thus the DAC has three operating modes:

Vdac = Vcm: stage input is between –Vref/4 and Vref/4.

During Φ1: $Q_{Cs}=C_sV_{in}$, $Q_{Cf}=C_fV_{in}$

During Φ2: C_s is discharged, thus by charge conservation: $C_sV_{in} + C_fV_{in} = C_fV_{out}$ (noting negative feedback forces node V_p to a virtual ground). Thus

$Vout = \frac{Vin(Cs+Cf)}{Cf}$ ➔ if $C_s=C_f$, then: $V_{out}=2V_{in}$

Vdac = Vcm + Vref: Input exceeds Vref/4, thus subtract Vref/2 from input

During Φ1: $Q_{Cs}=C_sV_{in}$, $Q_{Cf}=C_fV_{in}$

During Φ2: C_s is charged to V_{ref}, thus by charge conservation: $C_sV_{in} + C_fV_{in} = C_sV_{ref} + C_fV_{out}$

$Vout = Vin\left(\frac{Cs+Cf}{Cf}\right) - Vref\left(\frac{Cs}{Cf}\right)$ ➔ if $C_s=C_f$, then: $V_{out}=2V_{in}-V_{ref} =2(V_{in}-V_{ref}/2)$

Vdac = Vcm – Vref: Input below -Vref/4, thus add Vref/2 to input

During Φ1: $Q_{Cs}=C_sV_{in}$, $Q_{Cf}=C_fV_{in}$

During Φ2: C_s is charged to $-V_{ref}$, thus by charge conservation

$C_sV_{in} + C_fV_{in} = C_s(-V_{ref}) + C_fV_{out}$

$Vout = Vin\left(\frac{Cs+Cf}{Cf}\right) + Vref\left(\frac{Cs}{Cf}\right)$ ➔ if $C_s=C_f$, then: $V_{out}=2V_{in}+V_{ref}=2(V_{in}+V_{ref}/2)$

Signal dependent charge injection is minimized by using bottom plate sampling, where the use of an advanced clock Φ1p [1], makes charge injection signal independent. A non-overlapping clock generator is thus required for the MDAC.

Stage input V_{in}	Level	B_1	B_0	DAC output	Stage output V_{out}
$V_{in} < V_L$	Low	0	0	$-V_{ref}$	$2V_{in} + V_{ref}$
$V_L < V_{in} < V_H$	Mid	0	1	0	$2V_{in}$
$V_{in} > V_H$	High	1	0	$+V_{ref}$	$2V_{in} - V_{ref}$

2.9 Nonoverlap clock generator:

Switched-capacitor circuits need clocking schemes to turn on/off its switches to achieve a specific function. Most data converters rely on a special scheme that permits the signal acquired during the sampling phase to be transferred and amplified without loss. In other words, it is imperative that no charge is destroyed or lost between the sampling and amplification phases. To achieve this, the overlapping time between phases must be zero. This is accomplished by a nonoverlapping clock generator.

Nonoverlapping clock generator has one clock input and two phases with 180◦ phase shift are provided at the output. The nonoverlapping time is controlled by the delay of the input NAND gate and the two inverters (before the feedback). To increase this time, more inverters (in an even number) can be added.

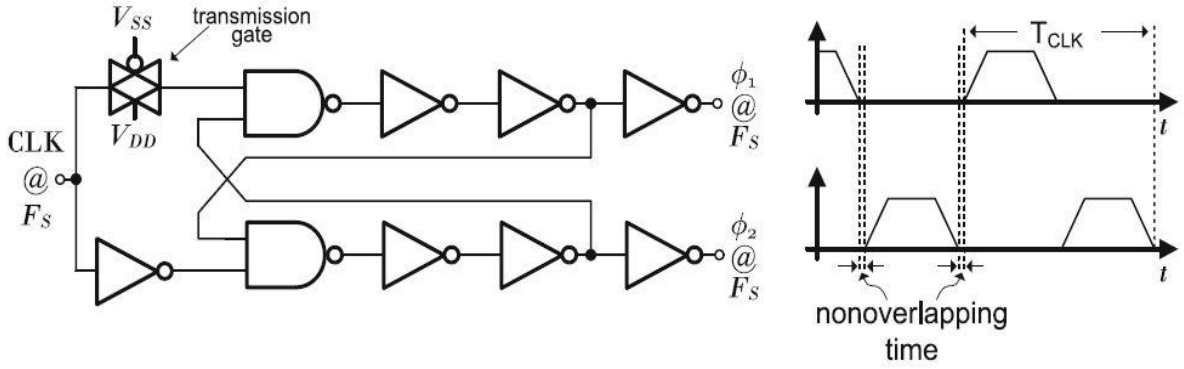


Figure 2.10: Nonoverlapping clock generator

2.10 Delay and digital error correction:

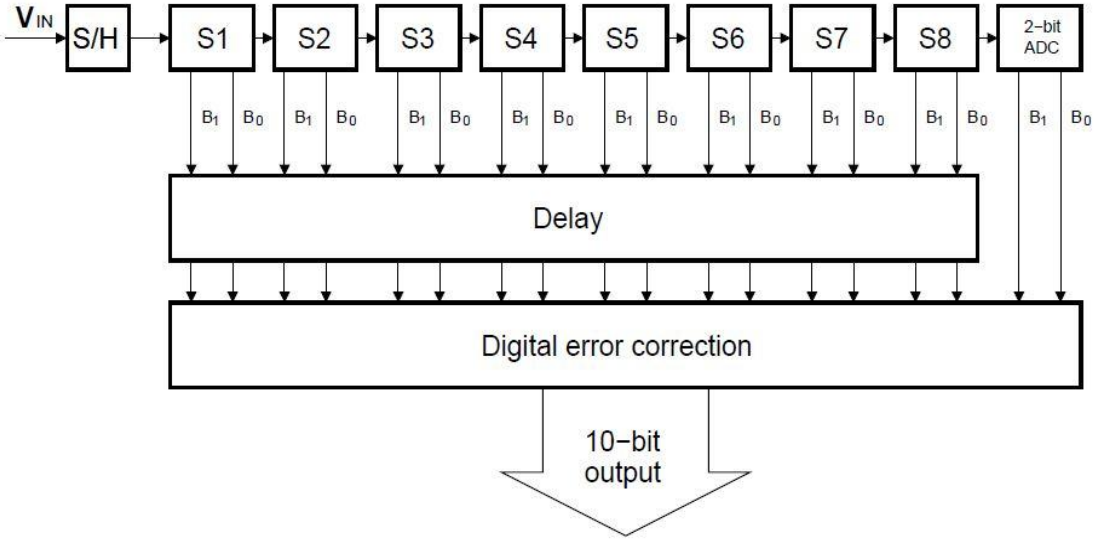


Figure 2.11 Block diagram of 10bit pipeline ADC

The purpose of the delay is to ensure that the output of the different stages are stored, until all of the stages has analysed the signal, and then deliver it to the digital error correction component as shown in Figure2.11. This can be achieved with digital logic, since the bit values either are logic high or logic low. The delay components function is to store the digital signals from the different stages, and then deliver them to the digital error correction when the input signal has passed through all the stages. This can be implemented with different components, but the straightest forward is to use DFF. The DFF is a clocked circuit that samples a digital input signal on, typically, at raising edge on the clock.

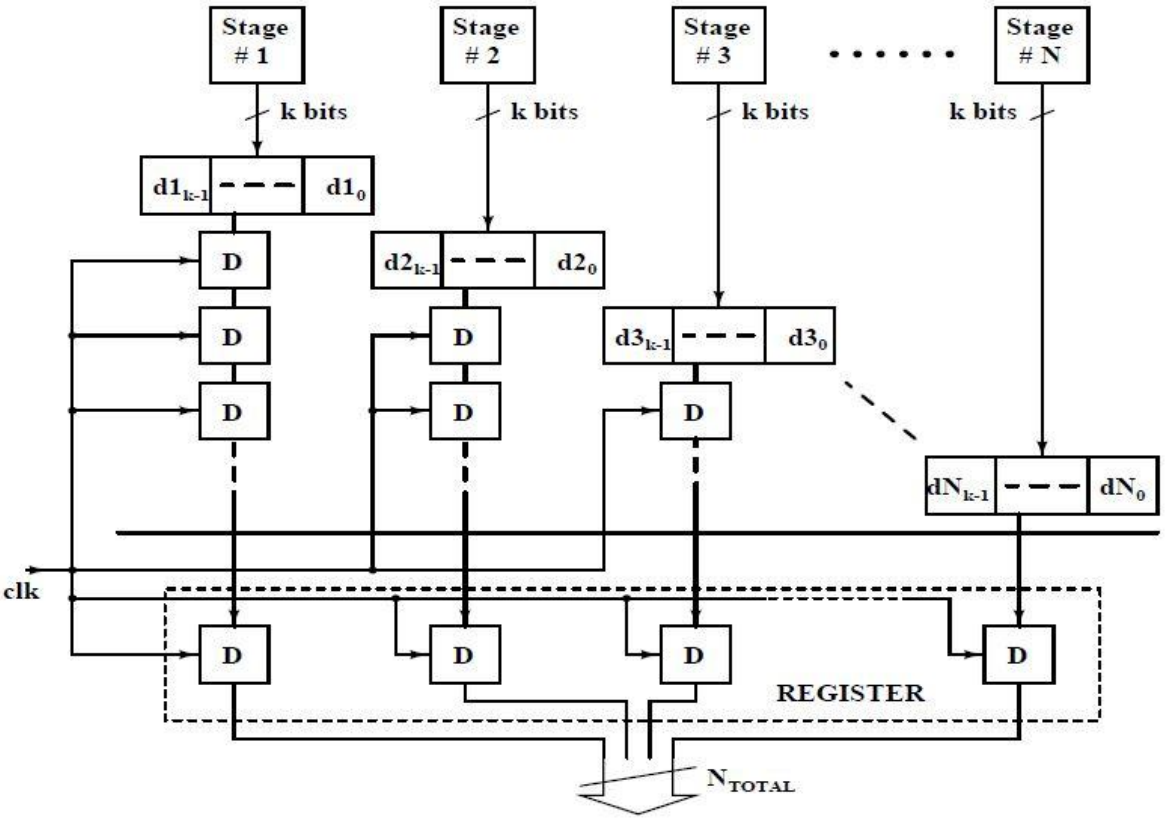


Figure 2.12: Digital scheme of the pipeline ADC

As Figure.2.12 shows it only requires proper alignment and synchronization. Delay elements D are D-F/Fs producing T_{clk} delay. A final register synchronizes all the digital bits to generate the final digital output.

2.11 Digital error correction: Redundant Signed Digit (RSD)

Due to the non-linearity of the comparators used in the sub-ADC and inconsistent reference voltage generation, threshold levels of the comparators become erroneous with offset. Such offset voltages shift the decision levels of the sub-ADC and transfer characteristics gets distorted as shown in Fig.2.13 (a). As the dynamic range of the analog output goes beyond the limitations, output saturates and faulty codes occur. To remedy this error, the digital correction method [11], [12], [13] is introduced. Digital error correction is implemented by reducing the stage gain Gi by half (Fig.2.13 (b)). This gives a margin of error of $\pm$LSBi/2. A two stage pipeline ADC with both having a stage resolution of 2 bits is now considered, i.e., n1 = n2 = 2, N1 = N2 = 4 and G1 = N1/2 = G2 = N2/2.

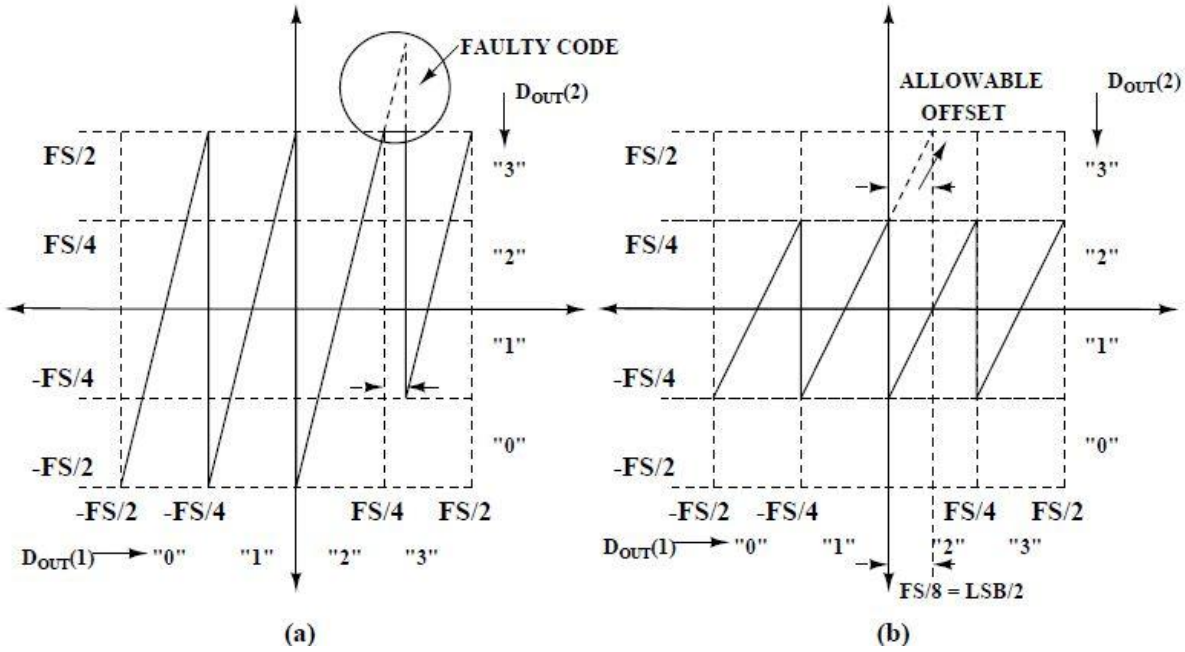


Figure 2.13: Reduction of gain to allow offset error

$$D_{OUT} = 2 \triangleright D_{OUT}(1) + D_{OUT}(2) \qquad (2.1)$$

Figure 2.14 shows that unlike the normal pipeline stages, reduced gain pipeline stages has a digital output scheme which is a little more complicated than the normal one. In this case, LSB of the 1st stage must be aligned with the MSB of the 2nd stage and carry propagation must also be considered while doing the digital addition.

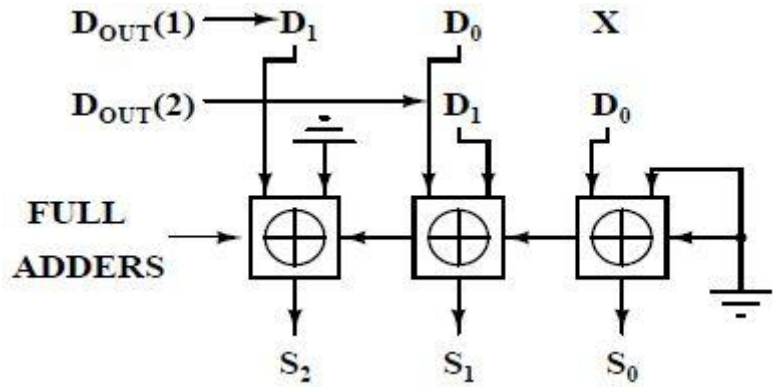


Figure 2.14: Digital output alignment after reduction of gain

Bit alignment scheme shown in Fig.2.14 suggests that resolution of the ADC must now be 3 bits. So, the maximum possible codes generated by the two stages combined must be $2^3 = 8$ in order to resolve them by 3 bits. But from Fig.2.13 we see that Maximum possible codes of stage 1 and stage 2 are 3 and 2 respectively whereas minimum codes are 0 and 1. Putting these values in Eq.2.1 it is found that the two stage ADC will now have a range of output codes from 1 to 2.3 + 2 =8≡ 1000. Although there are 2^3 number codes, to describe the maximum code in binary form will require 4 bits. To remove this

conflict, coding of the second stage must be modified by introducing negative numbers (Fig.2.15). Since second stage digital outputs are now (-1, 0, 1, 2), minimum and maximum possible output codes of the ADC are 0 and 7 respectively. These codes now can be resolved by 3 bits.

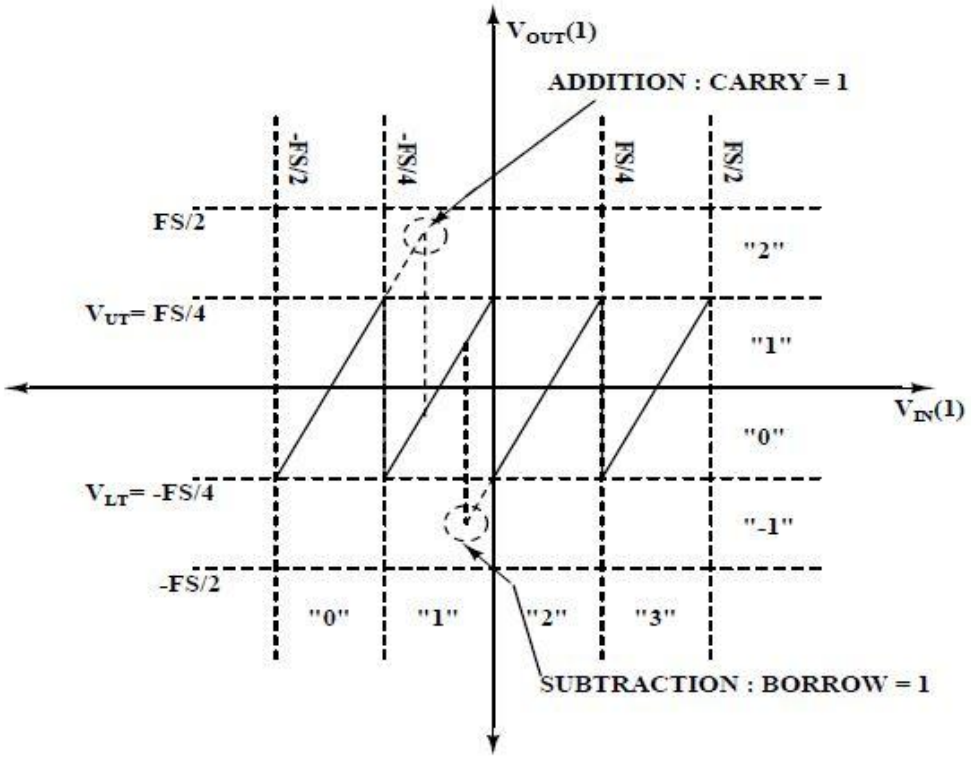


Figure 2.15: Coding scheme introducing negative numbers

But introducing this new coding scheme has its own difficulties. As long as the output of the 1st stage does not exceed VUT = FS/4 and does not go below VLT = -FS/4, digital addition will not involve any carry propagation. But once VOUT (1) crosses VUT, a carry will be generated and must be added. And if VOUT (1) < VLT then the carry generated must be subtracted. This makes the digital operations complicated. To alleviate such complications, transfer characteristics of the 1st stage are modified according to Fig.2.16 (b). Here, an offset of LSB/2 is given to the decision levels of the sub-ADC and an offset of -LSB/2 is given to the sub-DAC. In this case, the coding scheme will not require negative numbers anymore, as is evident from Fig.2.16(b) and 3 bits will be sufficient to describe the ADC output. Functional block diagram of a stage employing digital redundancy is shown in Fig.2.16 (d).

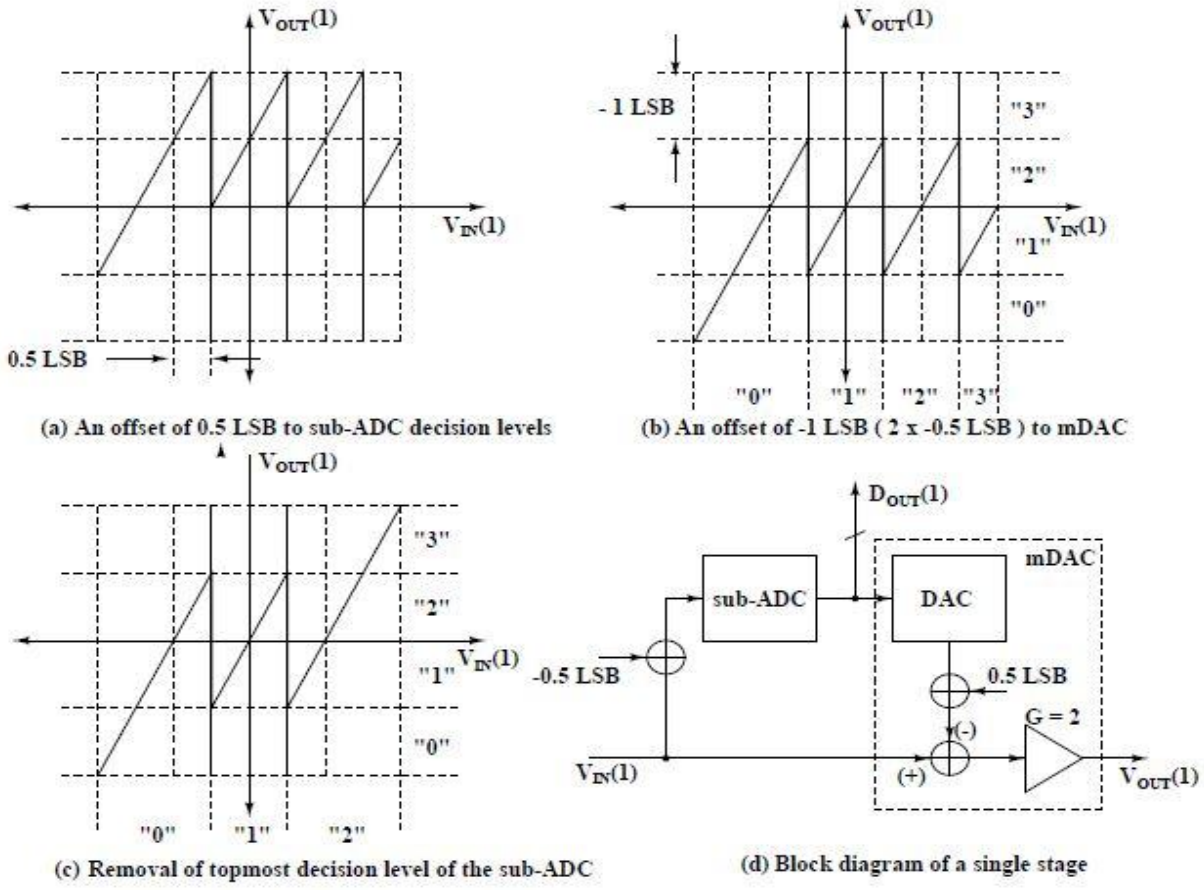


Figure 2.16: Redundant Signed Digit (RSD)

Interestingly, Fig.2.16(c) shows that by removing one decision level of the sub-ADC, maximum possible digital output code remains 7. This means a comparator of the sub-ADC can be removed which will be advantageous as far as savings of hardware, chip area and power consumption is concerned.

In this way, a digital redundancy of 0.5 bit is incorporated in the stage since out of four possible codes (0,1,2,3) only (0,1,2) are required to express the digital output codes of the ADC. So, instead of having a resolution of 2 bits (ni = log2 Ni) per stage a resolution of 1.58 bits (ni = log2(Ni-1)) is achieved. Since a single bit is extracted out of this 1.5 bits, for a total resolution of nTOT bits, nTOT-1 number of stages are required assuming that the last stage is a standard flash converter.

In a nut-shell, applying digital correction technique reduces the accuracy requirement of the sub-ADC by a great extent. This scheme reduces the amplifier gain of each stage by half, thus extending the margin of error of the sub-ADC thresholds by an amount of LSB/2. Advantage of using digital correction lies in reducing the number of comparators of the sub-ADC from 3 to 2. Not only the comparator thresholds got a margin of

error of LSB/2, reduction of comparators means less capacitive loading of the amplifier output and savings in terms of die area and power consumption. Digital output of an N stage pipeline ADC, with first N-1 stages applying digital correction, can be formulated as,

$$DIG_{OUT} = \sum_{i=1}^{N-1} \frac{M_N}{M_i} D_{OUT}(i) \prod_{j=i}^{N-1} G_j + D_{OUT}(N)$$

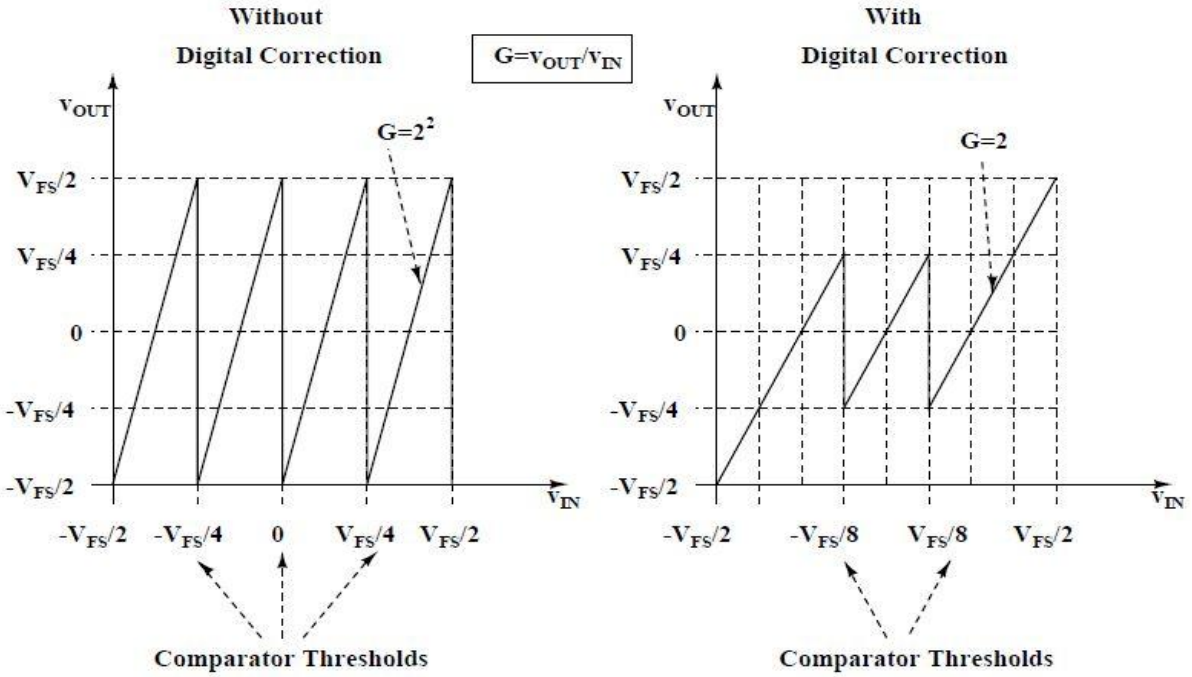


Figure 2.17: Transfer curve of the ith stage

For an ADC with an overall resolution of 10 bits, with each stage employing digital correction and generating 1.5 bits, above expression can be expanded as,

$DIG_{OUT} = 2^8 D_{OUT}(1) + 2^7 D_{OUT}(2) + 2^6 D_{OUT}(3) + 2^5 D_{OUT}(4) + 2^4 D_{OUT}(5) + 2^3 D_{OUT}(6) + 2^2 D_{OUT}(7) + 2 D_{OUT}(8) + D_{OUT}(9)$ (2.2)

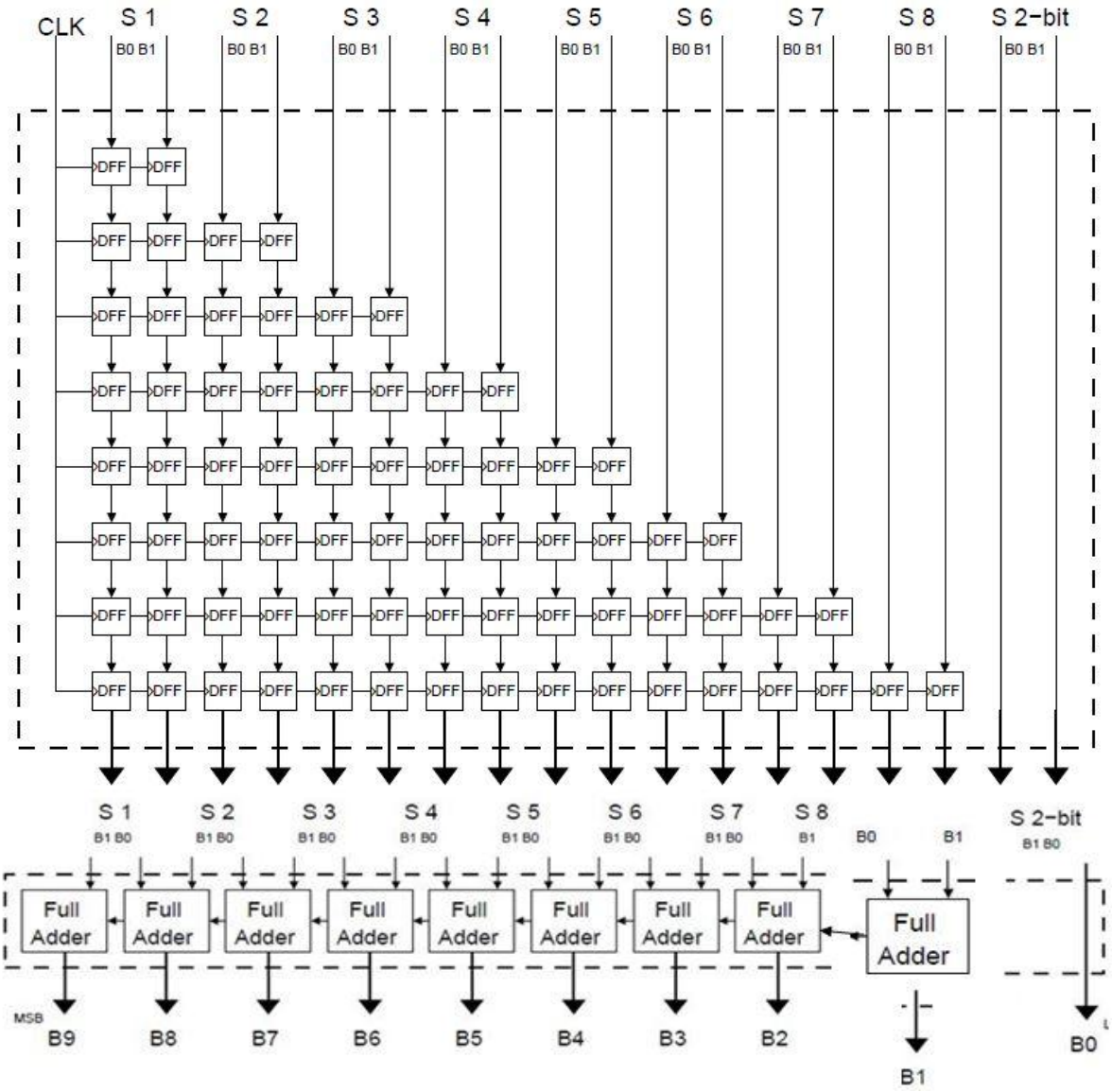


Figure 2.18: Digital block of an 8 bit pipeline ADC employing digital correction

Thus, for a pipeline ADC of 8 bits, employing digital correction will have N = 9 stages including the last flash-ADC stage. Although seven stages are used, Eq.2.2 suggests that digital output bits from the individual stages must be overlapped before digital addition is performed, i.e., MSB of the 6th stage must be aligned with the LSB of the 5th stage and so on. These outputs must be added using a full-adder to obtain the final digital output. This scheme is shown in Fig.2.18.

2.13 2.5bit stage:

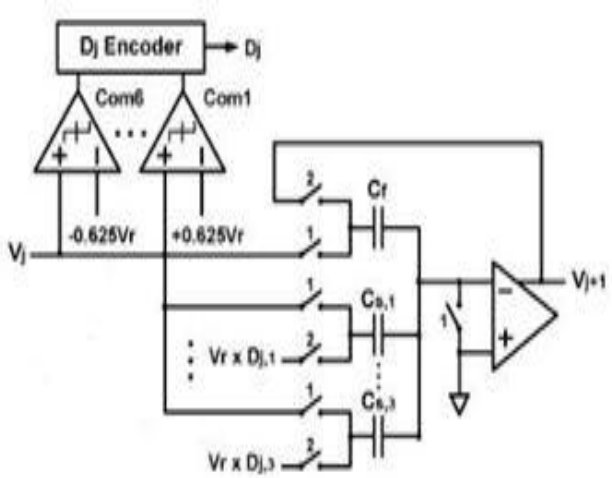


Figure 2.19: 2.5bit sub ADC

Sub-ADC Input(VIN)	T1	T2	T3	T4	T5	T6	D2	D1	D0
VIN ≤ Vcm-5Vref/8	0	0	0	0	0	0	0	0	0
Vcm-5Vref/8≤VIN≤ Vcm-3Vref/8	0	0	0	0	0	1	0	0	1
Vcm-3Vref/8≤VIN≤ Vcm-Vref/8	0	0	0	0	1	1	0	1	0
Vcm-Vref/8≤VIN≤ Vcm+Vref/8	0	0	0	1	1	1	0	1	1
Vcm+Vref/8≤VIN≤ Vcm+3Vref/8	0	0	1	1	1	1	1	0	0
Vcm+3Vref/8≤VIN≤ Vcm+5Vref/8	0	1	1	1	1	1	1	0	1
VIN ≤ Vcm+5Vref/8	1	1	1	1	1	1	1	1	0

Table 2.3: Truth table of 2.5bit encoder

The input Vin is sampled onto capacitors C1-C4. Then the charge stored in capacitors C1-C3 is transferred to capacitor C4, to gain up the input signal by a factor of 4. The bottom plates of capacitors C1-C3 are connected to the sub-ADC output simultaneously to implement the DAC subtraction.

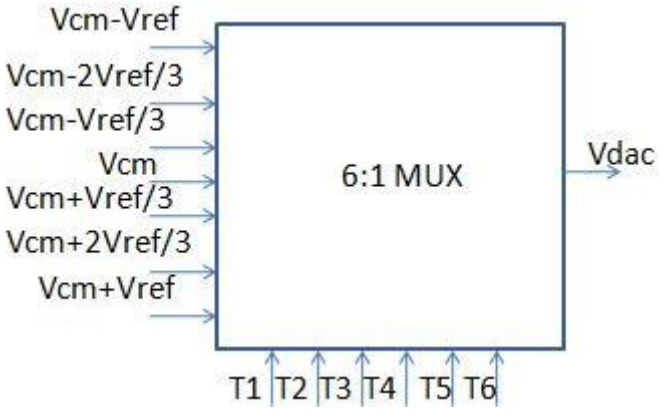


Figure 2.20: 2.5bit DAC

T6	T5	T4	T3	T2	T1	dacop+	dacop-
0	0	0	0	0	0	-vref	vref
0	0	0	0	0	1	-2vref/3	2vref/3
0	0	0	0	1	1	-vref/3	Vref/3
0	0	0	1	1	1	0	0
0	0	1	1	1	1	Vref/3	-vref/3
0	1	1	1	1	1	2vref/3	-2vref/3
1	1	1	1	1	1	vref	-vref

Table 2.4 Truth table of 2.5bit DAC

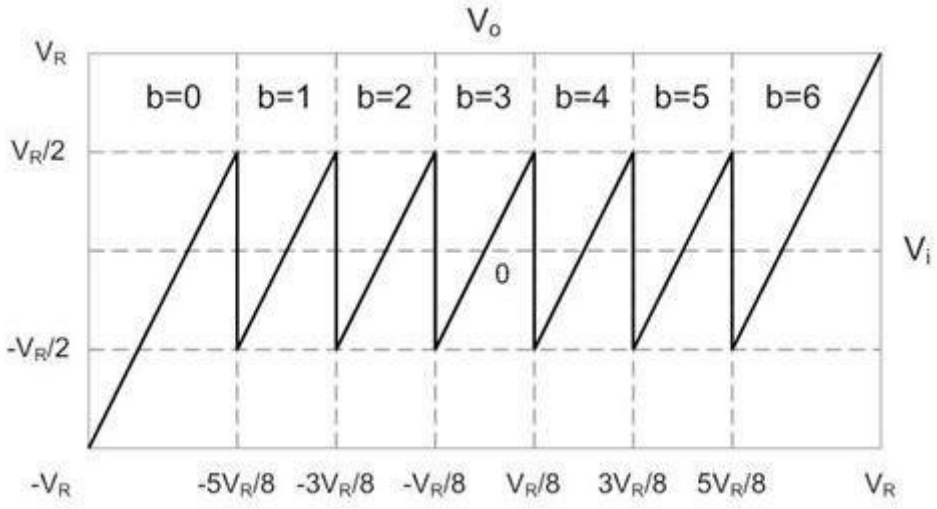


Figure 2.20 Transfer characteristics of 2.5 bit pipeline stage

2.5 bit pipeline stage requires 6 comparators and a 7 level DAC. Max tolerance on comparator is$\pm\frac{Vref}{8}$.

CHAPTER 3

Designed Building Blocks of the Pipeline ADC

The designed pipeline ADC uses analog pre-processing to divide the input signal range into sub-intervals and amplification of a residue signal for further processing in the subsequent stages. The realization of the pre-processing stages has been implemented using switched-capacitor circuits. Very accurate, linear amplification and algebraic operations are possible using switched-capacitor circuits. While designing the current pipeline ADC, two major blocks are implemented using switched-capacitor technique - front-end sample-and-hold amplifier (SHA) and the multiplying Digital to Analog Converter (MDAC). Needless to say, both these circuits need an amplifying device at its core. Since CMOS process has been chosen as the design platform for the current ADC, loads have been capacitive in nature. Consequently, Operational Transconductance Amplifiers (OTAs) are preferred over Op-Amps as an amplifying device.

3.1 Sample-and-Hold Amplifier:

In any traditional sample-and-hold amplifier (SHA), open loop architecture can achieve high sampling rate at the cost of resolution. Operational amplifiers or Operational trans-conductance amplifiers (OTAs), when operated in closed loop topology, improve the resolution of the SHA, but in order to achieve high sampling rate in closed loop, the concept of double sampling must be adopted. Other than sacrificing the accuracy, an open-loop SHA also suffers from clock feed-through generated by the switch induced charge injection. Applying op-amps in the negative feed-back loop can remove this feed-through to some extent. To further remove this error, techniques such as bottom plate sampling can be used. Bottom-plate sampling generates a constant charge injection from the switches, which can be effectively removed by using differential architecture. Also, by using boot-strapping, switch resistances can be made independent of the signal variations thus improving the linearity of the circuit.

3.1.1 Flip-around SHA

SHA, which is to be used as a front end sampler of an ADC, must have a resolution higher that of the ADC. Since the target resolution of the ADC is 10 bits, SHA

with a resolution of 12 bits must be designed. In order to achieve such accuracy, selecting closed loop architecture becomes imperative.

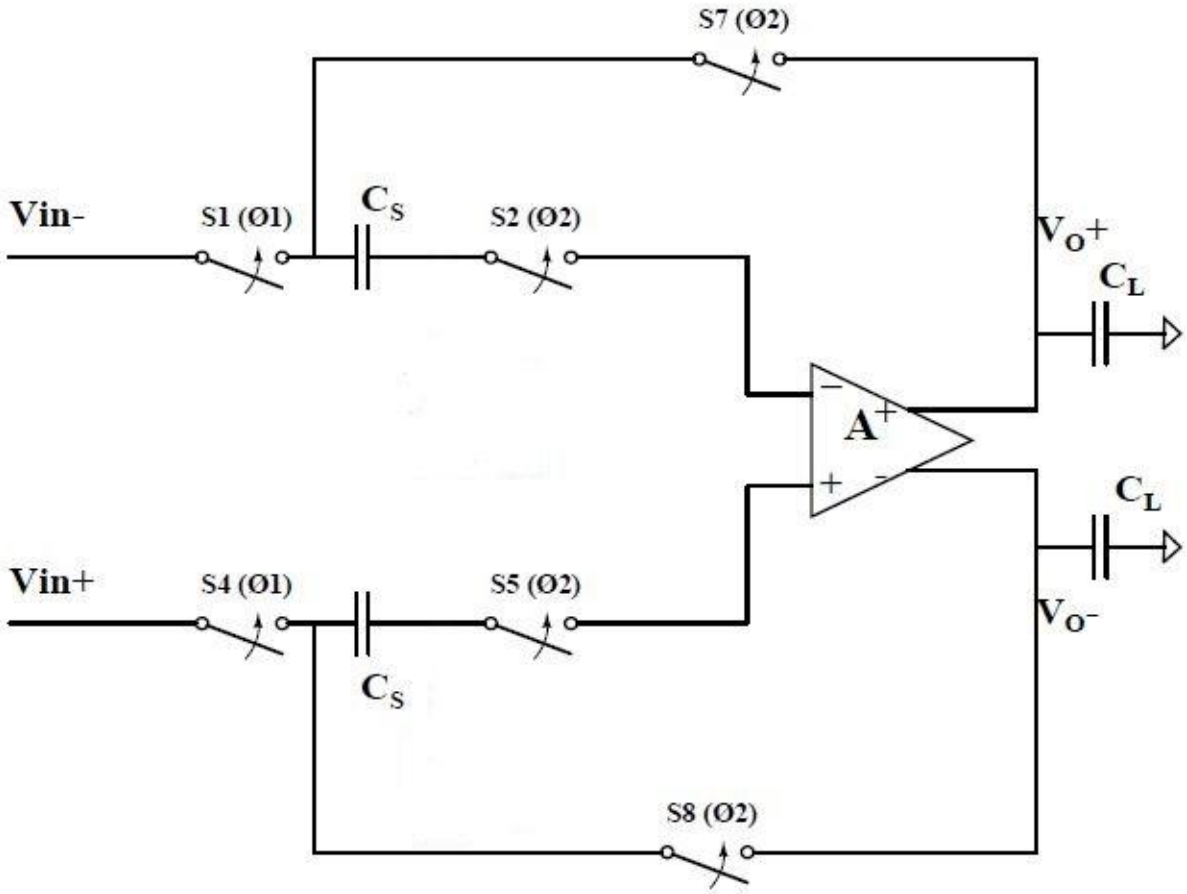


Figure 3.1: A flip around SHA circuit

A closed loop SHA architecture, commonly used in switched capacitor (SC) circuits and referred to as flip-around SHA is shown in Fig.3.1. Instead of using an op-amp in the negative feedback loop, this circuit uses passive circuits in the feedback, thus making faster acquisition possible. This differential circuit operates in two phases. In acquisition phase (Φ1) switch S1 is closed and the capacitor CS is charged to (Vin-). In the amplification phase (Φ2), switches S2 and S7 are closed. In this phase op-amp works in closed loop and the input signal gets reflected to the output.

In CMOS technology, switches are generally implemented using MOS transistors. A conducting MOS switch has a finite amount of mobile charges and when it turns off, charges distribute themselves through the drain, source and bulk terminals of the device. There are various methods to reduce these leakage charge error which is popularly known as charge injection error. Applying dummy switches working in opposite phase is a primitive but useful idea. The errors can be further reduced by applying transmission gates.

But if the errors can be made independent of the signal variations, superior linearity can be achieved by using differential architecture. Bottom-plate sampling (BPS) is one such technique [14] [15]. In order to understand bottom-plate sampling, the erroneous effects of charge injection arising from switches must be discussed briefly.

3.2 Errors associated with MOS switch:

a) Charge Injection Error:

In CMOS technology, switches are generally implemented using MOS transistors. A conducting MOS switch has a finite amount of mobile charges and when it turns off, charges distribute themselves through the drain, source and bulk terminals of the device. There are various methods to reduce these leakage charge error which is popularly known as charge injection error. For a mosfet to be on a channel must exist at the oxide silicon interface. Total charge in the inversion layer can be written as

$$Qch = WLCox(Vdd - Vin - Vth)$$

Where L denotes the effective channel length .When switch turns off Qch exits through source and drain terminals a phenomenon called "channel charge injection".

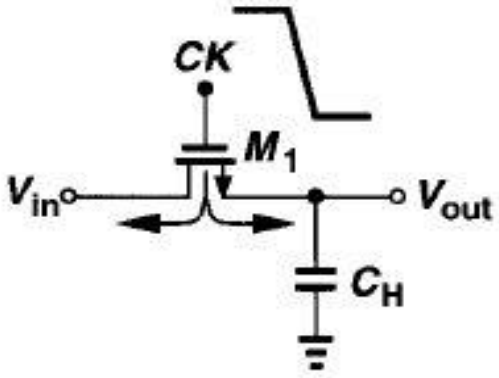


Fig 3.2 charge injection when switch turns off

The charge injected to the left side is absorbed by the input source creating no error. Charge injected to the right side is deposited on Ch introducing an error in the voltage stored on the capacitor. If half of Qch is injected on to Ch the resulting error equals to

$$\Delta V = \frac{WLCox(Vdd - Vin - Vth)}{2Ch}$$

In Figure 3.3 the error for an NMOS switch appears as negative pedestal at the output. Note that error is directly proportional to WLCox and inversely proportional to Ch.

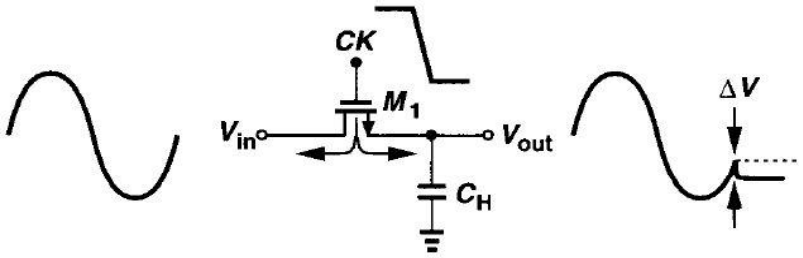


Fig 3.3 Effect of charge injection

In reality, the fraction of charge that exits through the source and drain terminals is a relatively complex function of various parameters such as the impedance seen at each terminal to ground and the transition time of the clock .Investigations of this effect have not yielded any rule of thumb that can predict the charge splitting in terms of such parameters. Furthermore, in many cases, these parameters, e.g., the clock transition time, are poorly controlled. Also, most circuit simulation programs model charge injection quite inaccurately. As a worst-case estimate, we can assume that the entire channel charge is injected onto the sampling capacitor.

Assuming all of the charge is deposited on the capacitor, we express the sampled output voltage as

$$Vout \approx Vin - \frac{WLCox(Vdd - Vin - Vth)}{Ch}$$

Where the phase shift between the input and output is neglected. Thus,

$$Vout = Vin\left(1 + \frac{WLCox}{Ch}\right) - \frac{WLCox(Vdd - Vth)}{Ch}$$

Suggesting that the output deviates from the ideal value through two effects: a non-unity gain equal to $1 + \frac{WLCox}{Ch}$ and a constant offset voltage of $-\frac{WLCox(Vdd-Vth)}{Ch}$ (Fig. 3.4). In other words, since we have assumed channel charge is a linear function of the input voltage, the circuit exhibits only gain error and dc offset.

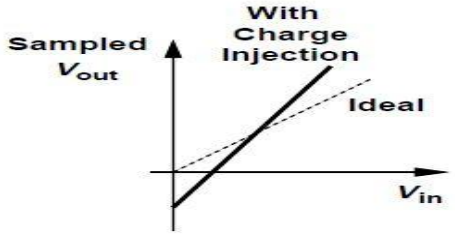


Figure 3.4. Input/output characteristic of sampling circuit in the presence of charge injection

In the foregoing discussion, we tacitly assumed that Vth is constant However, for NMOS switches (in an -well technology), body effect must be taken into account. Since $Vth = Vth0 + \gamma\left(\sqrt{(2}\phi B + VBS) - \sqrt{2}\phi B\right)$ and VBS = -Vin, we have

$$V_{out} = V_{in} - \frac{WLC_{ox}}{C_H}\left(V_{DD} - V_{in} - V_{TH0} - \gamma\sqrt{2\phi_B + V_{in}} + \gamma\sqrt{2\phi_B}\right)$$

$$= V_{in}\left(1 + \frac{WLC_{ox}}{C_H}\right) + \gamma\frac{WLC_{ox}}{C_H}\sqrt{2\phi_B + V_{in}} - \frac{WLC_{ox}}{C_H}\left(V_{DD} - V_{TH0} + \gamma\sqrt{2\phi_B}\right).$$

It follows that the nonlinear dependence of Vth uponVin introduces nonlinearity in the input/output characteristic.

In summary, charge injection contributes three types of errors in MOS sampling circuits: gain error, dc offsets, and nonlinearity. In many applications, the first two can be tolerated or corrected whereas the last cannot.

b) Clock Feed through:

In addition to channel charge injection, a MOS switch couples the clock transitions to the sampling capacitor through its gate-drain or gate-source overlap capacitance. Depicted in Fig. 3.5, the effect introduces an error in the sampled output voltage. Assuming the overlap capacitance is constant, we express the error as

$$\Delta V = Vck\left(\frac{WCov}{Wcov + Ch}\right)$$

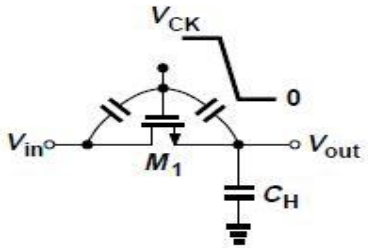


Figure 3.5. Clock feed through in a sampling circuit.

Where Cov is the overlap capacitance per unit width. The error ΔV is independent of the input level, manifesting itself as a constant offset in the input/output characteristic. As with charge injection, clock feed through leads to a trade-off between speed and precision as well.

c) KT/C Noise:

For high resolution ADC, the dominant noise source is usually KT/C noise. It comes from the sampling switch at front. Sampling transistor can be approximated by a

resistor, which has 4KTR ($\frac{V^2}{HZ}$) thermal noise associated with it. Since this is a linear time invariant circuit, the output mean square noise voltage can be calculated as:

$$\overline{V_{out}^2} = \int_{-\infty}^{\infty} |H(f)|^2 \cdot 4KTR \cdot df = \int_{-\infty}^{\infty} \frac{4KTR}{1+(2\pi fRC)^2} df = \frac{KT}{C}$$

A resistor charging a capacitor gives rise to a total rms noise voltage of$\frac{\sqrt{KT}}{C}$. As shown in Fig. 3.6, a similar effect occurs in sampling circuits.

Figure 3.6. Thermal noise in a sampling circuit

The on-resistance of the switch introduces thermal noise at the output and, when the switch turns off, this noise is stored on the capacitor along with the instantaneous value of the input voltage. It can be proved that the rms voltage of the sampled noise in this case is still approximately equal to$\frac{\sqrt{KT}}{C}$.The problem of KT/C noise limits the performance in many high-precision applications. In order to achieve a low noise, the sampling capacitor must be sufficiently large, thus loading other circuits and degrading the speed.

So the noise voltage at output has no relationship with the value of resistance. Noise voltage can be reduced to a small amount only when capacitor is large enough. Since resolution requirement is the tightest at first stage, capacitor size is largest at first stage's input. For the following stage, capacitor can be sized down due to a smaller resolution requirement. With capacitor scaling, the Op Amp driving it need not maintain that large bandwidth as first stage. As a result, the whole stage scales down. This is called stage scaling.

3.3 Charge Injection Cancellation:

Charge injected by the main transistor can be removed by means of a second transistor. As shown in Fig. 3.7, a "dummy" switch, M2 driven by $\sim CK$ added to the circuit such that after M1 turns off and M2 turns on, the channel charge deposited by the

former on Ch is absorbed by the latter to create a channel. Note that both the source and drain of M2 are connected to the output node.

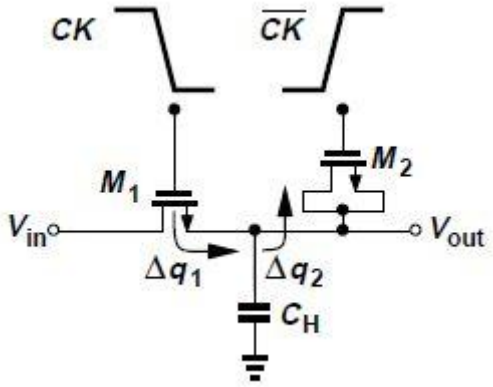


Figure 3.7. Addition of dummy device to reduce charge injection and clock feed through

How do we ensure that the charge injected by M1, $\Delta q1$ is equal to that absorbed by M2, $\Delta q2$?Suppose half of the channel charge of M_1 is injected onto Ch i.e.

$$\Delta q1 = \frac{W1L1Cox(Vck - Vin - Vth1)}{2}$$

Since $\Delta q2 = W2L2Cox(Vck - Vin - Vth2)$ if we choose W2=0.5W1 and L2=L1, then $\Delta q2 = \Delta q1$. Unfortunately, the assumption of equal splitting of charge between source and drain is generally invalid, making this approach less attractive.

Interestingly, with the choice W2=0.5W1 and L2=L1, the effect of clock feed through is Suppressed. As depicted in Fig. 3.8, the total charge in Vout is zero because

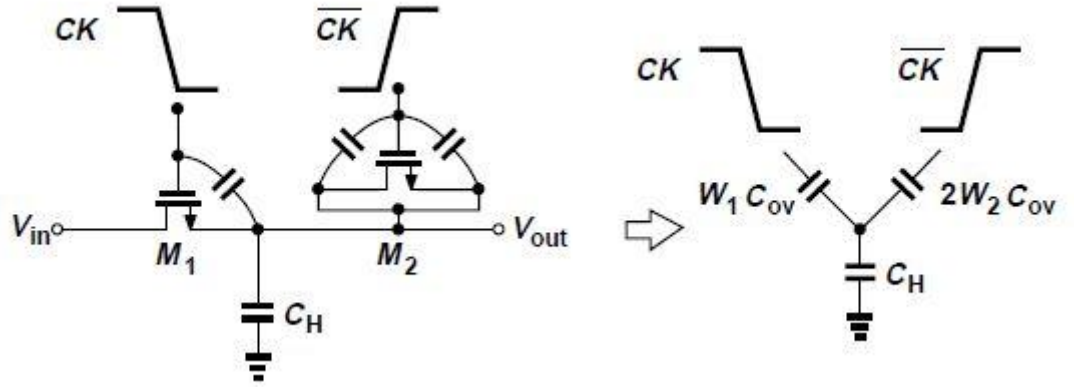


Figure 3.8. Clock feed through suppression by dummy switch

$$-Vck\left(\frac{W1Cov}{W1Cov + Ch + 2W2Cov}\right) + Vck\left(\frac{2W2Cov}{W1Cov + Ch + 2W2Cov}\right) = 0$$

Another approach to lowering the effect of charge injection incorporates both PMOS and NMOS devices such that the opposite charge packets injected by the two cancel each other (Fig. 3.9). For $\Delta q1$ to cancel$\Delta q2$, we must have

$$W1L1Cox(Vck = Vin - Vthn) = W2L2Cox(Vin - |Vthp|)$$

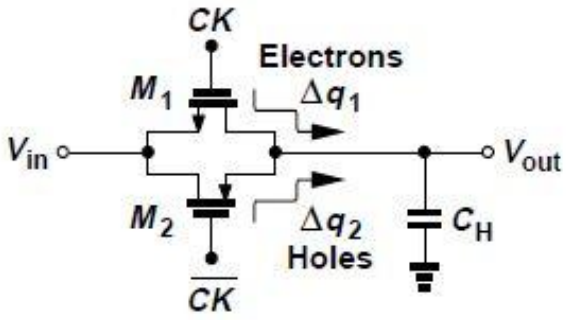


Figure 3.9. Use of complementary switches to reduce charge injection

Thus, the cancellation occurs for only one input level. Even for clock feed through, the circuit does not provide complete cancellation because the gate-drain overlap capacitance of NFETs is not equal to that of PFETs.

Our knowledge of the advantages of differential circuits suggests that the problem of charge injection may be relieved through differential operation. As shown in Fig. 3.10, we surmise that the charge injection appears as a common-mode disturbance. But, writing $\Delta q1 = WLCox(Vck - Vin1 - Vth1)$ and $\Delta q2 = WLcox(Vck - Vin2 - Vth2)$ we recognize that $\Delta q1 = \Delta q2$ only if Vin1=vin2. In other words, the overall error is not suppressed for differential signals. Nevertheless, this technique both removes the constant offset and lowers the nonlinear component. This can be understood by writing

$$\begin{aligned}\Delta q1 - \Delta q2 &= WLCox[(Vin2 - Vin1) + (Vth2 - Vth1)] \\ &= WLCox[Vin2 - Vin1 + \gamma(\sqrt{2\varphi F + Vin2} - \sqrt{2\varphi F + Vin1})\end{aligned} \quad (3.1)$$

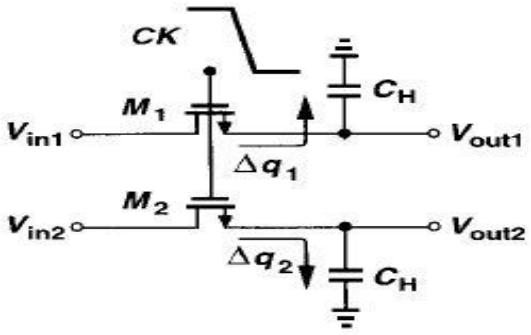


Figure 3.10 Differential sampling circuits

Since for Vin1=Vin2, $\Delta q1 - \Delta q2 = 0$, the characteristic exhibits no offset. Also, the nonlinearity of body effect now appears in both square-root terms of (3.1), leading to only odd-order distortion.

The problem of charge injection continues to limit the speed-precision envelope in sampled-data systems. Many cancellation techniques have been introduced but each leading to other trade-offs. One such technique, called "bottom-plate sampling," is widely used in switched-capacitor circuits.

3.4 Bottom plate sampling (BPS):

To remove the errors caused by supply dependent charge injection, bottom plate sampling are very widely employed in many switched-capacitor circuits. The MDAC circuit designed for the ADC in the present thesis also uses the concept of bottom-plate sampling in order to achieve good linearity. As shown in Fig.3.11 bottom plate sampling actually uses 3 clock phases. Phases Φ1 and Φ2 are of opposite polarity. Whereas clock Aclk (phase Φ1') is t s advanced than clock clk. At t s prior to the termination of phase Φ1, clock Aclk forces switch S3 to turn off. As one terminal of this switch is permanently connected to VCM, charge injected by this switch in the off period is constant. So, the bottom plate of the capacitance C_s is at a fixed erroneous potential thanks to switch S3. After t s, switch S1 turns off and charge induced by this switch gets no path to discharge as bottom plate of C_s is left floating. In differential architecture, this error gets cancelled as it is same for both halves of the circuit.

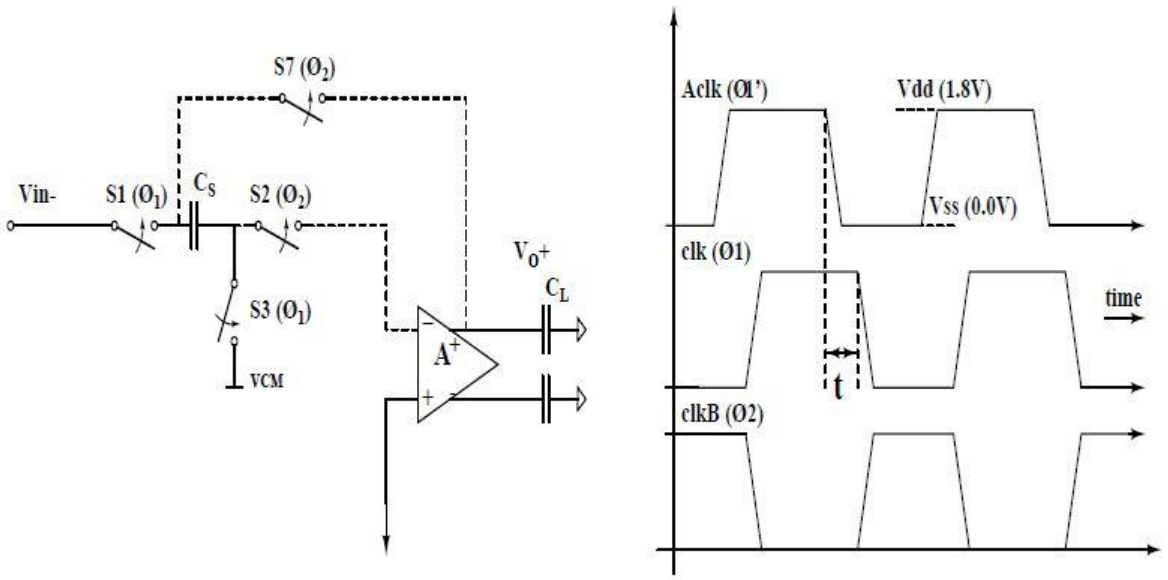


Figure 3.11: Bottom plate sampling technique

3.5 Nonlinearity of on-resistance:

When both NMOS and PMOS work in linear region, the on resistance can be found as shown in Figure 3.12.

$$R_{on} = \frac{1}{u_n C_{ox} \frac{W_n}{L_n}(V_{DD} - V_{in} - V_{thn})}$$

$$R_{op} = \frac{1}{u_p C_{ox} \frac{W_p}{L_p}(V_{in} - |V_{thp}|)}$$

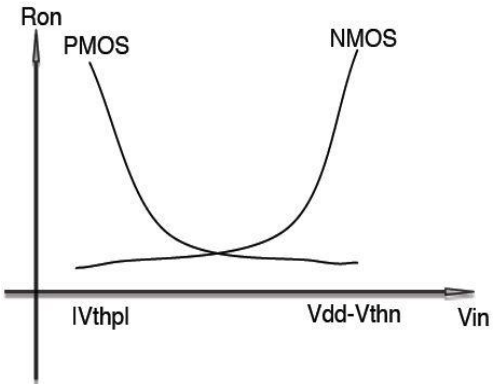


Figure 3.12 On resistance of NMOS and PMOS

It can be found that on-resistance varies with input voltage and the relationship is not linear, as shown in Figure 3.12, which results in harmonic distortion at output. This phenomenon is quite undesirable because it adds nonlinearity directly to input signal even before it's quantized.

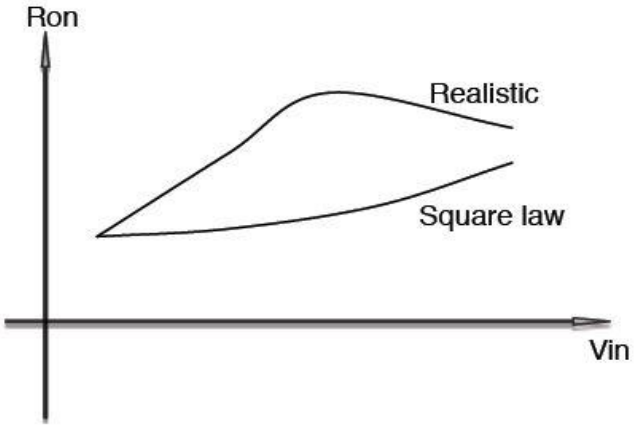
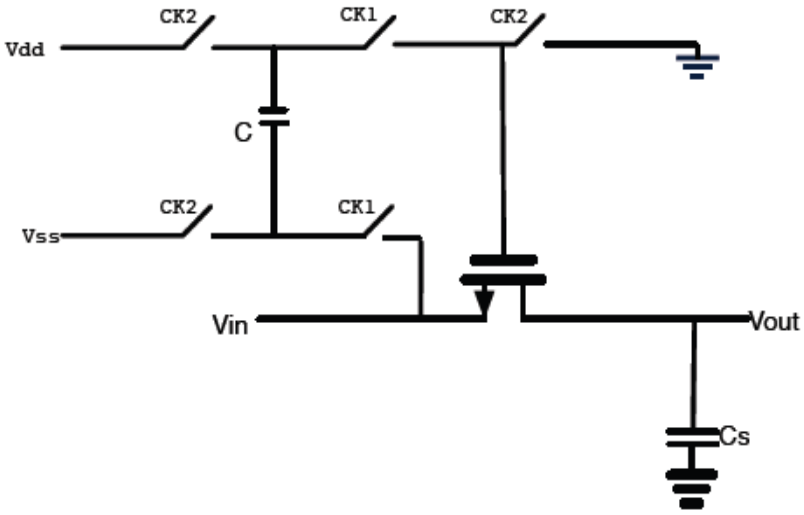


Figure 3.12 Nonlinearity of on-resistance

The way to address this is the bootstrap switch which is shown in Figure 3.13. The basic idea is to make gate source voltage constant.when CK2 is high, voltage between capacitor is Vdd, and sampling switch is off. When CK1 is high, bottom side of capacitor is connected to input signal, while the top is connected to gate, with a voltage Vdd+Vin, and sampling switchis on. Through this way, gate source voltage is maintained constant and it eliminates nonlinearity of on-resistance.



Fiure 3.13 Bootstrap switch

CHAPTER 4

MDAC OTA SPECIFICATIONS:

DC gain (Adc) can be derived from the resolution requirement of the ADC .Sampling speed of the ADC determines the Unity Gain Bandwidth (UGB) of the OTA .Input dynamic range of the ADC can be mapped directly to the Input Common Mode Range (ICMR) of the OTA.

4.1 DC gain (Adc):

To determine the required open loop dc gain, a closed loop configuration of the op-amp must be considered as shown in Fig.4.1 (a). Open loop DC gain of the amplifier is A. A step signal has been fed at the input and the output transient has been shown in Fig.4.1 (b).

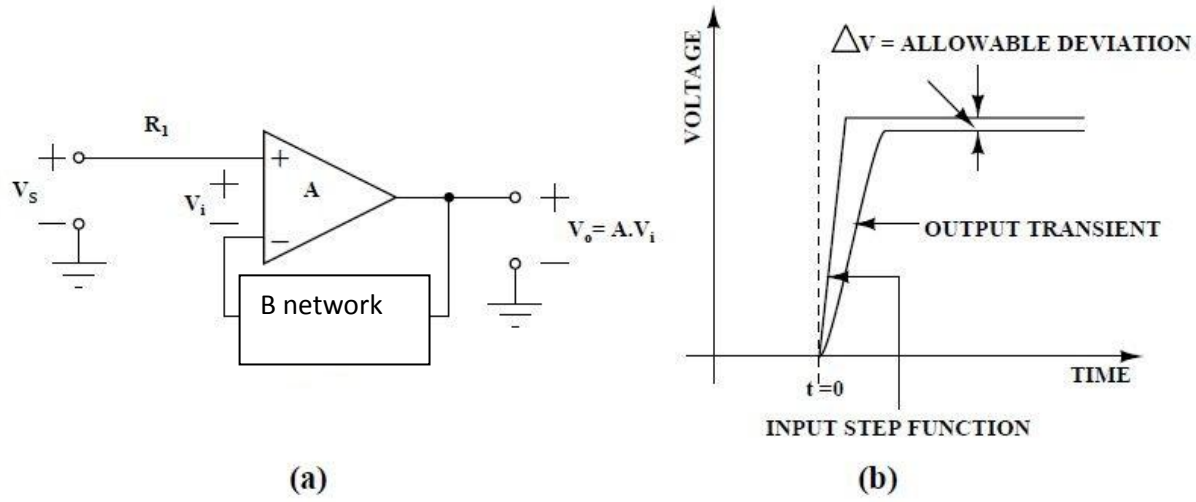


Figure 4.1: Op-amp in unity gain feedback configuration

As the target resolution is 10 bit, closed loop operation of the amplifier can allow only $\frac{ICMR}{2^{10}}$V of deviation. The non-inverting amplifier configuration shown in Fig 4.1 (a) has a closed loop gain of Aclosed = (1/β) under the condition that open loop gain of the amplifier is infinite. In practical situations though the amplifier gain is finite and the closed loop gain equation gets modified as

$$A'closed = \frac{A}{1 + A\beta}$$

So, the deviation of the output can be determined by using the following equations:

$$\left(\frac{V0}{Vs}\right) - \left(\frac{Vo'}{Vs}\right) = \left(\frac{1}{\beta}\right) - \left(\frac{A}{1+A\beta}\right) = \frac{1}{A\beta}$$

Vs mentioned in the above equations are the ICMR of the amplifier. So, from the following equations the open loop gain A can be estimated as,

$$\frac{ICMR}{A\beta} \leq \frac{ICMR}{2^{10}}$$

$$Adb \geq 20\log\left(\frac{2^{10}}{\beta}\right)$$

In 1.5bit MDAC $\beta = \frac{Cf}{Cf+Cs} = \frac{1}{2}$ (where Cf is the feedback capacitor and Cs is the sampling capacitor)

Adb>67db

In order to achieve satisfactory resolution from the ADC, the open loop gain of the OTA has been set as A(0) ≥67 dB.

4.2 Unity Gain Bandwidth (UGB):

OTA must settle its output to a desired value (2-5 % of the final value) within time T/2 where T = 1/fclk. As the dominant pole of the unity gain closed loop OTA will be same as the UGB of the open loop OTA, following equations will hold

$$Aopen.f3db, open = UGB$$

$$f3db, closed = (1 + Aopen.\beta)f3db, open \approx Aopen.\beta.f3db, open$$

$$f3db, closed = \beta.UGB = \frac{1}{2\pi\tau}$$

Where τ is the time constant of the closed loop OTA. For a square wave input, the single time constant closed loop OTA will behave as shown in Fig.4.2. Mathematically, the transient behaviour of the OTA output from t = 0 to t = T/2 can be expressed as

$$Vo(t) = E\{1 - e^{-\frac{t}{\tau}}\}$$

Since the OTA must settle within T/2,

$$E\left\{1 - e^{-\frac{T}{2\tau}}\right\} \geq E - \frac{E}{2^N}$$

$$\tau \leq \frac{T}{2Nln2}$$

With fclk = 50 MHz, T/2 = 20 ns, resolution N = 10 bit and $\tau = \frac{1}{2\pi\beta UGB}$

UGB > 230MHZ

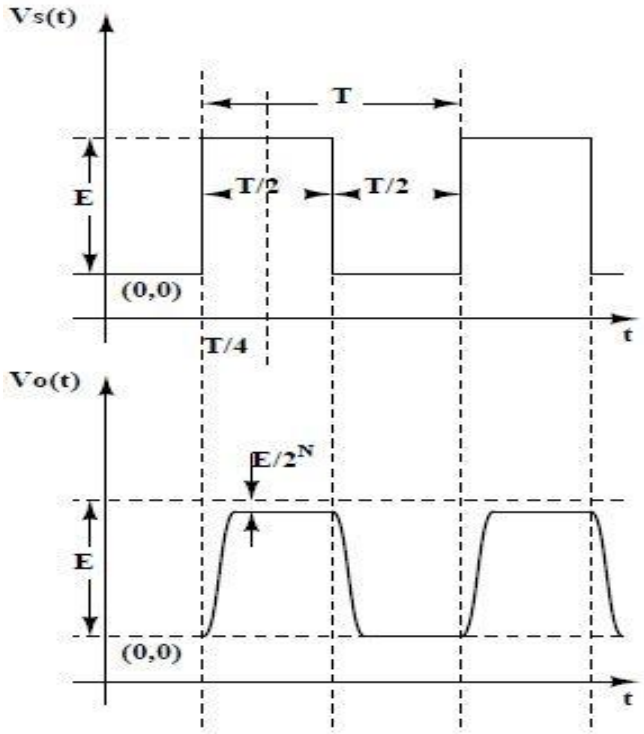


Figure 4.2: Transient behaviour of OTA

4.3 OTA architecture: Gain boosted Telescopic OTA

In order to achieve high dc gain of an OTA as well as high GBW (Gain Band Width), selection of architecture of the OTA is of prime concern. DC gain Adc can be increased if a two stage amplifier is considered. But in such circuits, to achieve stability, compensation capacitors are required. These capacitors help form Miller effect capacitances which in turn increases the effective time constant of the amplifier. Thus the operational speed of the amplifier reduces. Cascoding a single stage amplifier increases its output impedance and the dc gain Adc according to the equation Adc = Gm.ROUT . Also, single stage amplifier works much faster than its two stage counterpart. But cascode OTAs have limited output swing (OS) and Input Common Mode Range (ICMR).

For a telescopic OTA,

$$VGS2 + VDSAT1 \leq ICMR \leq VDD - VDSAT8 - VDSAT6 - VDSAT4$$

$$VDSAT1 + VDSAT4 + VDSAT2 \leq OS \leq VDD - VDSAT8 - VDSAT6$$

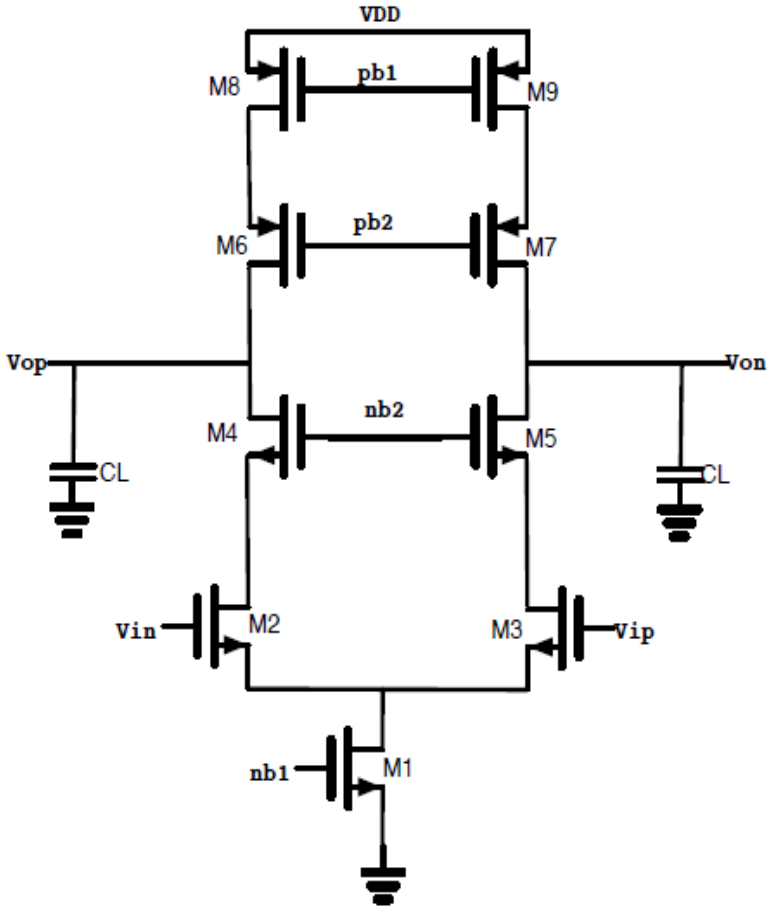


Figure 4.3 Telescopic OTA

The differential pair is loaded with cascade current source. Therefore, the output impedance is increased to:

$$ROUT = R1 \| R2 = [(gm4rds4)\ rds2 \| (gm6rds6)\ rds8]$$

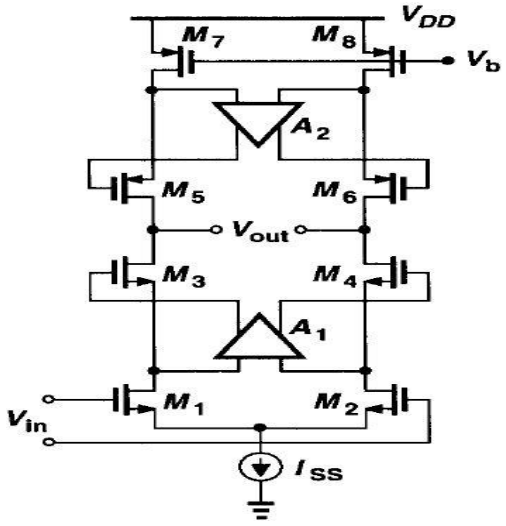
Since trans-conductance is still gm2, DC gain can be found to be:

$$A = gm2\ [(gm4rds4)\ rds2 \| (gm6rds6)\ rds8]$$

Since dominant pole frequency is at output, given by $\frac{1}{ROUT.CL}$, the unity gain bandwidth is approximately $\frac{gm2}{CL}$.Slew rate is simply $\frac{I1}{CL}$.This kind of amplifier will be used in MDAC, but the open loop gain is far from enough to maintain small close loop gain error. Thus, gain-boosting technique is utilized in the proposed amplifier.

a) Gain boosted telescopic OTA:

DC gain of a telescopic amplifier is dependent on the output resistance of the amplifier. Although cascading improves the output impedance considerably, in some applications even higher gain is often required. To achieve that, a telescopic OTA is retrofitted with gain boosters as shown in Figure 4.4 which increase the dc gain of the amplifier immensely. Cascode load stage of these amplifiers has two gain boosters with gain A_1 and A_2. These boosters help increase the output impedance of the amplifier by a factor of $A_1 = A_2 = A$.



A1 – pmos input folded cascode amplidier

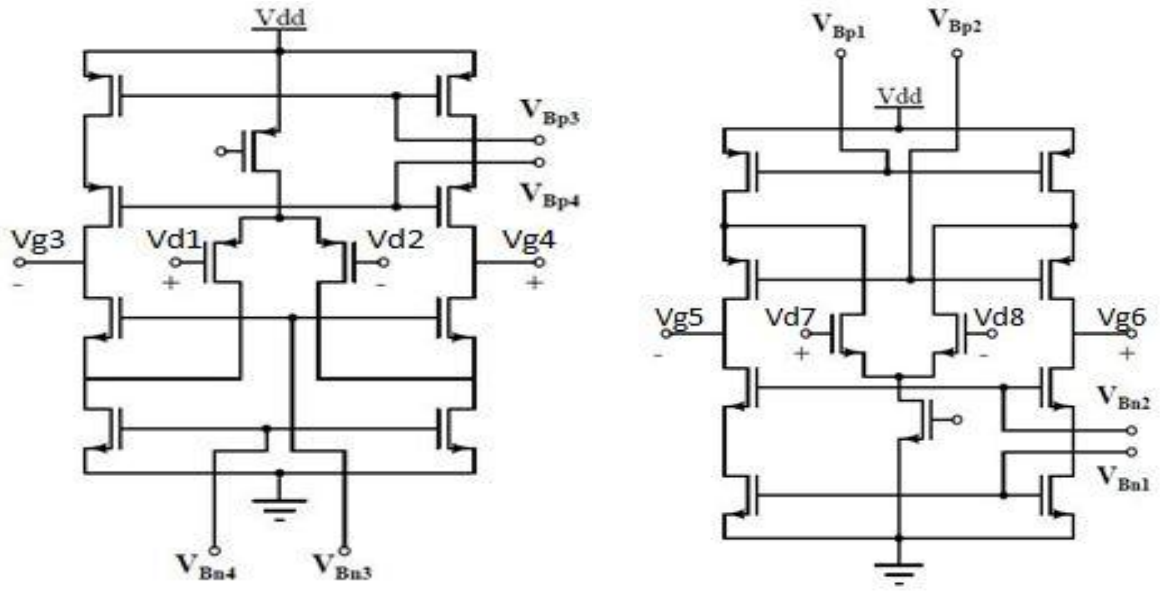
A2 – nmos input folded cascode amplifier

Figure 4.4 Gain boosted telescopic OTA

Since the dc gain of an OTA is defined as $A_{dc} = A(0) = G_m.R_{OUT}$, where G_m and R_{OUT} are transconductance and output resistance of the amplifier respectively, gain-boosted amplifier dc gain $A_{GB}(0)$ can be written as,

$$A_{GB}(0) = g_{m2} \cup A g_{m4} r_{ds4} r_{ds2} \parallel A g_{m6} r_{ds6} r_{ds8} \uplus$$

From above equation, enhancement of gain of the amplifier is evident. To maintain the output swing of the OTA high, it is necessary that the gain booster amplifiers have high ICMR. For this reason, folded-cascode amplifiers are often chosen as the gain boosters. If the auxiliary amplifier has moderate DC gain, then telescopic amplifier will probably have enough gain. Meanwhile, stability won't be affected since gain boosting is not on main signal path. Bandwidth of auxiliary amplifier should be large enough to avoid slowing down the main stage.

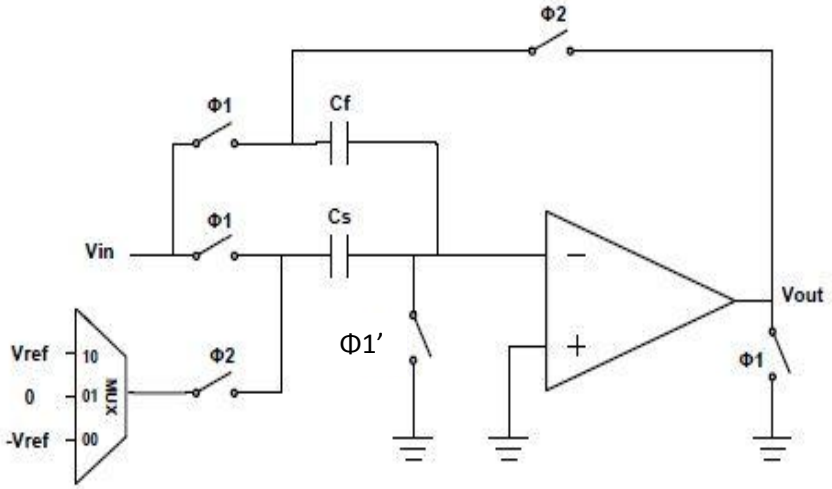


(a) (b)

Figure 4.5 : (a)pmos and (b)nmos gain boosting folded cascode amplifers

4.4 **Multiplying Digital to Analog Converter (MDAC):**

In a pipeline ADC, an MDAC is a critical block performing multiple jobs like signal subtraction, multiplication and sample-and-hold function altogether. In this Section, an MDAC to be used in a pipeline ADC is detailed. To achieve reduced power consumption and better linearity, switched-capacitor technique has been applied while implementing the MDAC. The method of optimizing the size of the capacitors involved in this circuit in order to meet the speed requirement is also detailed thereafter.



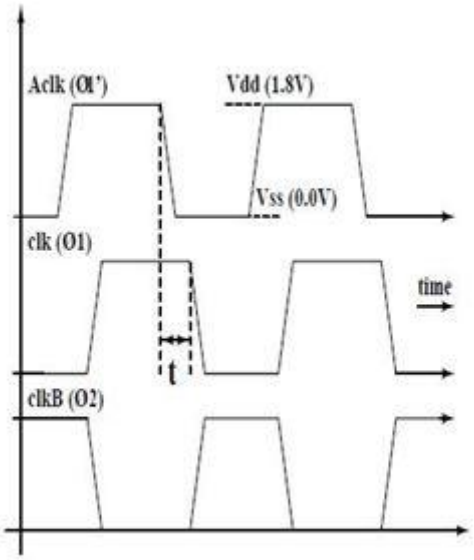


Figure 4.6: Functional Block diagram of a SC MDAC circuit

Like most SC circuits, SC MDACs also work in two clock phases. Fig.4.6 shows a typical SC MDAC circuit. A single ended topology has been considered to explain the function of this MDAC Input signal is Vin while the output signal is Vo. In clock phase Φ1 input voltage Vin is charged across all the capacitors. The charge q1 accumulated on the top plate of the capacitors can be expressed as q1= Vin (Cf+Cs) In clock phase Φ2 the amplifier is put into closed loop. Apart from capacitor Cf the other capacitor Cs gets connected to Vref as denoted by the sub-ADC outputs. Assuming gain of the amplifier finite (Gain=A), charge q2 on the top plates of capacitors in 2 is formulated as,

$$q2 = Cf*Vo + Cs\ (2b1+b0)\ Vref$$

From the law of conservation of charge, q1 = q2

$$Vin\ (Cf+Cs) = Cf*Vo + Cs\ (2b1+b0)\ Vref$$

$$Vo = Vin\ (Cf + Cs)/Cf \ - \ Vref\ (2b1 + b0)\ Cs/Cf$$

Where b1; b0 are the sub-ADC output. To achieve a gain of 2, Cs = Cf. Equations involving the transfer function of a 1.5 bit MDAC can be described as for single ended circuit, with Vref = FS, and for differential circuit, Vref = FS/2 as

$$V_o = \begin{cases} 2V_{in} & V_{in} \le \frac{3V_{ref}}{8} \\ 2V_{in} - \frac{V_{ref}}{2} & \frac{3V_{ref}}{8} \le V_{in} \le \frac{5V_{ref}}{8} \\ 2V_{in} - V_{ref} & V_{in} \ge \frac{5V_{ref}}{8} \end{cases} \quad V_o = \begin{cases} 2V_{in} + V_{ref} & V_{in} \le -\frac{V_{ref}}{4} \\ 2V_{in} & -\frac{V_{ref}}{4} \le V_{in} \le \frac{V_{ref}}{4} \\ 2V_{in} - V_{ref} & V_{in} \ge \frac{V_{ref}}{4} \end{cases}$$

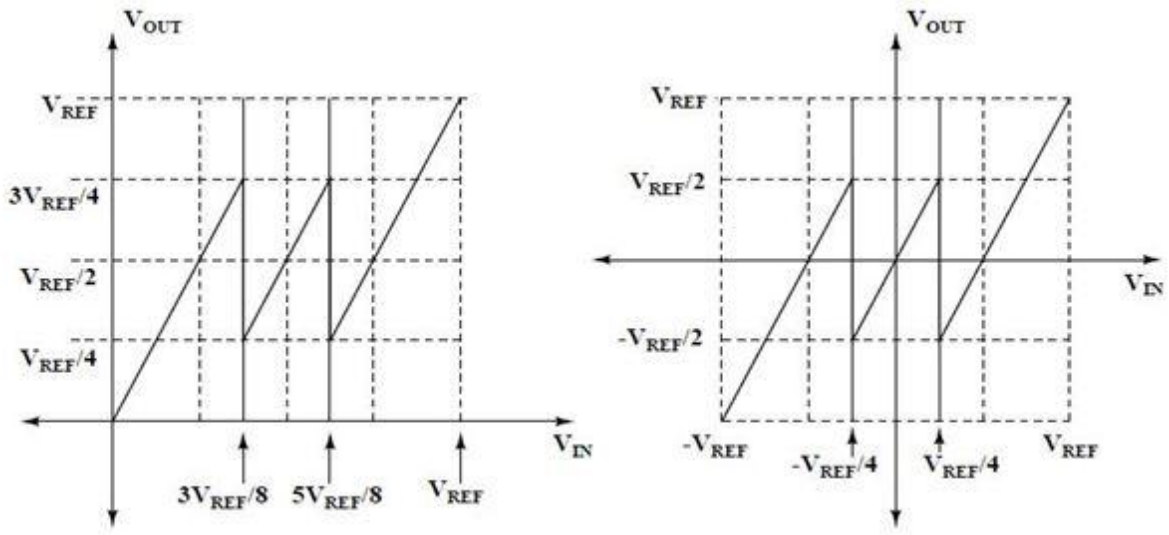


Figure 4.7 (a) Transfer curve for single ended circuit (b) Transfer curve for differential circuit

4.5 Thermal noise in MDAC:

Performance of a SC MDAC is primarily limited by the thermal noise generated by the sampling capacitors of the circuit. Noise is also contributed by the parasitic Capacitances of the OTA. Generally, noise due to these parasitic capacitances is ignored while calculating the thermal noise of the circuit. An m stage pipeline ADC has been shown in Fig.4.8 along with its MDACs in each stage. Stage resolutions of this ADC are n1; n2 ...nm. Effect of the sub-ADC in noise contribution has been neglected for the simplicity of the noise calculation.

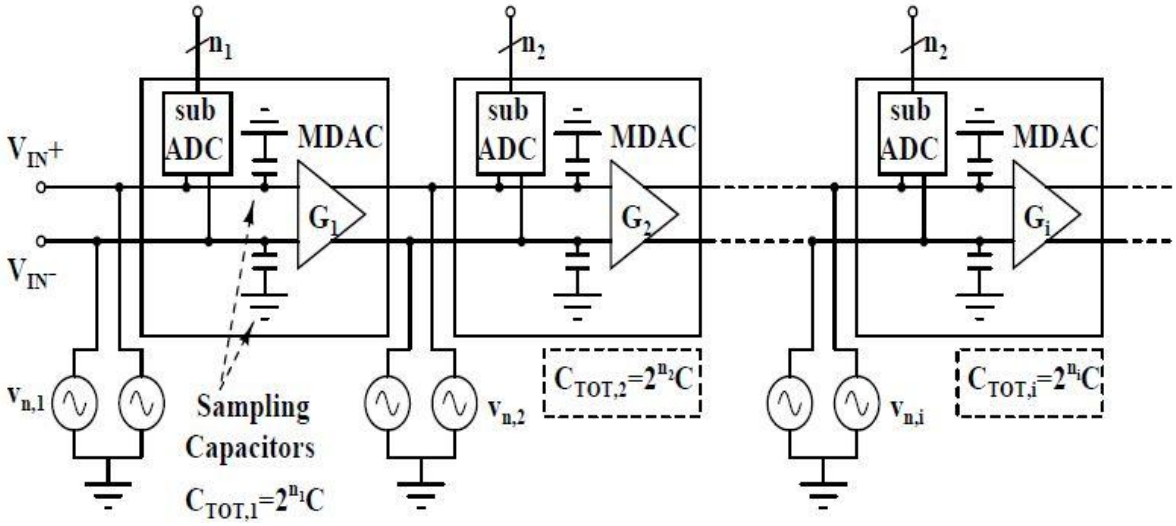


Figure 4.8: Thermal noise in MDAC

Considering each stage independently, thermal noise generated will follow the equations described as [12],

$$Vn, i^2 = KT/(2^{ni} * \mathrm{C})$$

The thermal noise power generated by the 1st stage is denoted as $Vn, 1^2$, for 2nd stage it is $Vn, 2^2$ and so on. Since the input referred noise of the ADC occurring only due to 1st stage is $Vn, input1^2 = KT/(2^{n1}\mathrm{c})$ accuracy requirement of this stage becomes very stringent. Thus, the input referred noise of the 1st stage must be less than the quantization noise of the entire ADC. For the 1^{st} stage the condition must be,

$$Vn, input1^2 \leq Vn, quantization^2 = \frac{\left(\frac{FS}{2^{nTOT}}\right)^2}{12}$$

$$KT/(2^{n1}\mathrm{C1}) \leq \frac{\left(\frac{FS}{2^{nTOT}}\right)^2}{12}$$

$$C1 \geq \frac{3.2^{2nTOT+2}KT}{2^{n1}FS^2}$$

Thus the thermal noise limitation helps determining the lower limit of the sampling capacitor of the 1^{st} stage.

4.6 Bandwidth limitation of MDAC:

Size of the sampling capacitors in an MDAC can seriously limit the sampling speed of both the MDAC and the ADC. Load capacitance C_L of the 1st stage can be determined taking the sampling capacitors of the 2^{nd} stage into consideration. The parasitic capacitance of the OTA, COUT1,p of the 1st stage at the output node will also contribute to its load capacitance. For simplicity, the parasitic capacitances will be ignored while analyzing the settling behaviour. Load capacitance CL, 1 turns out to be

$$\mathrm{CL1} = \mathrm{Cf1} + (\mathrm{Cs2} + \mathrm{Cf2})$$

Where Cf1 is the feedback capacitor of the 1st stage while Cs2 and Cf2 are the sampling and feedback capacitors of second stage. Settling error occurring from this OTA would be

$$Er = e^{-ts\omega 3db}$$

Where t_s is the settling time and ω_{3dB} is the -3dB frequency of the OTA. Since the OTA is in closed loop during the sampling mode, feedback factor β can be calculated as

$$\beta = \frac{Cs1}{Cs1 + Cf1}$$

Where Cs1 and Cf1 are sampling and feedback capacitors of first stage respectively. Also, as 3dB frequency ω_{3dB} and Unity Gain Frequency (UGB) ω_u of the OTA are related as $\omega_{3dB} = \omega_u\beta$, it can be further rewritten as,

$$\omega 3db = \omega u.\beta$$

$$\omega 3db = gm1.\frac{\beta}{CL,1}$$

$$\omega 3db = \frac{gm1.Cs1}{(Cs1+Cf1).(Cf1+Cs2+Cf2)}$$

MDAC must work fast enough so that the output of the 1^{st}stage settles to LSB/2, where LSB would be as determined from the 2nd stage on-wards, i.e., LSB =$\frac{1}{2^{nTOT-n1+1}}$ Here, it has been assumed that digital correction is applied to the 1st stage. Also, considering the MDAC must settle within half of the sampling period, ts =$\frac{1}{2fs}$

$$Er = e^{-ts\omega 3db} \leq \frac{1}{2^{nTOT-n1+2}}$$

$$\omega 3db \geq 2fsln(2^{nTOT-n1+2})$$

$$\frac{gm1.Cs1}{(Cs1+Cf1).(Cf1+Cs2+Cf2)} \geq 2fsln(2^{nTOT-n1+2})$$

By taking same capacitance value for both first and second stages i.e.; Cs1=Cf1=Cs2=Cf2 we get

$$C \leq \frac{gm1}{12fsln(2^{nTOT-n1+2})}$$

$$\frac{3.2^{2nTOT+2}KT}{2^{n1}FS^2} \leq C \leq \frac{gm1}{12fsln(2^{nTOT-n1+2})}$$

CHAPTER 5

5.1 Opamp Shared Pipeline ADC:

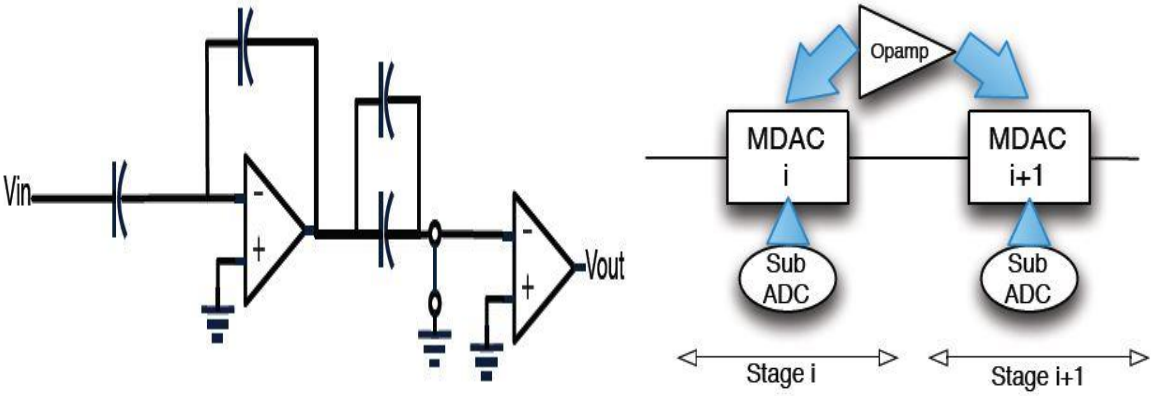


Figure 5.1: Opamp sharing between two pipeline stages of MDAC

When one stage is in amplification phase, the following stage is in sampling phase. Then the first stage goes to sampling phase while the following stage starts to amplify. It's obvious that the amplifier in each stage is used in half clock cycle. The other half cycle is actually resetting error on amplifier. The proposed idea is to do Op Amp sharing. When first stage is amplifying, the second stage won't need Op Amp. When second stage is amplifying, it uses the previous amplifier because the first stage won't need it in this half cycle

5.2 Conventional opamp-sharing MDAC:

Opamp sharing technology can save nearly half of the power consumption, it is achieved at the cost of resolution reduction, since the conventional opamp-sharing ADC has two serious problems. First, because the opamp input summing node is never reset, every input sample is affected by the error voltage stored on the input capacitor due to the previous sample. Thus it suffers from the memory effect, which can be considered as a signal-dependent OTA offset [17]. To avoid memory effects, the OTA inputs can be reset using a short duration third phase. However, this would reduce the time available for MDAC stage output settling. Second, there is a potential crosstalk path between two successive stages caused by the parasitic capacitors of switches, which are used to implement opamp sharing. The conventional opamp-sharing MDAC with parasitic capacitance is shown in Fig.5.2. The signals in the current and successive stages, which appear at input nodes of the shared opamp, will influence each other through the crosstalk path. In addition, the opamp-sharing switches also introduce charge injection and signal-dependent resistance. These factors degrade both the linearity and the signal-to-noise-ratio (SNR).

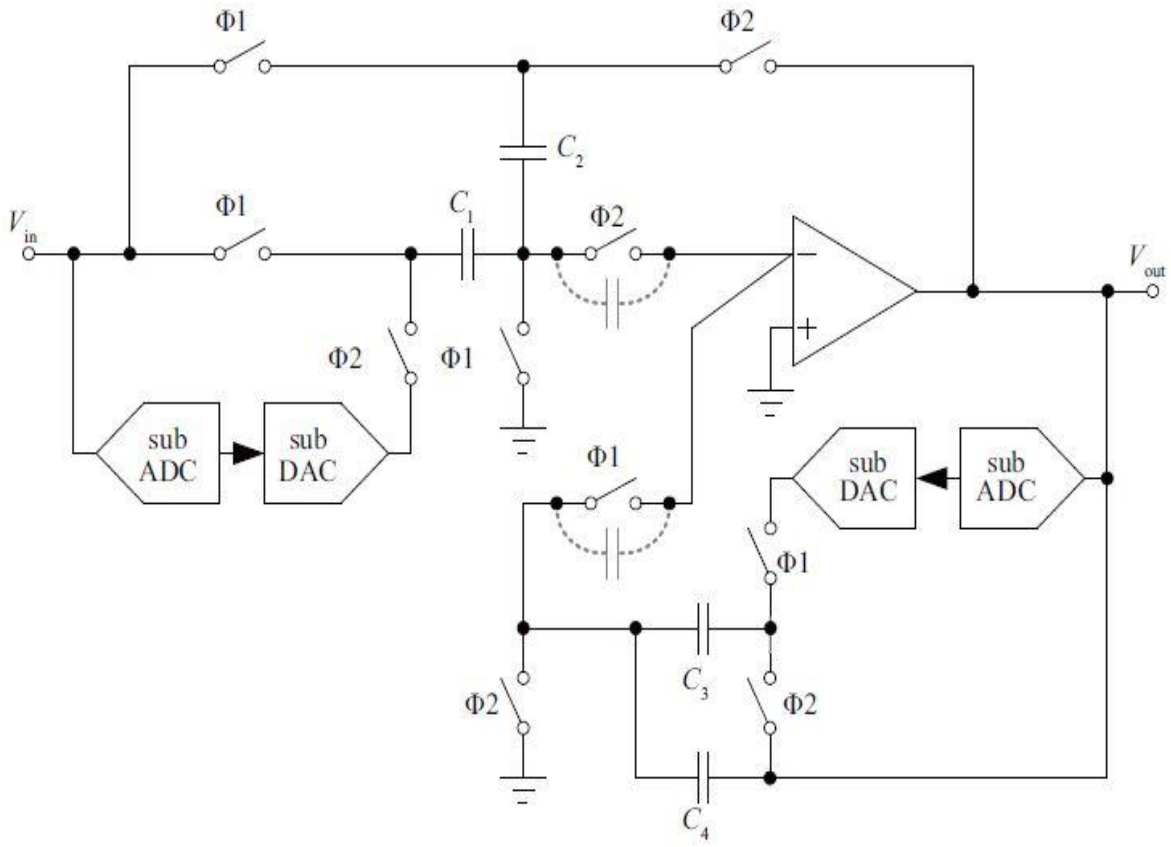


Figure 5.2: Conventional opamp-sharing MDAC

5.3 Switch-embedded OTA:

To get rid of the problems of non-resetting and successive stage crosstalk, an opamp-sharing pipelined ADC using a switch-embedded MDAC with dual NMOS differential input pairs current-reuse OTA controlled by two-phase overlapping clocks. The topology of the switch-embedded gain boosting telescopic OTA with dual NMOS differential input pairs is shown in Fig. 5.3.

Each input transistor (M1–M4) is connected with an embedded NMOS switch (M5–M8) in series. The switch is on when its corresponding control signal (i.e., Φ1Dn and Φ2Dn) is high, and is off when the control signal is low. In [18], OTA employs dual-NMOS input differential pairs but needs two different common-mode input voltages for resetting. This methodology is restricted to telescopic cascode OTAs, which have most power efficiency and result in loss of output swing. The adding switch also reduced the OTA DC gain AOL and GBW in Φ2 due to the on-resistance of the switches.

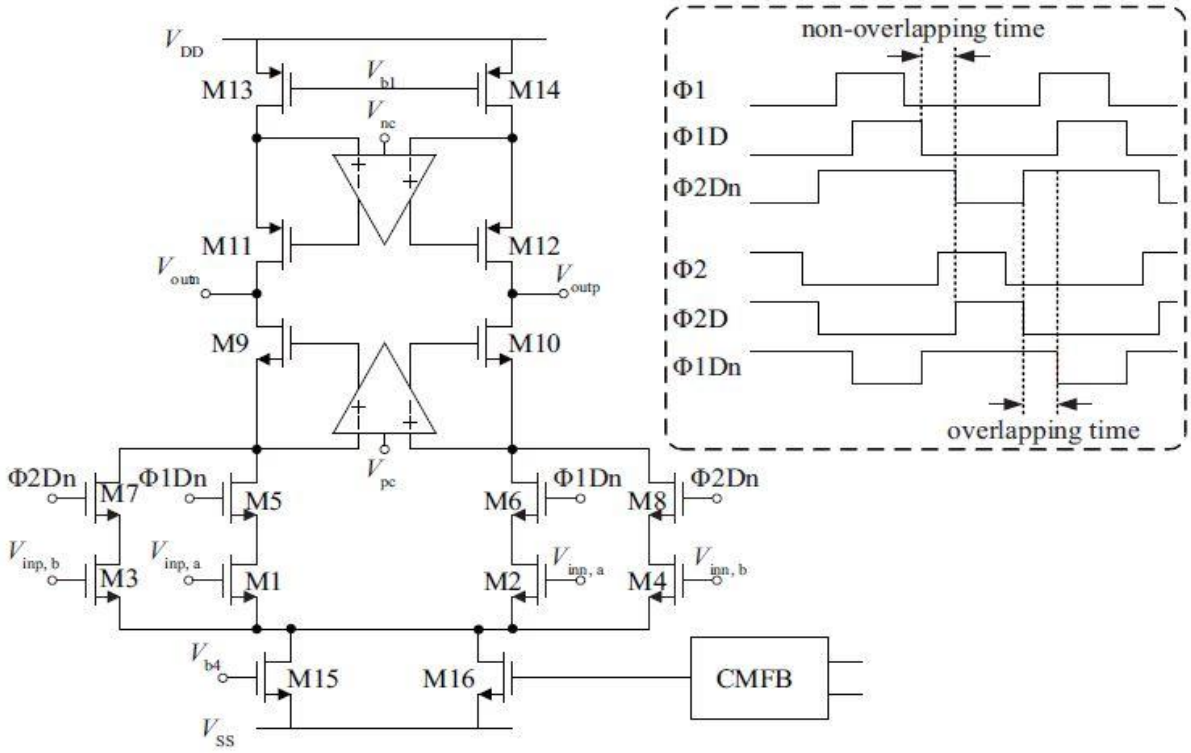


Figure 5.3: Two-input-differential-pair gain-boosting telescopic amplifier with clock timing.

5.4 Dual-input MDAC:

The proposed 1.5-bit opamp-sharing MDAC using the switch-embedded amplifier is shown in Figure 5.4. When Φ1 is high, both Vinp; a and Vinn; a are connected to the common-mode input voltage Vicm for resetting. When Φ1D is high, the sampling switches are on and C1a and C2a sample the input signal for stage-A while the opamp is working on holding mode for stage-B. At the end of the sample process, Φ1 turns to low before Φ1D, which is so called “bottom plate sampling”. At the moment after the bottom plate sampling switch is completely off and the previous signal is still holding, the sub-ADC compares the result, passes the 2-bit digital codes to the sub-DAC and the digital error correction module. During the overlapping period of Φ1Dn and Φ2Dn, the opamp is working on dual input- on mode. During this time, both pairs of input are active and have a half current, but are still in saturation. When Φ2D is high, the signal pathway is on. Meanwhile, Vinp; b and Vinn; b are disabled since Φ2Dn goes low, Vinp; a and Vinn; a are the only active inputs and the opamp is working on holding mode for stage-A.

Since both input pairs are reset to a common-mode input voltage alternately, the memory effect is completely eliminated without needing any additional clock phase. Furthermore, the opamp-sharing switches are embedded into the opamp instead of in

series between the sampling capacitors and the opamp inputs; therefore the crosstalk path is avoided. In addition, since the opamp-sharing switches do not connect directly to the opamp input transistors, the charge injection and the signal dependent resistance do not exist for the same reason.

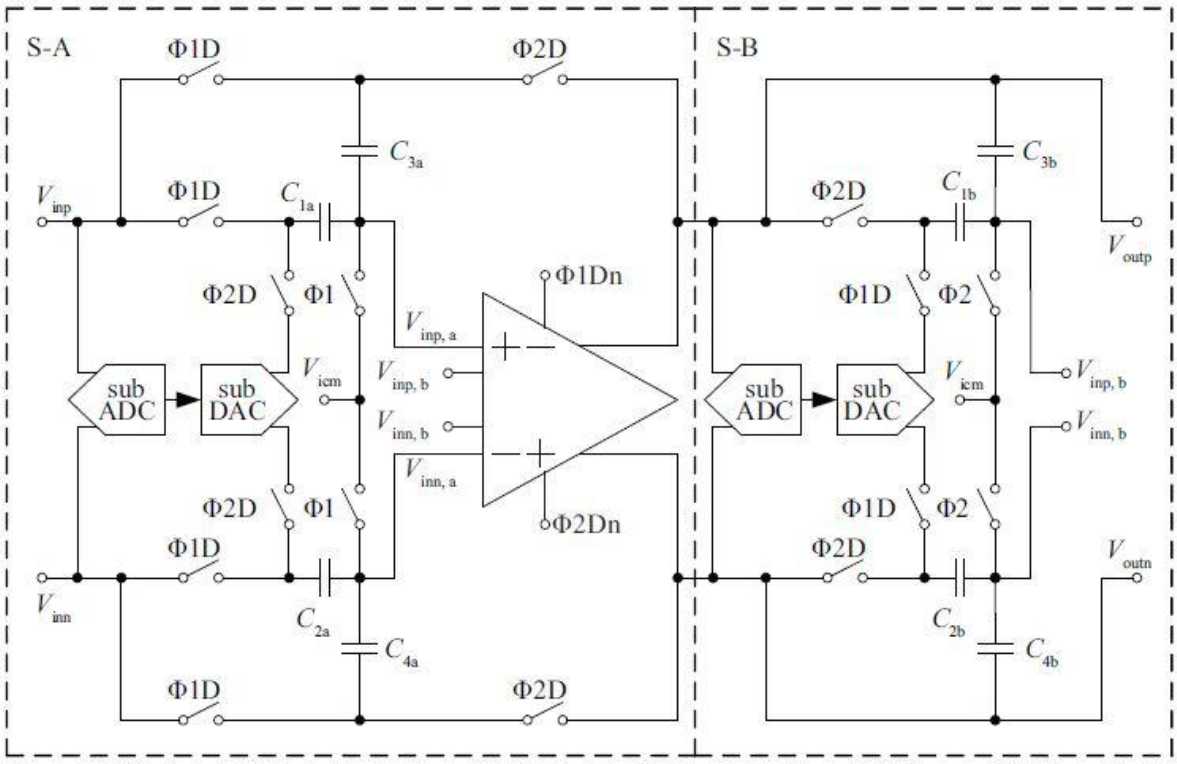


Figure 5.4: Proposed opamp-sharing MDAC

5.5 Timing consideration:

The two-phase non-overlapping clock is always used in a pipelined ADC but is not suitable for controlling the opampsharing switches in the proposed OTA. If the non-overlapping clocks Φ1D and Φ2D are used, during the non-overlapping period, both pairs of opamp input transistors will be disabled, so there is no current path to the ground for PMOS transistor branches (M11–M14). The output voltages of the shared opamp will shift to a much higher level above the common output voltage during this period. In the worst case, PMOS transistors may enter into the linear region and the holding phase of MDAC stages would waste sometime in the large-signal slew rate. Therefore, the proposed opamp uses two-phase overlapping clocks (Φ1Dn and Φ2Dn) to avoid this problem. Since Φ1Dn and Φ2Dn are already used for CMOS switches; no additional clock phase is needed. The use of an overlapping working scheme will not affect the fidelity of signal transfer, settling or the quantization process. On the one hand, during the overlapping period, the shared opamp has

not been working for signal settling until Φ1D/Φ2D is high. Signal transfer and settling will not be affected because there is no charge leakage path and two input differential pairs will not affect each other. Further, the opamp input transistors in saturation region in the overlapping period can improve the settling time. On the other hand, the comparing operation has already achieved at a moment between the falling edges of Φ1 and Φ1D, so the overlapping working has no adverse effect on the quantization process.

5.6 ADC architecture:

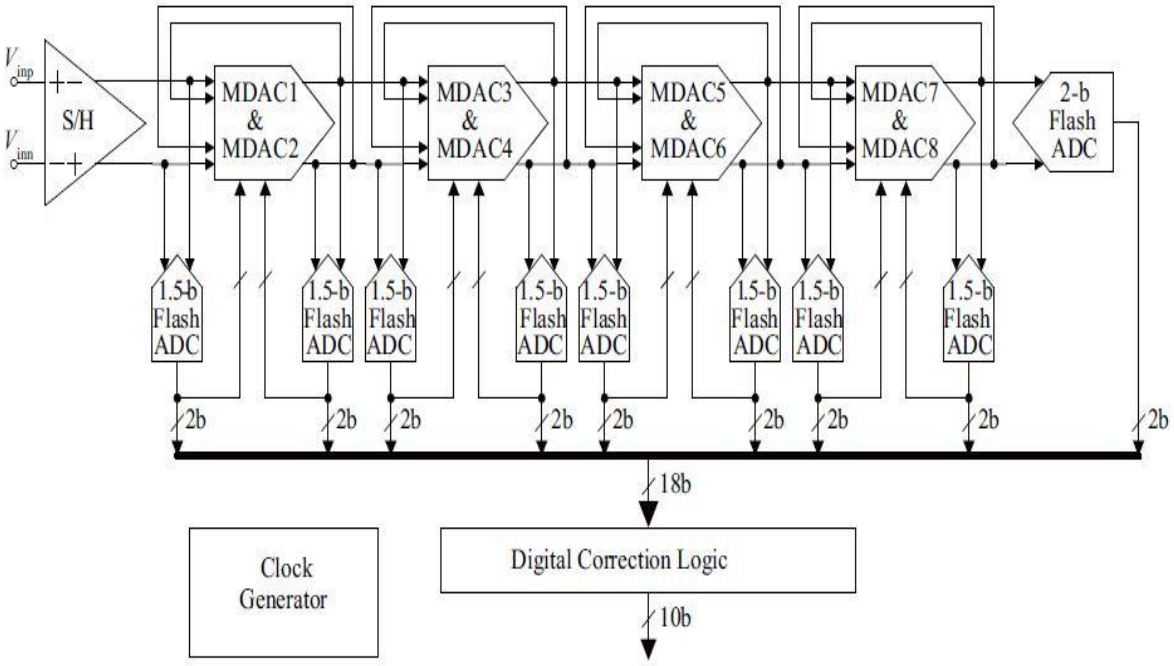


Figure 5.5:10 bit opamp sharing pipeline ADC

A common pipelined ADC configuration is used in this work, as shown in Fig. 4.20. The ADC is composed of an S/H circuit, eight 1.5-bit MDACs using four shared opamps, and a 2-bit flash ADC as the last stage. The ADC also has a distributed clock generation circuit, a digital error correction circuit. The input-sampling switch in the S/H circuit is bootstrapped, while the bottom-sampling switch is a symmetrical gate-bootstrapping one to increase linearity. Capacitor sizes are carefully chosen to meet matching and noise requirements. By using the technique of redundant-signed-digit (RSD) correction, which allows a large offset error for a simple latch-type comparator without static power consumption, the power consumption could be reduced further. Each stage processes data from the previous stage as soon as its output is passed to the next stage for sampling. The most efficient method that has been utilized to obtain significant power saving is opamp sharing between multiplying digital-to-analogue converter (MDAC) stages in pipelined

ADCs.That is because the signal amplification in each MDAC stage is in alternate phases, so the operational transconductance amplifier (OTA) only works in a half clock cycle. Therefore, half of the opamps can be removed, leading to nearly 50% power reduction.

5.7 Reconfigurable Data Converter:

Reconfigurable data converters have become more popular in research recently because of their ability to increase power efficiency for systems with variable speed and resolution requirements. The reconfigurable tag refers to the fact that the ADC is able to change its operable sampling rate, resolution, or both after fabrication. The resolution or sampling rate configuration range depends on the requirements of the system for which the converter is being designed for. Some popular implementations for reconfiguration will be described in the following subsections.

5.8 Sampling Rate Reconfigurable:

The sampling rate of an analog-to-digital converter refers to the rate at which a single analog sample is converted to a digital output. Data converters are typically mixed-signal circuits (they consist of analog and digital circuitry). Since digital circuits can easily operate much faster than analog circuits, the limiting factor in ADC operation speed is generally the analog circuitry, or specifically, the amplifiers and comparators.

(a) Bias Current Scaling

The bandwidth of an amplifier is proportional to the bias current as can be seen from Equations 5.1 and 5.2, assuming square-law saturation operation

$$GBW = \frac{gm}{2\pi Cload} \qquad (5.1)$$

$$gm = \sqrt{\frac{2Id\mu nCoxW}{L}} \qquad (5.2)$$

Thus, a common method of configuring the sampling rate of a data converter is through adaptive biasing. Adaptive biasing, as the name implies, results when the bias currents of the analog blocks are adjusted so that they achieve the desired bandwidth for a conversion. By increasing and decreasing the bias currents, the ADC can more efficiently operate with a higher or lower sampling rate, respectively.

5.9 Resolution Configuration:

For a pipelined ADC, there are two ways to configure the resolution,turning off the beginning stages or the ending stages as illustrated in Figure 5.6. The second method is generally easier than the first as it does not disrupt the pipeline. The first method disrupts

the pipeline and requires re-routing of original signal from the main sample-and-hold amplifier to stage 3. Although, using the beginning stages adds slightly more complexity, the added power efficiency outweighs this drawback. An analysis of the resolution configuration scheme, a potential drawback, and a solution to that drawback is carried out here.

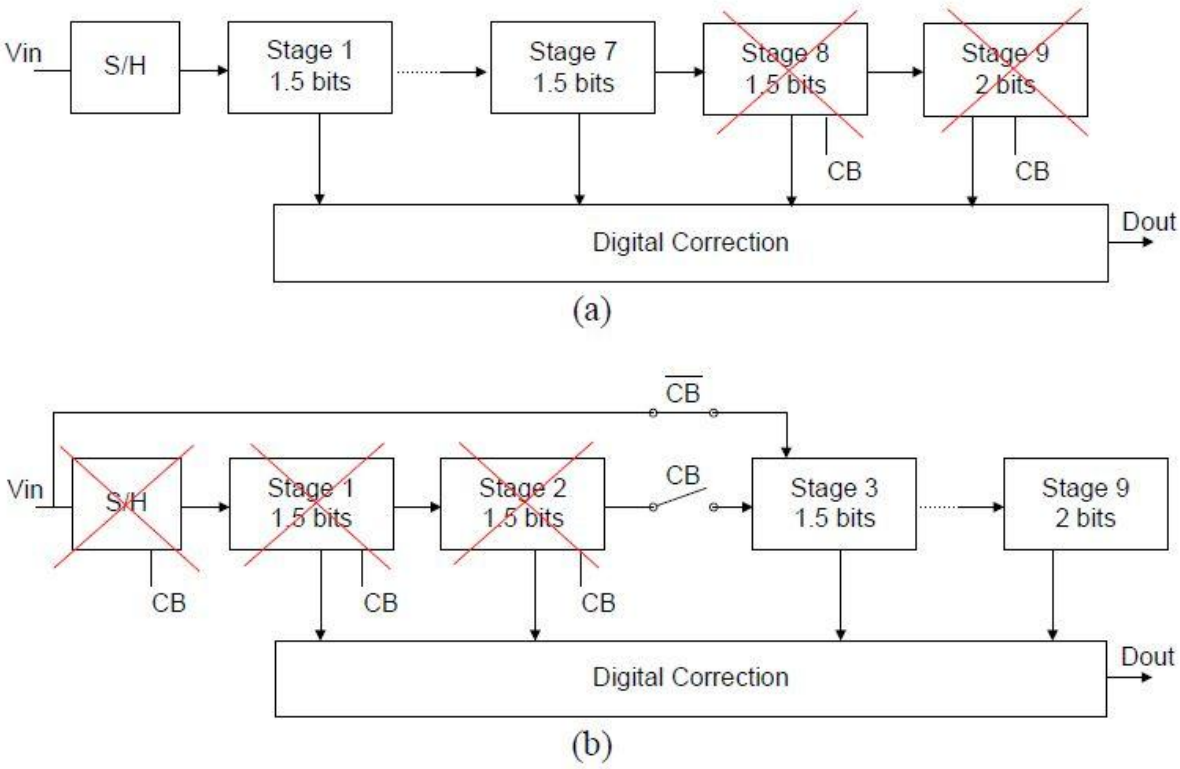


Figure 5.6: Two possible reconfigurable resolution schemes for pipelined ADC.

(a) Power in Pipeline Stages:

The later stages of a pipelined ADC generally consume far less power than the earlier stages because the earlier stages require more accuracy. For instance, the SHA of a 10-bit pipelined ADC requires 10-bit accuracy. Another way of saying this is the SHA is allowed 1 part in 2^{10}, or 0.1%, error. The next stage needs 9-bit accuracy, or 0.2% error is allowed, and so on.This error includes all non-idealities such as finite gain, dynamic settling error, slewing, charge injection, noise, interference, etc. In order to achieve high accuracy in the earlier stages, more current is used to increase the bandwidth and the slew rate, and lessen the effects of noise. Current is then slightly relaxed in the later stages to save power as accuracy requirements are diminished. As a result, using the beginning stages for resolution configuration achieves more power efficiency. A graph of the normalized power consumption of each pipeline stage is shown in Figure 5.7. It is clear that the earlier stages use significantly more power than the later stages for the reasons expressed above. Using the

beginning stages for reconfiguration also eliminates an extra stage, the front end sample-and-hold amplifier, which further improves power efficiency.

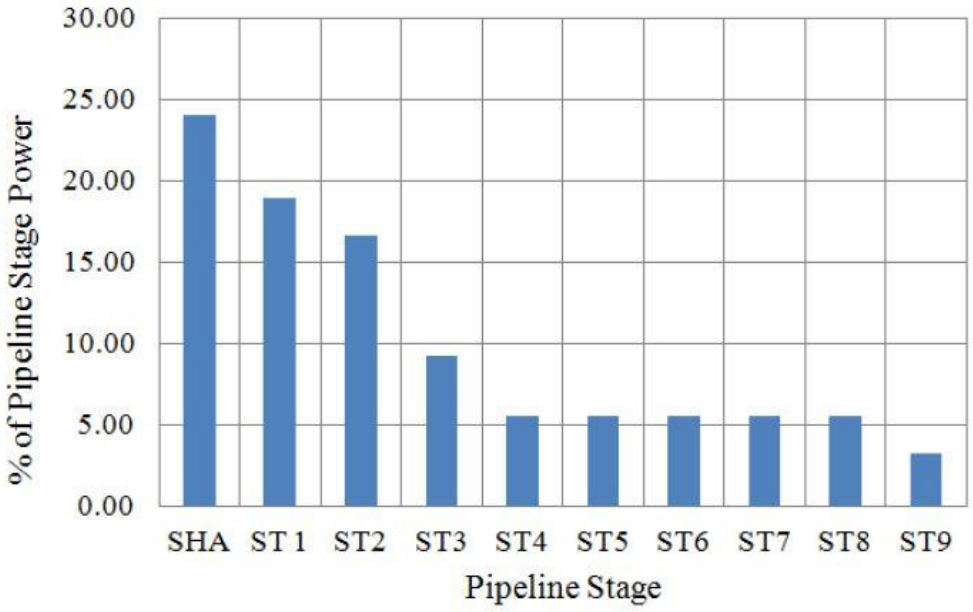


Figure 5.7: Normalized power consumption for pipelined converter stages.

CHAPTER 6

6.1 Comparator:

Comparator is the most essential block to quantize an analog signal because it provides digital information with respect to the analog input. Comparator needs to provide high gain but the circuit doesn't have to be linear. And phase margin is not important because it doesn't use negative feedback**.** A simple plot is shown in Figure 6.1

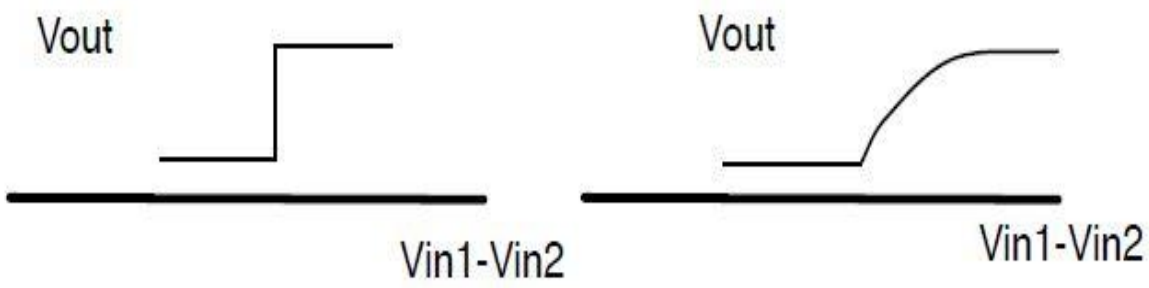


Figure 6.1 Characteristic of comparator in ideal (left) and practical (right) cases

As shown above, ideal comparator resolves the correct result even from infinitely small input difference. But in practical condition, comparator takes very long time to resolve when input difference is very small. This can be understood by the inherent time constant of a comparator. Since latch is usually a key block in comparator, it's useful to evaluate the behaviour of latch**.** Figure 6.2 shows the model of cross-coupled inverter latch.

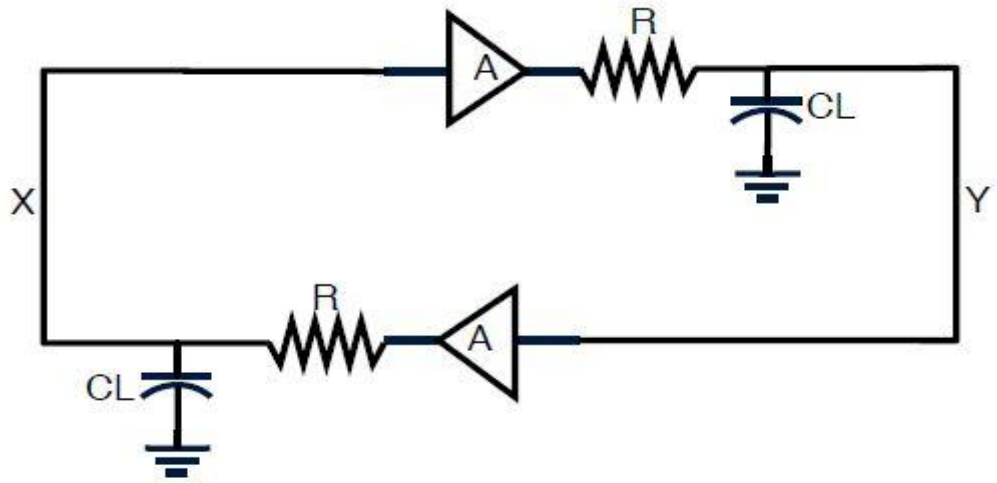


Figure 6.2 Model of cross-coupled inverters

Equations for X and Y are:

$$RC_L\frac{dV_X}{dt}+V_X=AV_Y$$

$$RC_L\frac{dV_Y}{dt}+V_Y=AV_X$$

Therefore, voltage difference between X and Y is:

$$V_{XY}=V_{XY0}e^{\frac{t}{\tau}},where\ \tau=\frac{RC_L}{-A-1}=\frac{RC_L}{g_mR-1}$$

If gain is larger than one, time constant is positive. Thus, exponential increase can be found in the characteristic of latch. However, for infinite small initial voltage difference, the resolving time for latch will be infinite large. Since comparator is clocked in ADC scenario, the resolving time must be smaller than one clock cycle. So the input voltage resulting in very large resolving time defines meta-stability region.

6.2 Comparator architecture:

Meta-stability region is not desired, so high gain is necessary in comparator. The problem associated with this is the input offset. Since a small offset will be regenerated due to high gain, there comes trade off between gain and mismatch requirement. To release this effect, comparator usually consists of a pre-amplifier as shown in Figure 6.3.

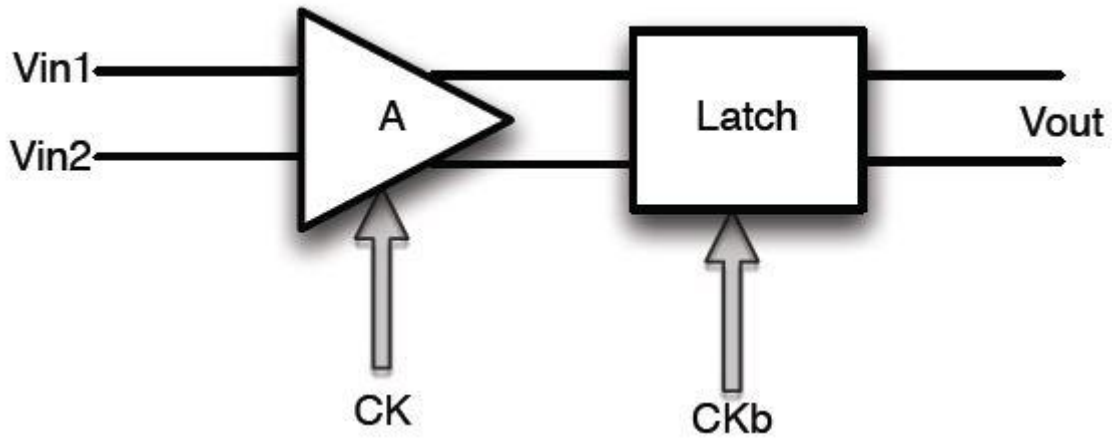


Figure 6.3 Comparator architecture

When CK is high, amplifier will amplifier the input voltage difference and latch is not triggered. When CKb is high, latch will regenerate the voltage to digital level.

Due to the existence of pre-amplifier, gain of latch need not be very high, thus the offset requirement is released.

6.3 Flash ADC:

The block diagram of a typical flash ADC is shown in Figure 6.4. A track-and-hold samples the continuous-time input and holds it for half a clock cycle. This held value is compared against a set of references, typically generated using a resistor ladder. In practice, there will be offsets in the comparators, which need to be corrected. The comparator outputs are processed by the digital back end to yield an *N*-bit digital word that is representative of the continuous-time input. The track-and-hold is not strictly necessary, as one could use the inherent sampling properties of the comparators to sample the input. However, clock skews in the comparator array are bound to result in poor dynamic performance. It has therefore become commonplace to use some form of track-and-hold mechanism at the input of a flash converter. The comparator array now processes a "held" signal, so that clock skews are no longer an issue. The track-and-hold also serves to drive the large capacitance of the comparator array while presenting only a small load at the converter input.

Incorporating a track-and-hold upfront causes several problems. Since this necessarily will be operating at high speeds, it is usually not possible to use feedback-based linearizing techniques– fast, open-loop circuits are called for. These open-loop track-and-hold circuits exhibit significant static nonlinearity (nonlinearity which is independent of input frequency), causing distortion, thereby limiting the peak input signal swing of the converter. Reduction of input swing results in a smaller LSB size, so offsets in the comparator need to be smaller. This leads to increased device sizes (and parasitic capacitances) in the comparators. This in turn necessitates higher bias currents in the track-and-hold, as well as increased digital power since clocks have to be routed over longer distances. It is thus seen that use of a larger input swing (while somehow eliminating distortion) could reduce power dissipation of the entire ADC.

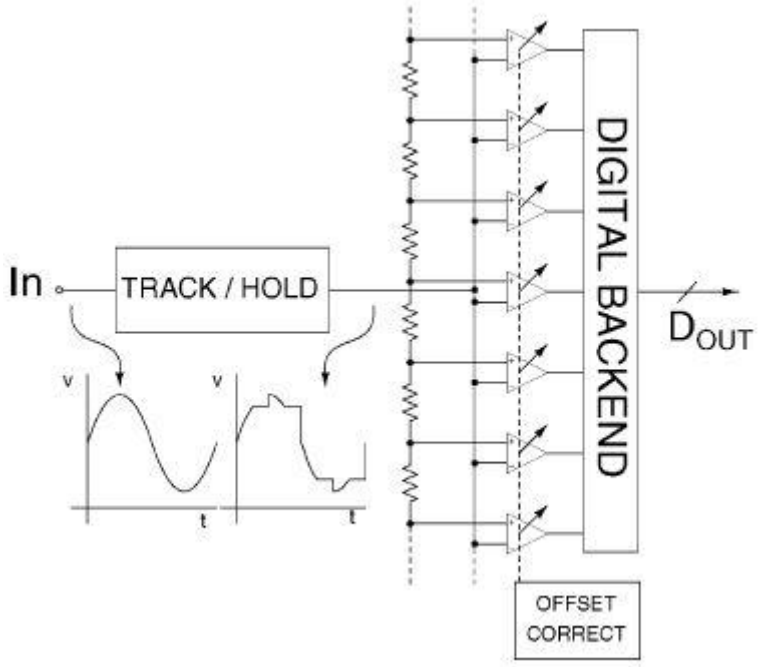


Fig.6.4. Block diagram of a generic flash ADC.

6.5 Comparator:

A simplified schematic of the comparator and representative waveforms during its operation are shown in Figure 6.5. It consists of a preamplifier and a latch. The preamp gain effectively reduces latch offset when referred to the comparator input. During regular operation, the auto zero signal AZ is low. The preamp inputs are connected to the track-and-hold outputs. The switches are operated according to the timing diagram shown in Figure 6.6. When the T/H output is tracking the input signal, the preamp is reset by making PRST high. It begins to amplify when PRST goes low. The preamp outputs are connected to the latch inputs through the switches LC, so that the latch input capacitances can be charged to an amplified version of the preamp differential input. While the latch is being charged regeneration is disabled by making LE low. Once LC goes low, LE goes high so that the latch can regenerate. During this time, the preamp is reset again. At the end of the regeneration period, the decisions are processed by the majority logic and the rest of the digital back end. The latch is reset so that memory of past decisions is removed.

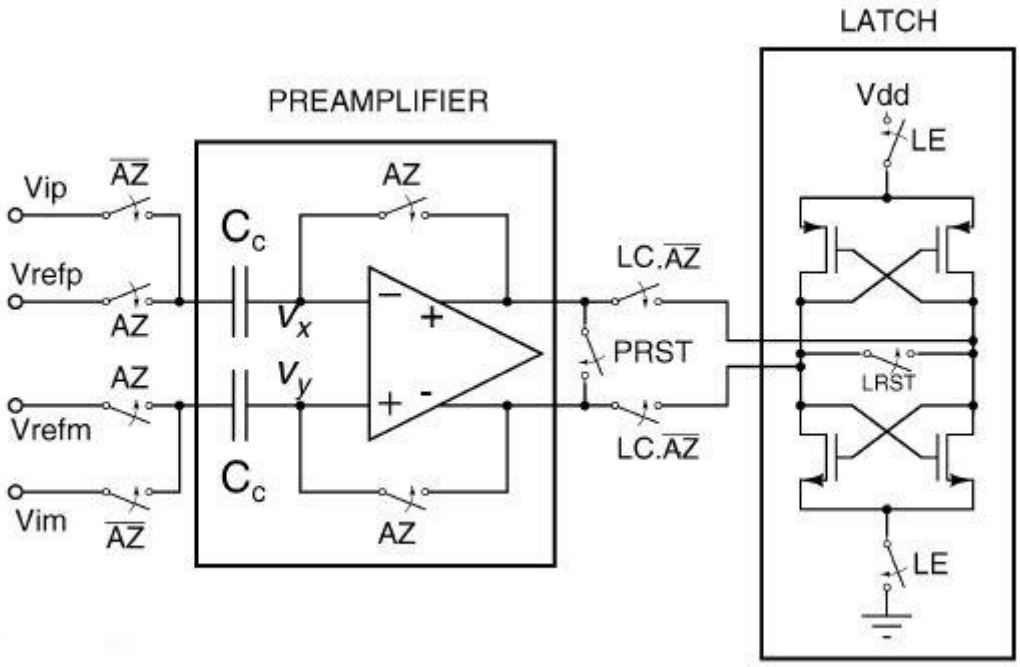


Fig.6.5. Comparator schematic

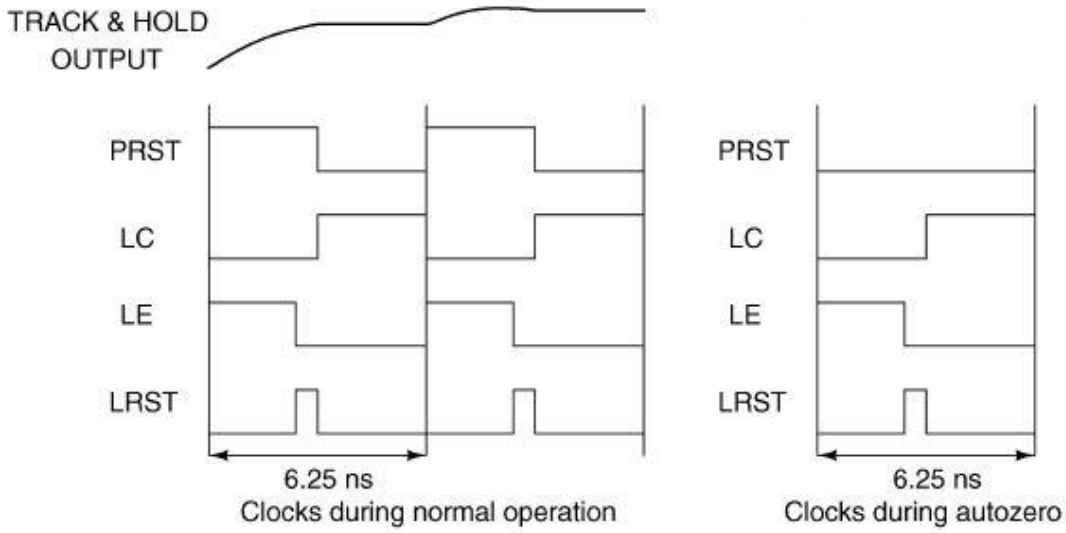


Fig.6.6. Timing diagram of the clocks

Preamp offset is cancelled during an auto zero phase (AZ). When AZ is high, the input of the preamp is disconnected from the T/H output (Vip and Vim). The preamp reset signal is set to zero and the inputs are connected to the desired references (Vrefp and Vrefm), generated by the nonlinear reference generator. If the DCgain and input referred offset of the preamp are Apre and Voff respectively, it can be shown that during the AZ mode,$Vx - Vy = Voff.\frac{Apre}{1+Apre}$

In regular operation (AZ low), the input to the amplifier is

$$Vx - Vy = (Vip - Vim) - (Vrefp - Vrefm) - Voff.\frac{Apre}{1 + Apre}$$

The LE and LRST signals are still active during auto zero, so that the latch puts out a random decision when the preamp is being auto zeroed.

6.6 Preamplifier:

The schematic of the preamplifier is as shown in Figure 6.7. M2 and M3 constitute the input pair of the preamplifier. M6 and M7 provide common mode feedback. These transistors are operated in the saturation region to maximize the bandwidth of the common mode feedback loop. M4 and M5 are active loads; hence the preamplifier works as an integrator resulting in a large dynamic gain.

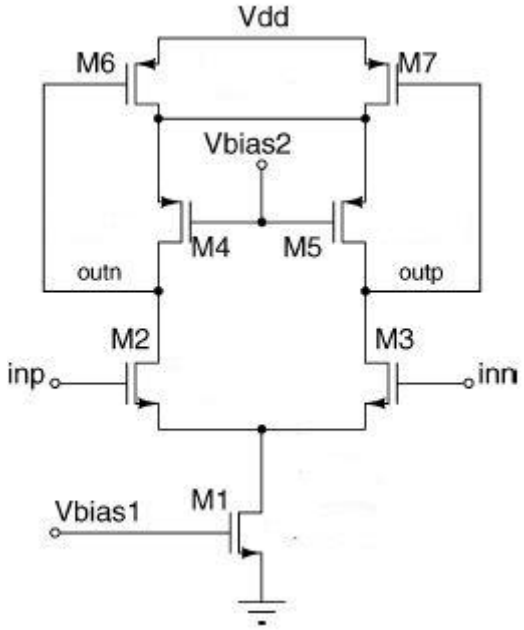


Figure 6.7. Schematic of the preamplifier

6.7 Reference voltage generator for 1.5bit and 2bit flash ADC:

Dynamic range of the pipeline ADC has been set as Vp-p = 1200 mV. Since the analog blocks are fully differential in nature, the input signal is fed with a 900 mV dc bias. A dynamic range of 600 mV is required for each of these differential ends.

Where VCM = 900 mV, Vref = 300 mV, Vref/4 = 75 mV which implies a single ended full-scale range of (VCM +Vref)-(VCM -Vref) = 600 mV. Since the last stage

Of the ADC is a 2 bit ash ADC, it would require two more reference voltages of VCM + 3Vref/4 and VCM - 3ref/4 . In Figure7.8 V1, V2, V3 are reference voltages for 2bit flash and 1V, 2V are reference voltages for 1.5bit flash ADC.

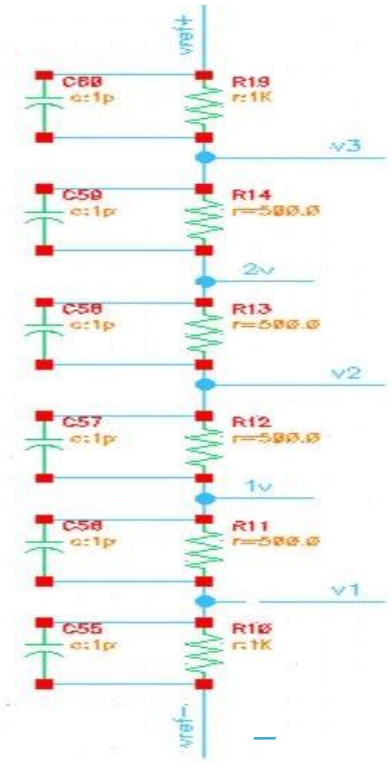


Figure 6.8: Schematic of reference voltage generator

$Vref$/Vcm-Vref=600mv

Vref+=Vcm+Vref=1.2v

As we know threshold voltages of 1.5bit flash are at 1.5Vlsb and 2.5Vlsb so their values are given as

1V=1.5Vlsb= (Vref-)+1.5*2Vref/4=Vcm-Vref/4=825mv

2V=2.5Vlsb= (Vref-)+2.5*2Vref/4=Vcm+Vref/4=975mv

As we know threshold voltages of 2bit flash are at 1Vlsb, 2Vlsb and 3Vlsb so their values are given as

V1=1Vlsb= (Vref-) +1*2Vref/4=Vcm-Vref/2=750mv

V2=2Vlsb= (Vref-)+2*2Vref/4=Vcm=900mv

V3=3Vlsb= (Vref-) +3*2Vref/4=Vcm+Vref/2=1.05v

Chapter 7

Nonopamp and low power based MDAC techniques:

7.1 Comparator based switched capacitor MDAC:

While the opamp is a key component in a pipeline stage, it is generally the most power hungry and it scales poorly with CMOS technology. A lot of current research in pipelined ADCs involves designing stages without the use of opamps, and instead using a circuit that is less power hungry and scales better. Recent technology scaling in CMOS process makes it more and more difficult to design a high-gain high-speed opamp due to a low intrinsic gain of transistors and an operation under a low supply voltage. Particularly, for high-resolution high-speed data converters in deep sub-micron technologies, it is challenging to implement switched-capacitor circuits which require a high-performance opamp for precise charge transfer.

One approach to solve the issues from technology scaling in high-performance data converter designs is to adopt digital calibration techniques.Another approach is to utilize a comparator-based switched-capacitor (CBSC) circuit which replaces a power consuming opamp with a combination of a comparator and current sources to implement a same charge transfer operation as opamp-based switched-capacitor circuits [19]. Since a CBSC circuit excludes opamps and does not require stabilizing a charge transfer feedback loop, it is amenable to designs in deep sub-micron technologies with potential for low-power operations. CBSC circuits, however, introduce linearity problems such as output overshoots and voltage drops across switches.

In conventional switched-capacitor circuits, the opamp is mainly responsible for providing a virtual ground to ensure accurate charge transfer from sampling to feedback capacitors [20]. Instead of using an opamp to generate a virtual ground, CBSC circuits use a comparator in a feedback loop to effectively emulate the functionality of an opamp with a large DC gain. Figure 2.20 depicts a CBSC circuit which provides a gain of two.

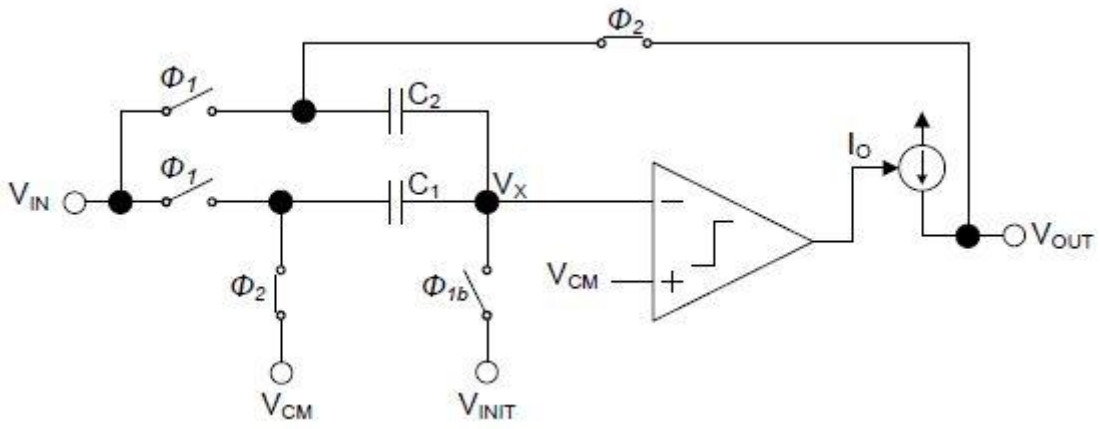


Figure 7.1 Comparator-based switched capacitor circuit implementing a 2x circuit.

During Φ_1, the input is sampled on capacitors C_1 and C_2, and the node V_X is initialized to be below V_{CM}. This is different than the case when an opamp is used in which case V_X would be initialized to V_{CM}. During Φ_2, the current source at the output, I_O, is turned on and V_{OUT} and V_X subsequently increase. When V_X equals V_{CM}, the comparator toggles and turns off the current source I_O, and the node voltages at V_X and V_{OUT} appear the same as if an opamp were used to create a virtual ground at V_X. Thus the CBSC arrangement implements the same functionality as an opamp based arrangement (i.e. gain of 2x).

The significant advantage of CBSC is that the topology does not depend on an opamp which would otherwise require a large DC gain and/or large supply voltage to implement the same functionality in a switched-capacitor circuit. As comparators can be easily designed even with low supply voltages and with transistors that have low intrinsic gain, CBSC is well suited for implementation in deep submicron technologies. Furthermore in [33] it is shown that the CBSC approach has less inherent thermal noise than an opamp based approach and thus is able to use smaller sampling capacitors, hence have lower power consumption. One of the drawbacks of CBSC is thus far the technique has only been shown in single-ended form and not the more desirable differential form. As such, it is susceptible to common mode noise.

7.2 Ring amplifier based switched capacitor MDAC:

Ring amplifier essentially a stabilized offset cancelled three stage inverter, has the benefit of slew based charging. In addition, ring amplifiers have a near rail-to-rail output swing because the output Stage is a simple inverter that operates in sub-threshold steady state. Ring amplifier based switched capacitor circuits use feedback just as conventional OTA based SC circuits do, and therefore the accuracy depends on the gain if thr

ring amplifier. The required gain can be relatively easily achieved from three gain stages. Requirement for external bias voltages limits the practically when we consider PVT variation.

7.3 Conventional ring amplifier:

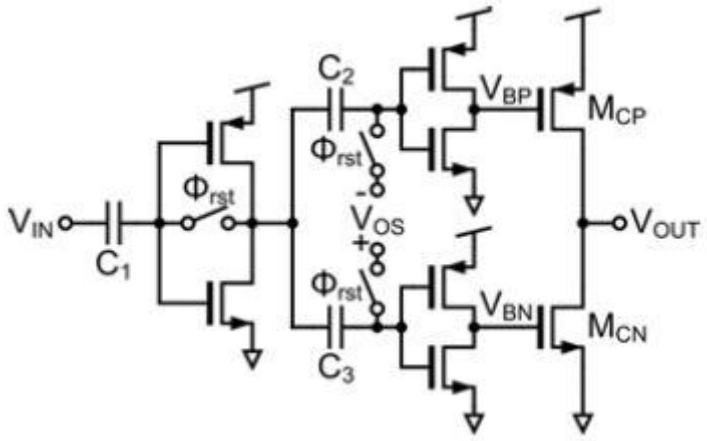


Figure 7.2: Conventional ring amplifier

Second stage inverter drives the gate of PMOS transistor of the third stage (VBP) while the other drives the gate of the NMOS transistor(VBN).The offset voltages of the two second stage inverters are turned to bias the third stage transistor, MCP and MCN in sub-threshold a VIN approaches VCM:

VBP>VDD-Vthp , VBN<Vthn

The capacitors C2 and C3 act as the floating bias offset voltage sources .An external bias voltage Vos, sets the capacitor voltages during a reset period. A positive small signal phase margin is a necessary but insufficient condition for stability of the ring amplifier. Conventional ring amplifier circuit has drawbacks because it depends on the external offset voltage Vos. The quiescent voltages of VBP and VBN ,when VIN=VCM, must be set within narrow voltage windows as illustrated in Fig7.3 If the quiescent overdrive voltages of the last stage are set too high then the ring amplifier can oscillate because the output resistance of the third inverter stage is never sufficiently large to create a sufficient phase margin. On the other hand if the overdrive voltage is too low the bandwidth of the last stage is reduced and the ring amplifier might not settle fully in the given settling time.

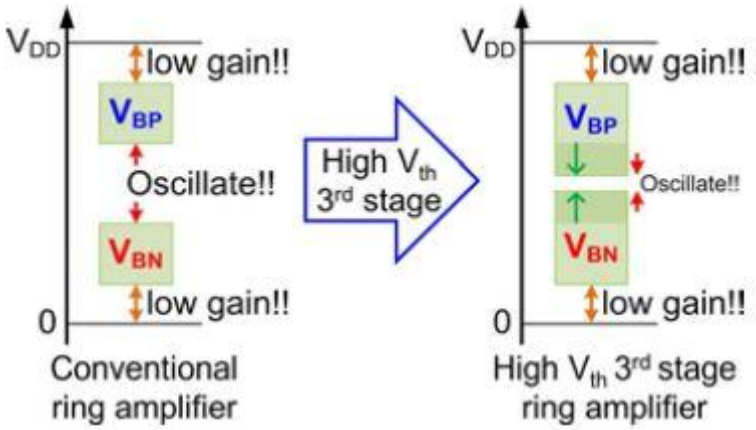


Figure7.3: Ring amplifier third stage quiescent offset voltage range

7.4 Self biased ring amplifier:

Here we adopt high threshold devices for the last stage inverter to extend the stable offset (VOS) range. We also eliminate the external biases and split second stage inverter. We dynamically apply an offset using a resistor in second stage to make the ring amplifier more practical and power efficient.

We introduce high threshold devices in the third stage of the ring amplifier to take advantage of their higher output resistance. Because we can get orders of magnitude higher output resistance from the high threshold voltage device inverter, we can extend the Vos range. This extended Vos range increases the robustness of the ring amplifier to PVT variation.

Adopting high threshold devices for the last stage allows us to stabilize a three-inverter stage amplifier without split second stage and offsets as shown in Fig7.4. This simple three stage ring amplifier has an advantage compared to conventional ring amplifier. Reduced number of second stage inverters, together with the removal of offset capacitors and switches reduces the loading of the first stage allowing us to reduce the power consumption of the first inverter.

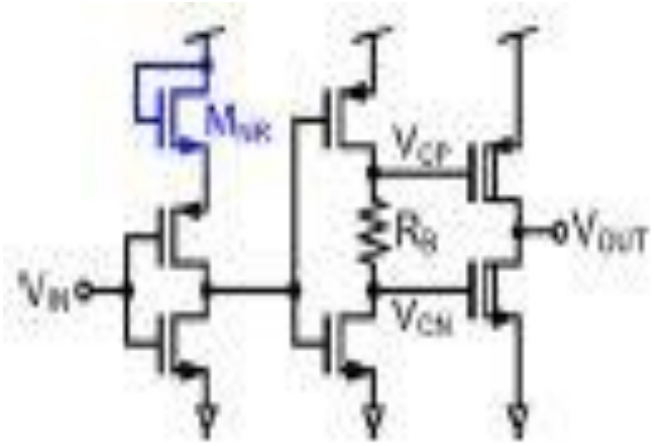


Figure 7.4: Self biased ring amplifier

7.5 MDAC with ring amplifier:

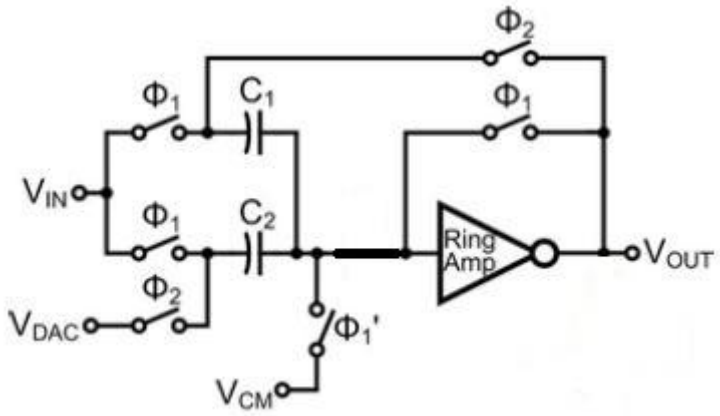
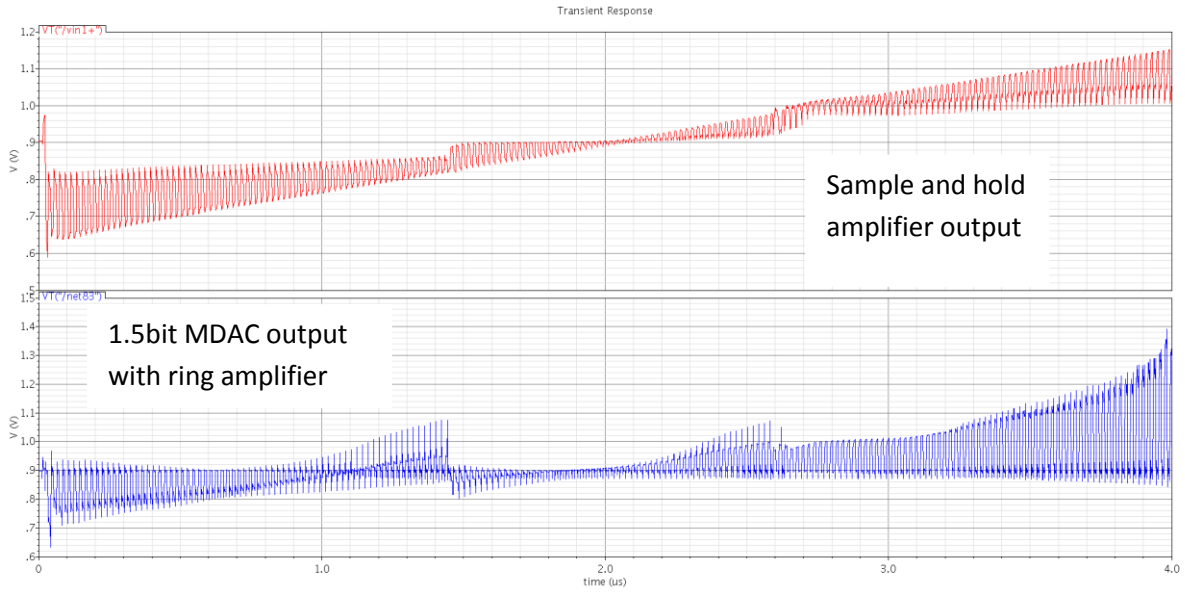


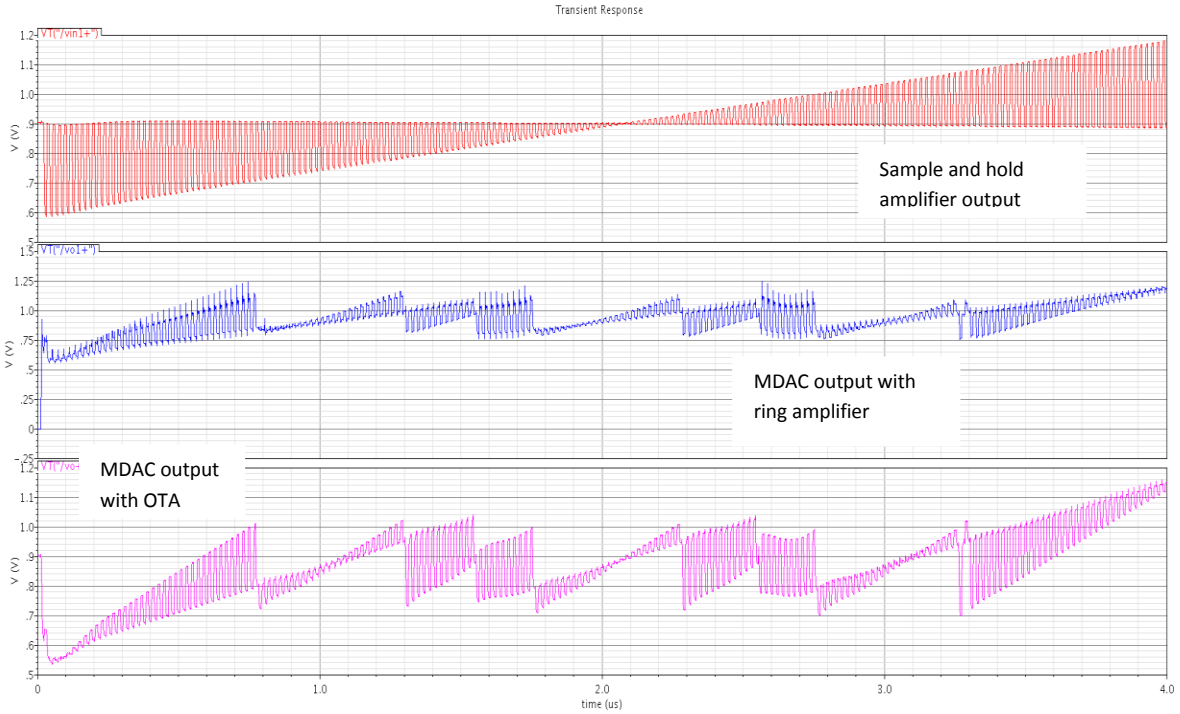
Figure 7.5: 1.5bit flip around MDAC with ring amplifier

Results:

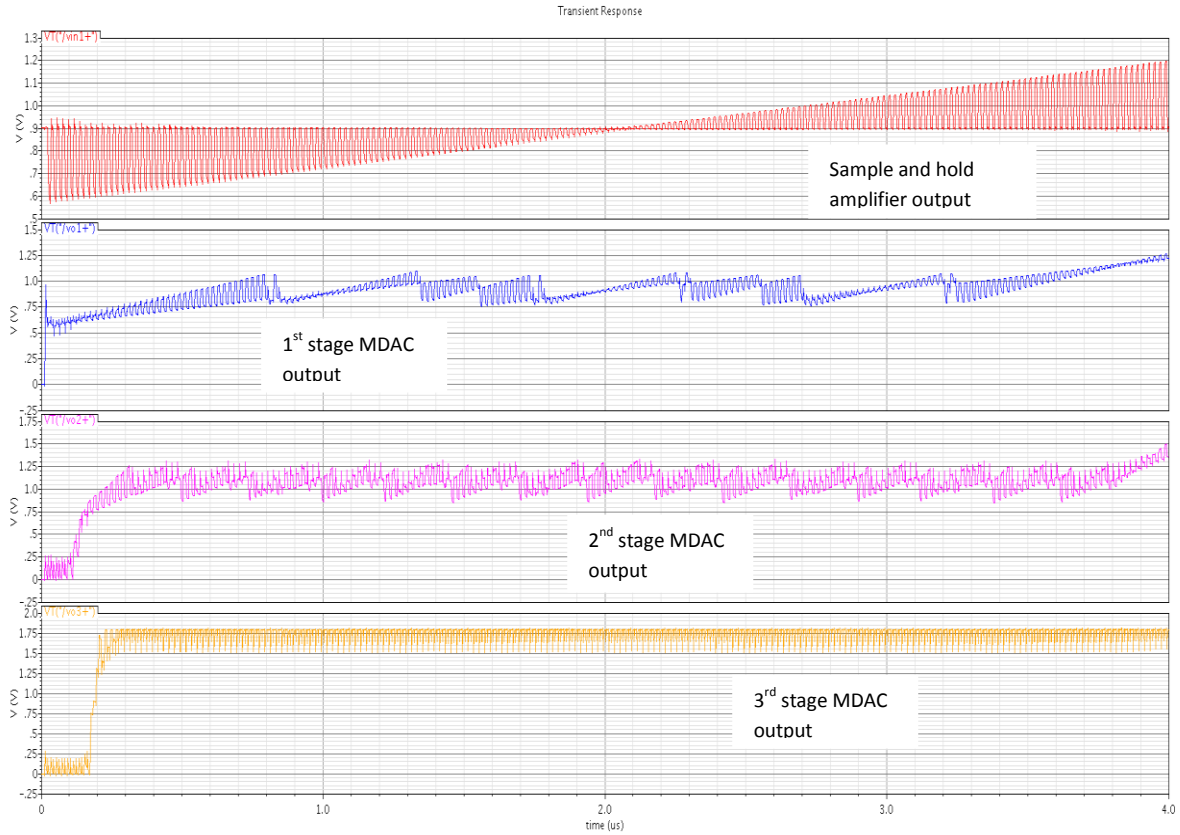
a)1.5 bit MDAC output of one stage with ramp input and without opamp sharing:



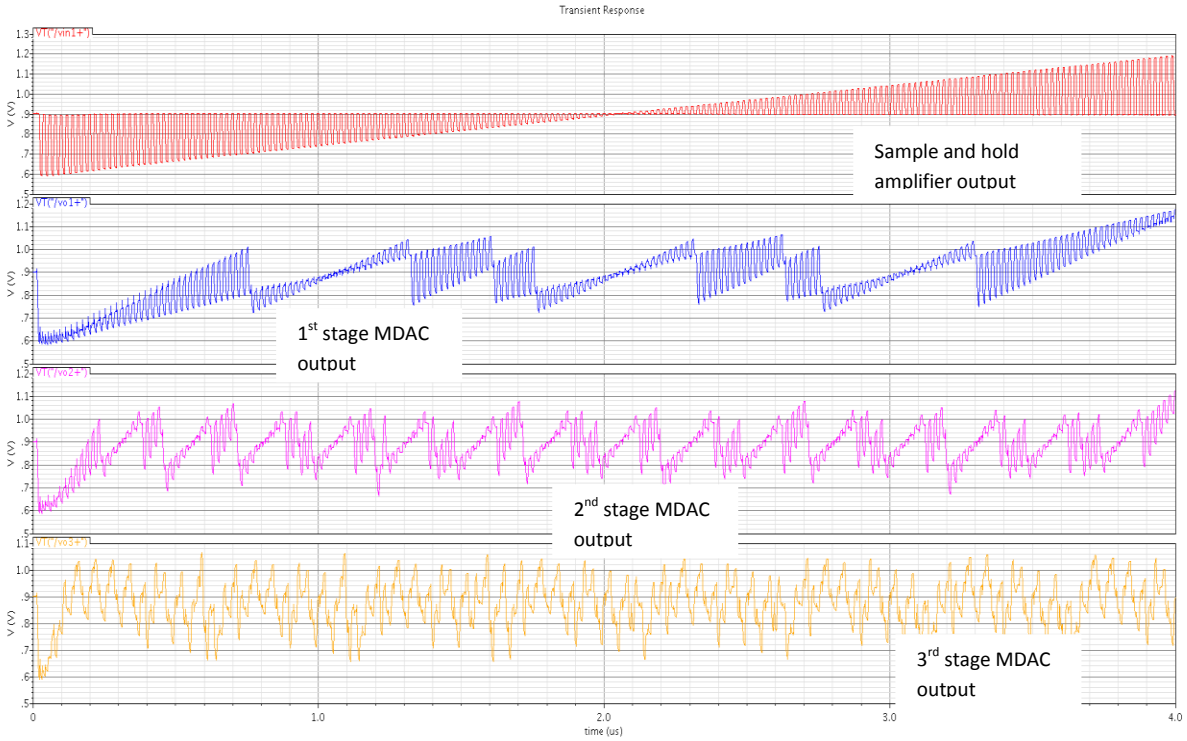
b)1.5 bit MDAC outputs of one stage with ramp input and opamp sharing:



c)MDAC outputs of three stages with ramp input and ring amplifier sharing:



d)MDAC outputs of three stages with ramp input and opampsharing using OTA:



e)Comparison table of low power MDAC techniques:

MDAC type	Sampling frequency (Fs)	Resolution	Power	FOM	Supply voltage
OTA	50MSPS	10	7.2mw	279fJ/conv-step	1.8V
Comparator [ref 8]	50MSPS	10	6mw	81fJ/conv-step	1.2V
Charge pump [ref 7]	50MSPS	10	4mw	300fJ/conv-step	1.8V
Ring amplifier [ref 6]	30MSPS	10	2.5mw	90fJ/Conv-step	1.3V

Chapter 8

Simulation results of ADC

8.1Nonoverlap clock generator:

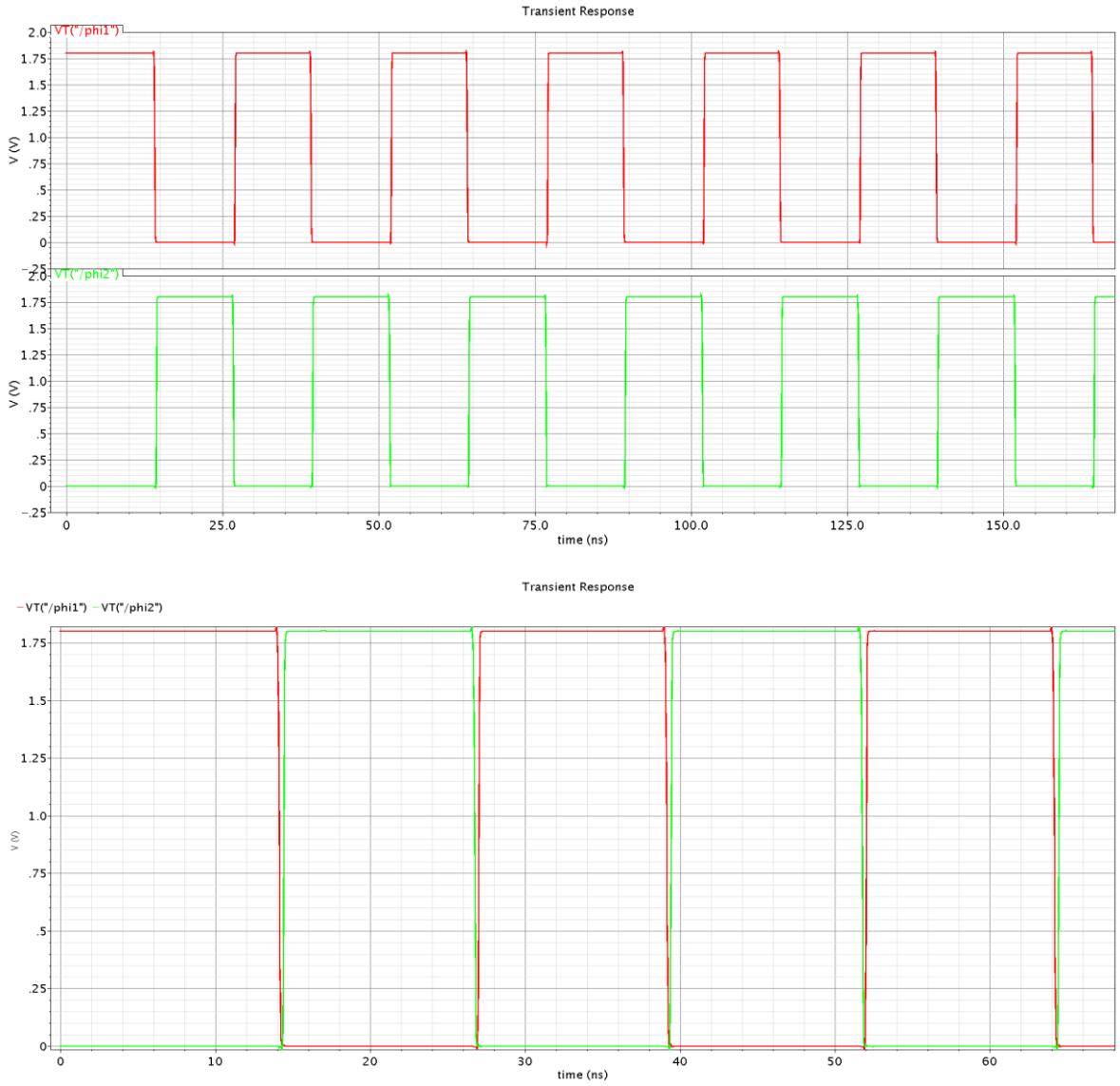


Figure 8.1: Transient simulation of nonoverlap clock generator

8.2 Sample and hold amplifier:

A ramp input is applied to sample and hold amplifier which varies from 0.6v to 1.2v. In phase Φ1 the input voltage is sampled across the capacitor and is given to flash ADC as its input. In Φ2 the amplifier stays in unity gain mode and Vcm (0.9v) is stored across capacitor.

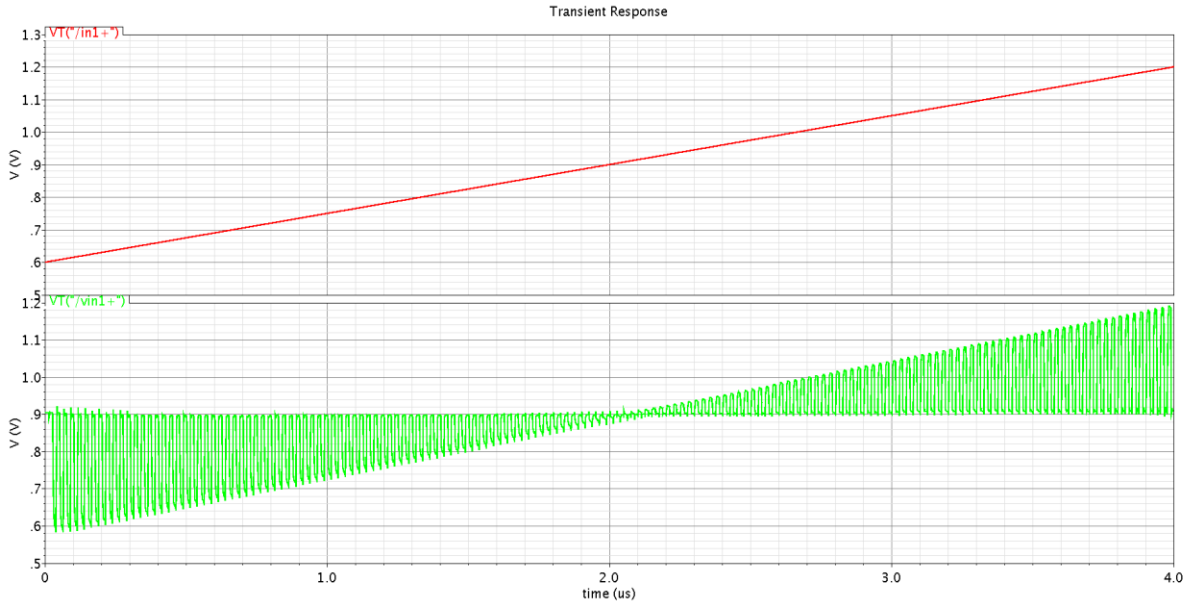


Figure 8.2: Transient simulation of sample and hold amplifier

8.3 1.5bit Sub ADC:

In the below figure we can see when voltage on capacitor of sample and hold amplifier crosses 825mv which is threshold voltage of first comparator in 1.5bit flash ADC then its output make transition from 0 to 1(0 to vdd). In the same way when output of sample and hold amplifier crosses the threshold voltage of second comparator which is 975mv then output of second comparator in 1.5bit ADC make transition from 0 to 1(0 to vdd).

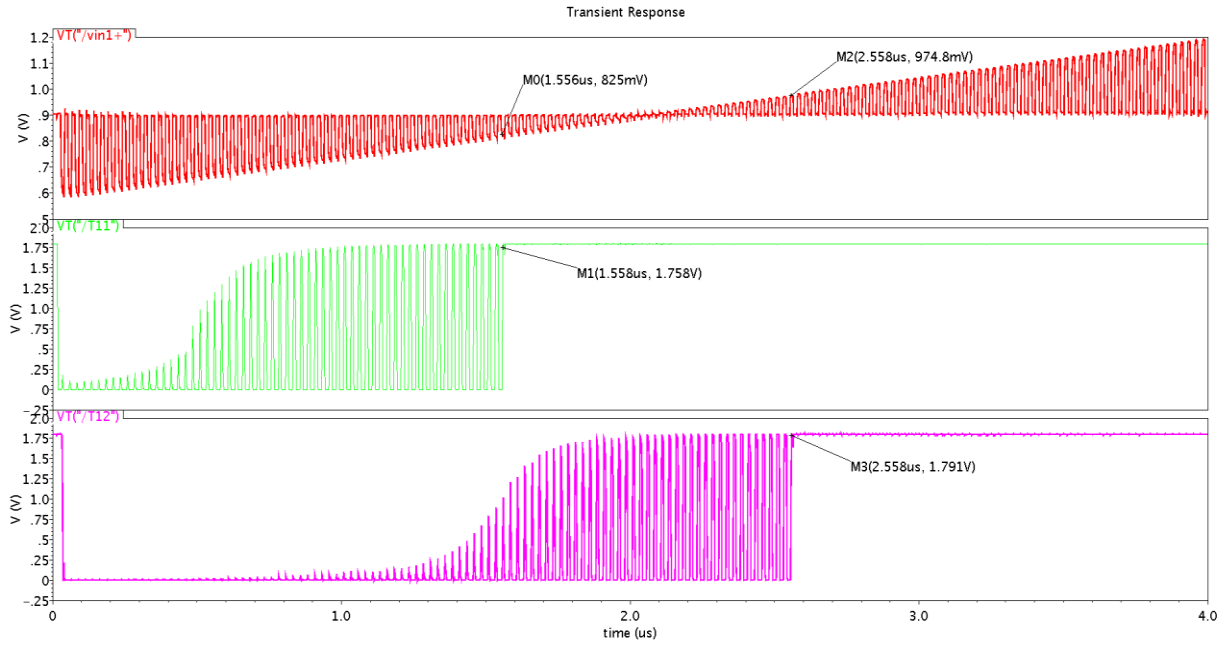


Figure 8.3: Transient simulation of the 1.5bit sub ADC

8.4 1.5bit encoder:

In the below figure T11 and T12 are outputs of flash ADC and s11 and s22 are outputs of encoder. The below figure follows Table 8.1 which is the operation of encoder.

T12	T11	S12	S11
0	0	0	0
0	1	0	1
1	1	1	0

Table 8.1: Truth table of 1.5bit encoder

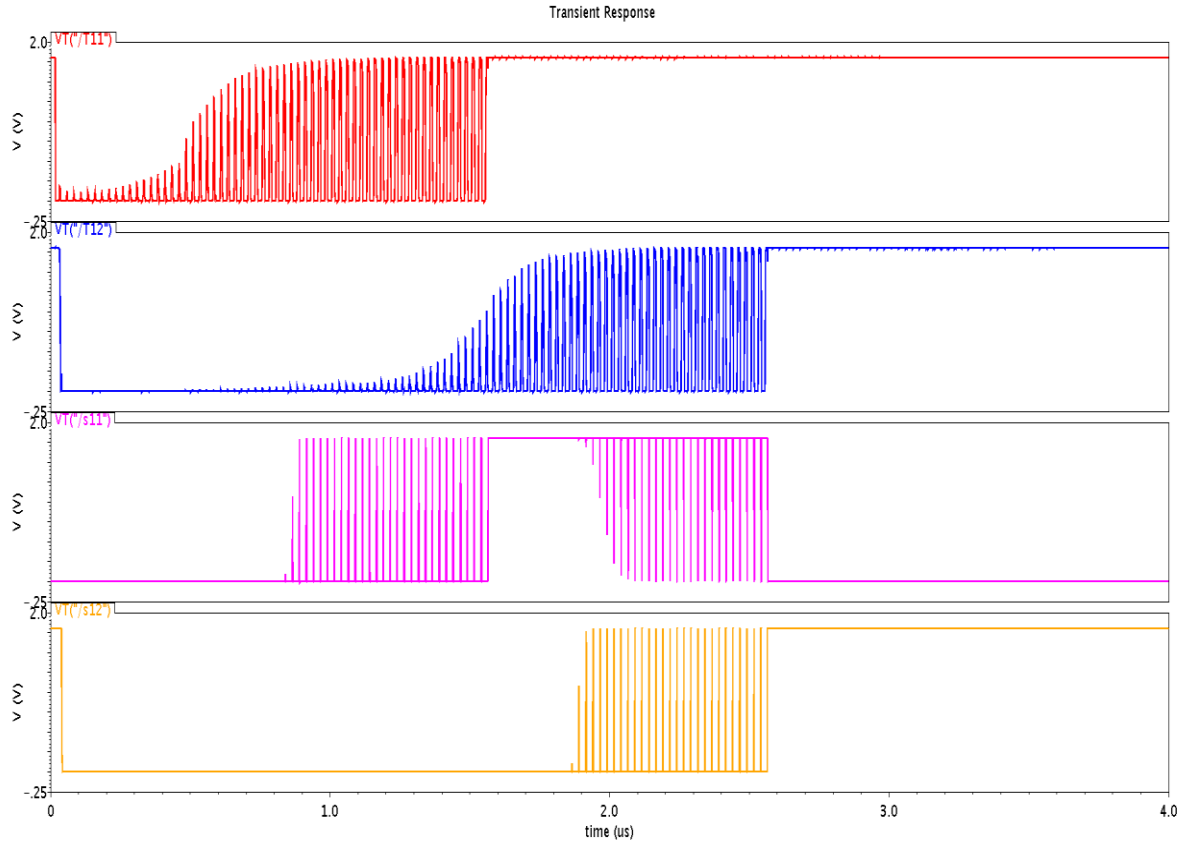


Figure 8.4: Transient simulation of the 1.5bit encoder

8.5 1.5bit DAC (3:1 MUX):

In the below figure T11 and T12 are outputs of flash ADC and vdac1+ is the output of DAC. Table 8.2 explains its ouput.

T12	T11	Vdac1+	Vdac1-
0	0	Vref-	Vref+
0	1	Vcm	Vcm
1	1	Vref+	Vref+

Table 8.2: Truth table of 1.5bit dac

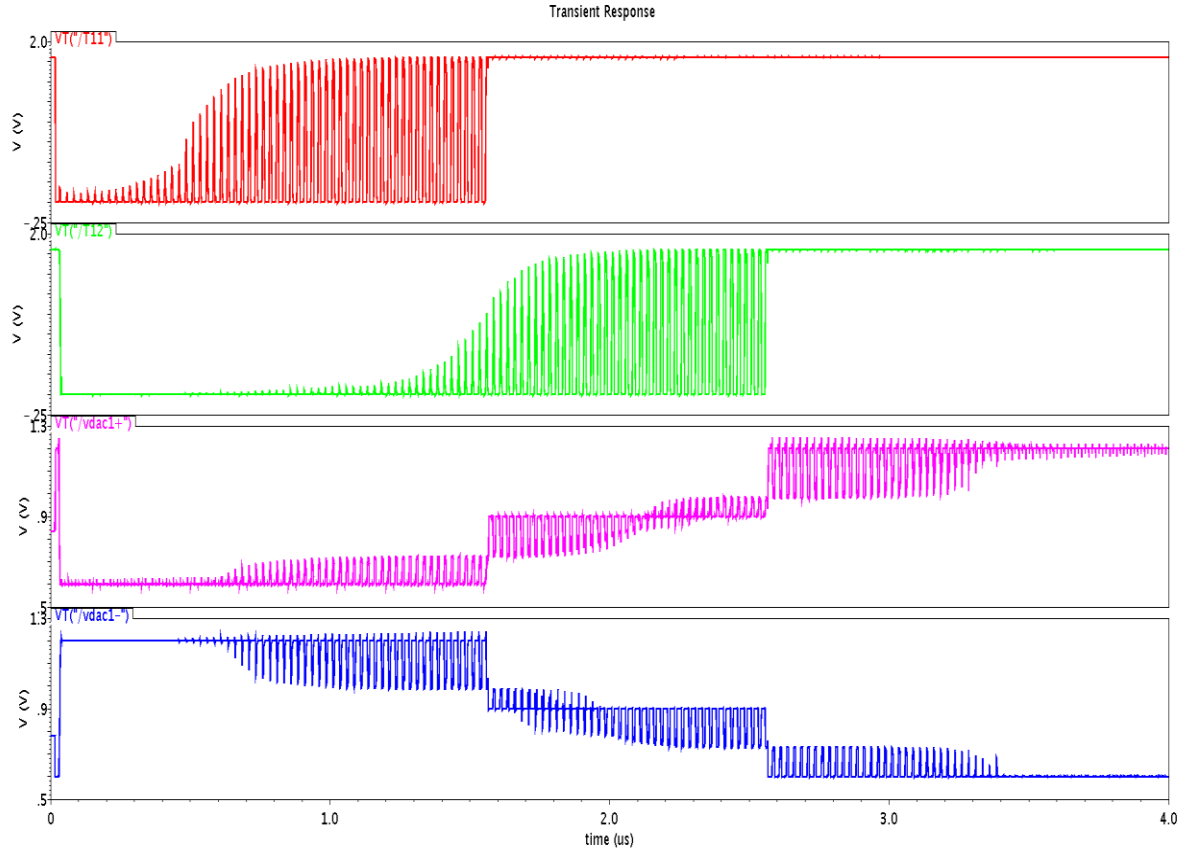


Figure 8.5: Transient simulation of the 1.5bit DAC

8.6 1.5bit MDAC:

$$V_o\mp = \begin{cases} (2V_{in} \pm -V_{CM}) + V_{ref} & V_{in} \leq V_{CM} - \frac{V_{ref}}{4} \\ (2V_{in} \pm -V_{CM}) & V_{CM} - \frac{V_{ref}}{4} \leq V_{in} \leq V_{CM} + \frac{V_{ref}}{4} \\ (2V_{in} \pm -V_{CM}) - V_{ref} & V_{in} \geq V_{CM} + \frac{V_{ref}}{4} \end{cases}$$

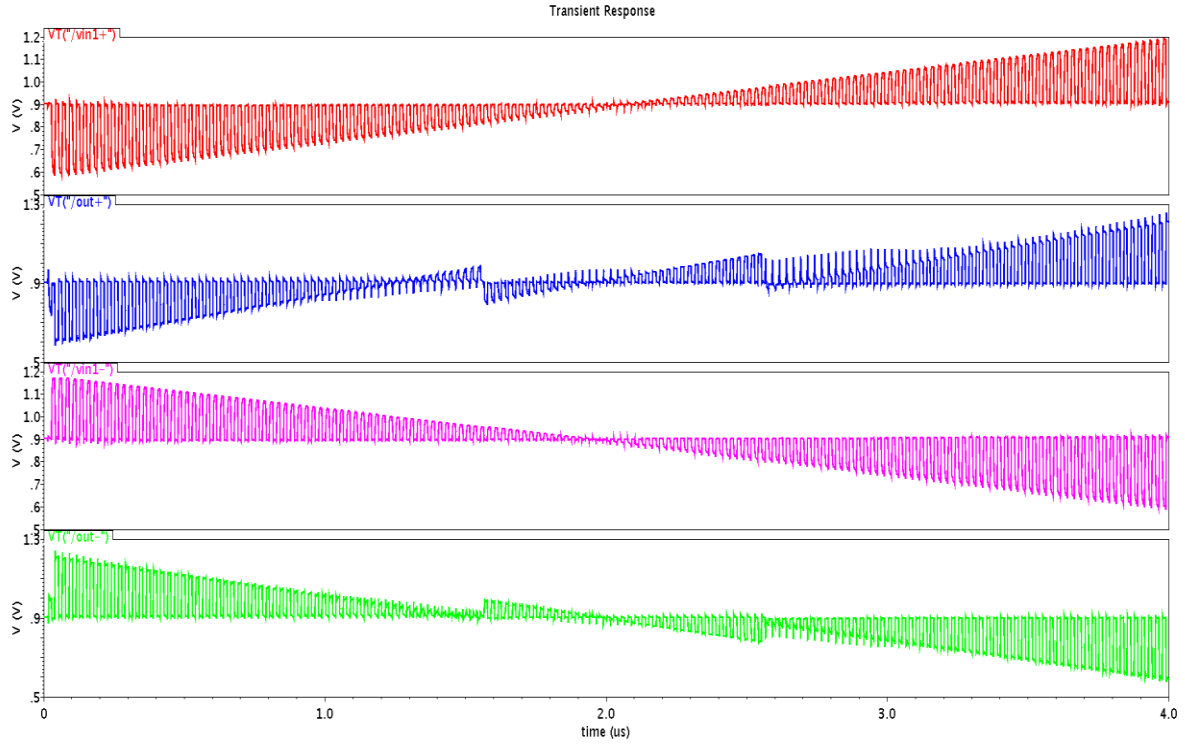


Figure 8.6: Transient simulation of the 1.5bit DAC

8.7 Gain boosted telescopic OTA:

a) Current of OTA = 300uA (for 40 MHz ADC), power of OTA=0.54mw

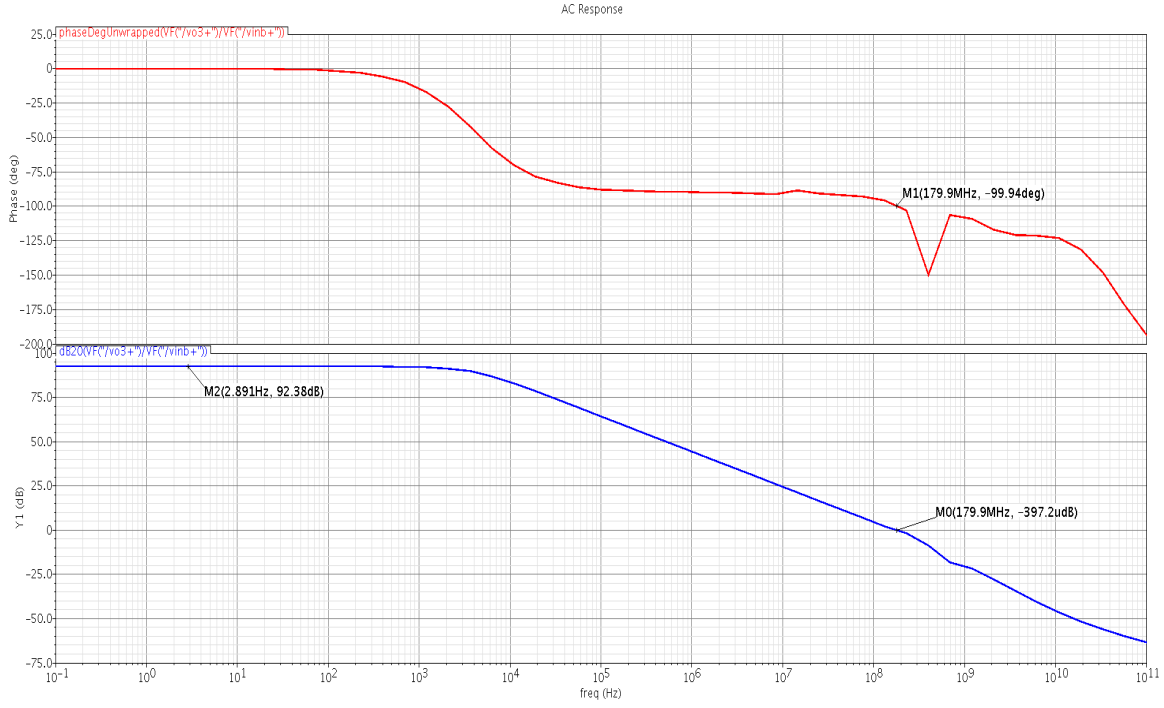


Figure 7.7: Transient simulation of the OTA for 40MHZ ADC

b) Current of OTA = 400uA (for 50 MHz ADC), power of OTA=0.72mw

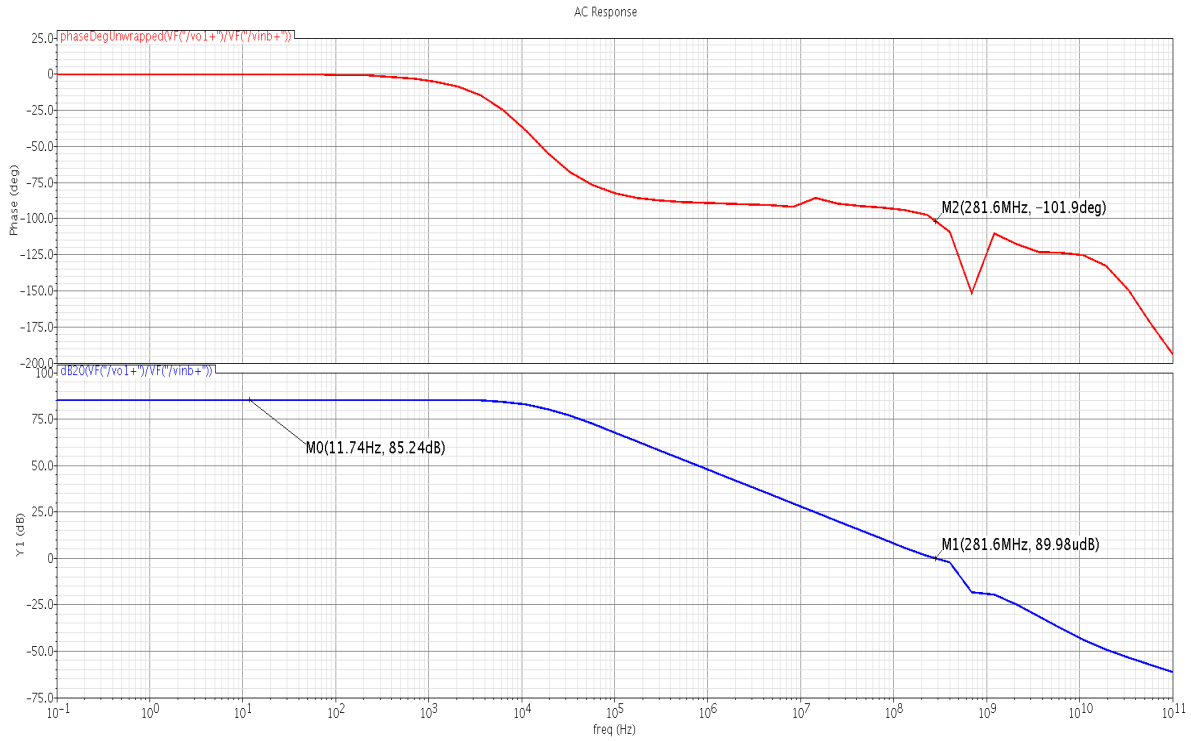


Figure 7.8: Transient simulation of the OTA for 50MHZ ADC

c) Current of OTA = 550uA (for 60 MHz ADC), power of OTA=0.99mw

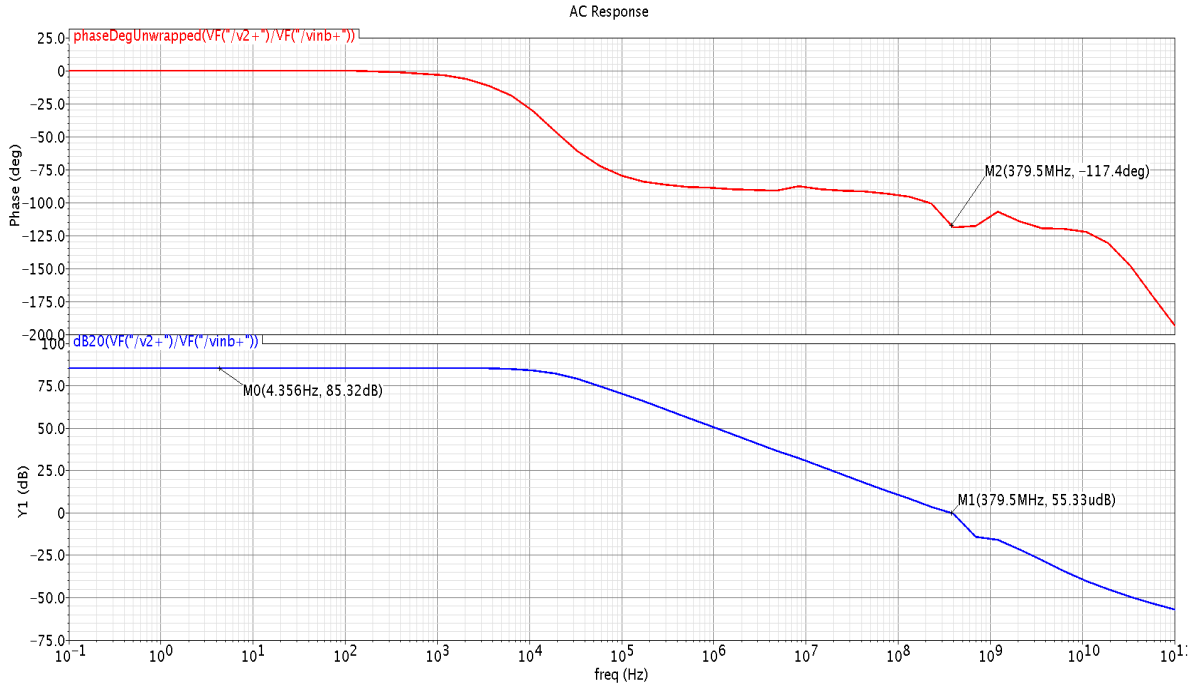


Figure 7.9: Transient simulation of the OTA for 60MHZ ADC

d) Tabular Results of OTA:

Parameters	OTA (40Msps)	OTA (50Msps)	OTA (60Msps)
Gain (dB)	92.38	85.24	85.32
UGB(HZ)	179.9M	281.6M	379.5M
Phase Margin (^{o})	80	78.1	62.6
Total current of OTA(A)	300u	400u	550u

8.8 10bit opamp shared pipeline ADC dynamic behaviour:

a) Input frequency=3.94MHZ, Sampling frequency=40MHZ

SNDR = 58.8 dB, ENOB= {(SNDR-1.76)/6.02}=9.47, SFDR=66.37db

Total power consumption of ADC = 5.51mw.

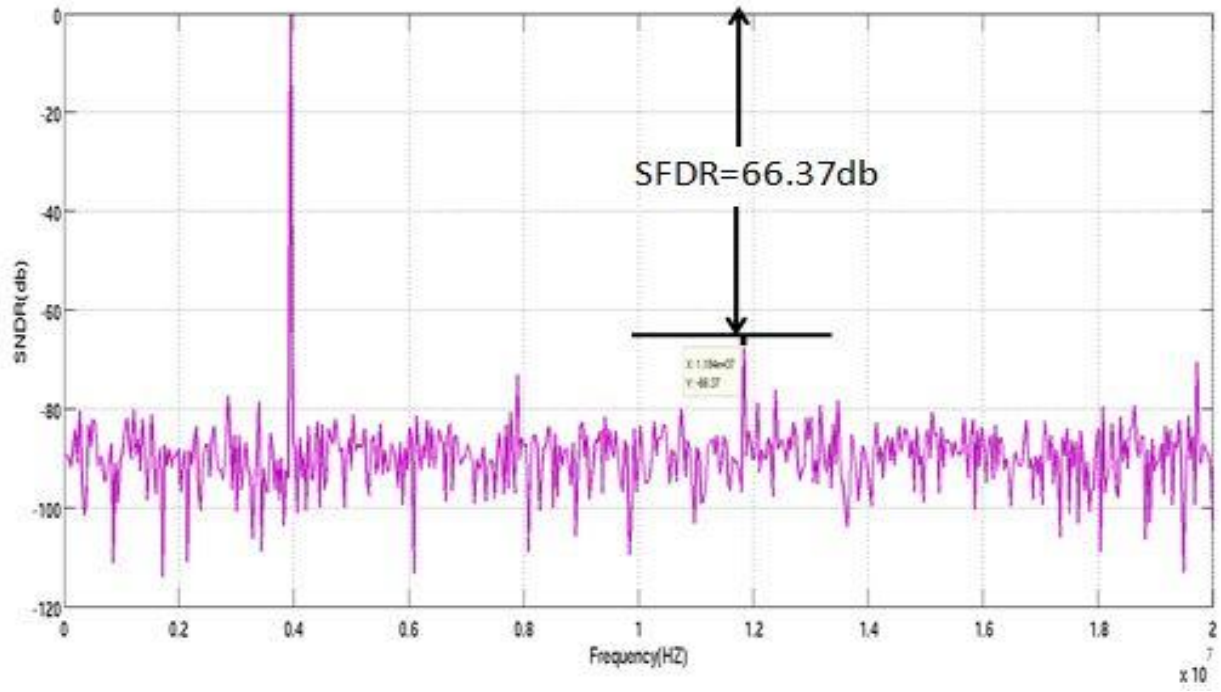


Figure 7.9: Dynamic behaviour of ADC at 40MHZ

b) Input frequency=19.88MHZ, Sampling frequency=40MHZ

SNDR = 55.1 dB, ENOB= {(SNDR-1.76)/6.02}=8.86, SFDR=65.7db

Total power consumption of ADC = 5.59mw

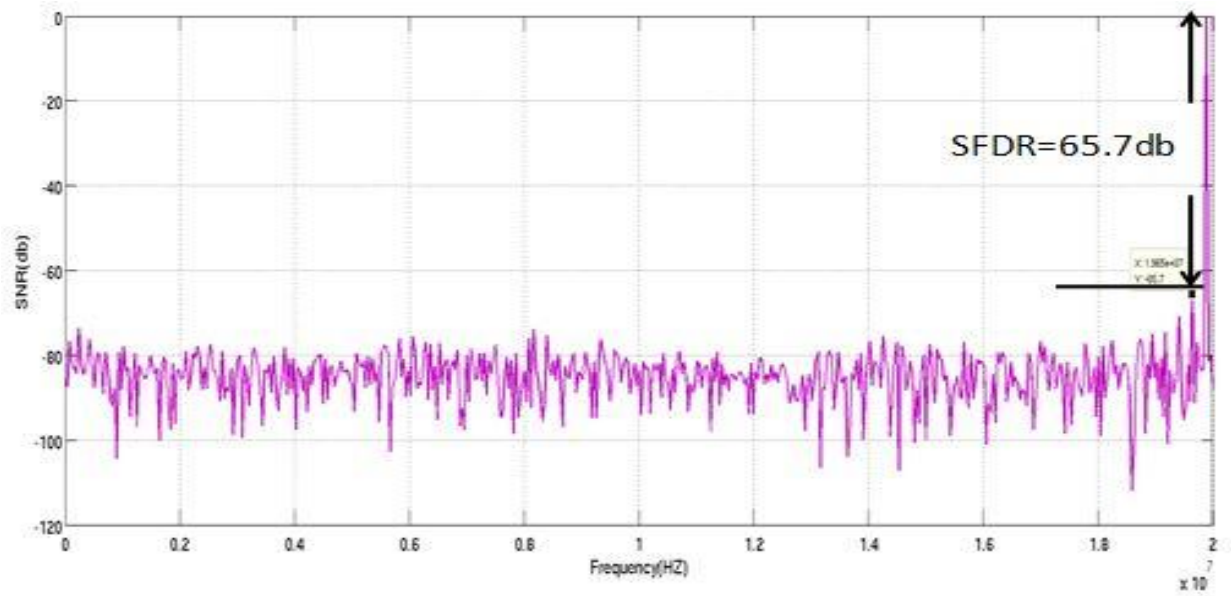


Figure 7.10: Dynamic behaviour of ADC at 40MHZ

c) Input frequency=4.93MHZ, Sampling frequency=50MHZ

SNDR = 56 dB, ENOB= {(SNDR-1.76)/6.02}=9.01, SFDR=59.46db

Total power consumption of ADC = 7.13mw

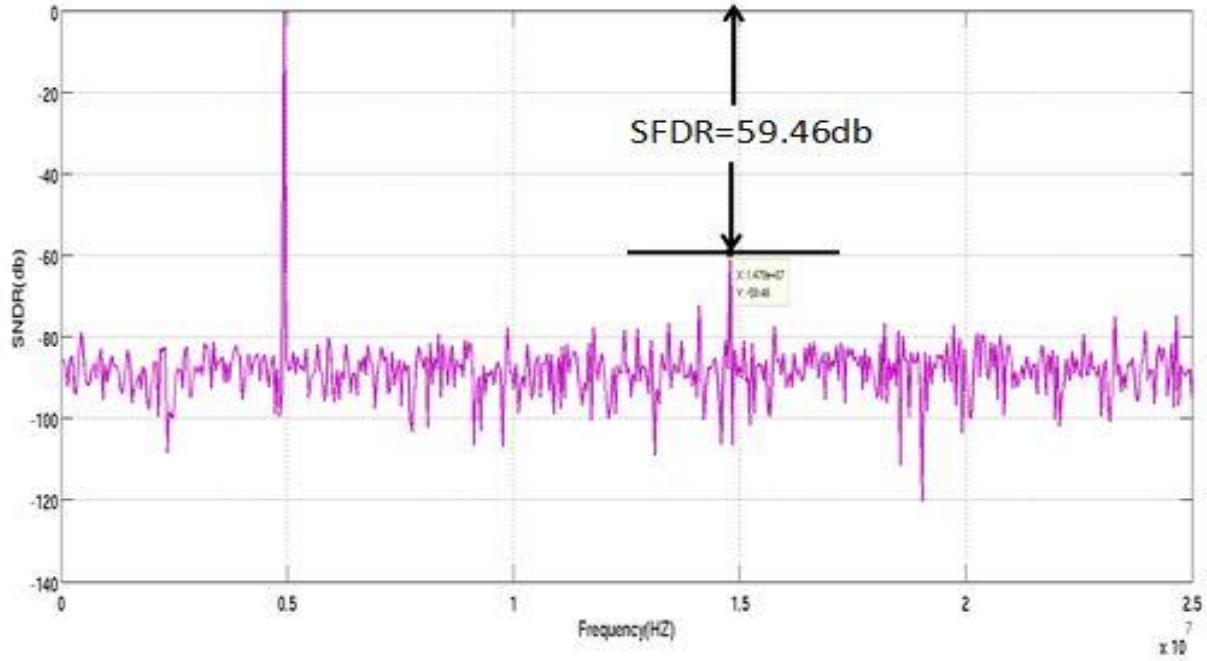


Figure 7.11: Dynamic behaviour of ADC at 50MHZ

d) Input frequency=24.85MHZ, Sampling frequency=50MHZ

SNDR = 53 dB, ENOB= {(SNDR-1.76)/6.02}=8.51, SFDR=57.64db

Total power consumption of ADC = 7.2mw

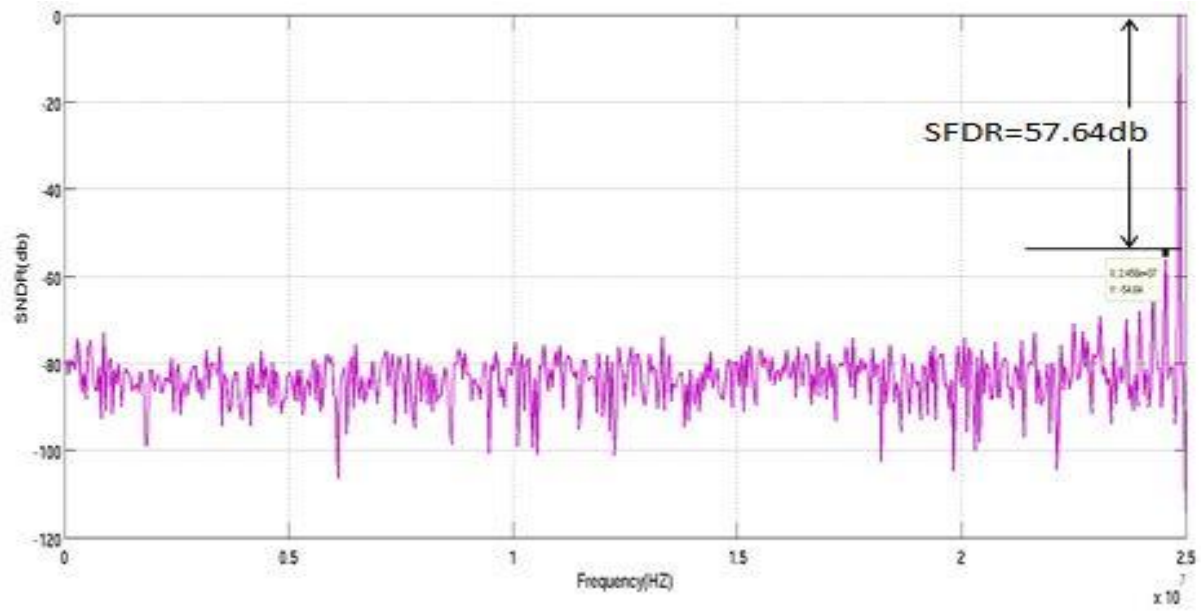


Figure 7.12: Dynamic behaviour of ADC at 50MHZ

e) Input frequency=5.92MHZ, Sampling frequency=60MHZ

SNDR = 52.5 dB, ENOB= {(SNDR-1.76)/6.02}=8.43, SFDR=56.6db

Total power consumption of ADC = 8.14mw

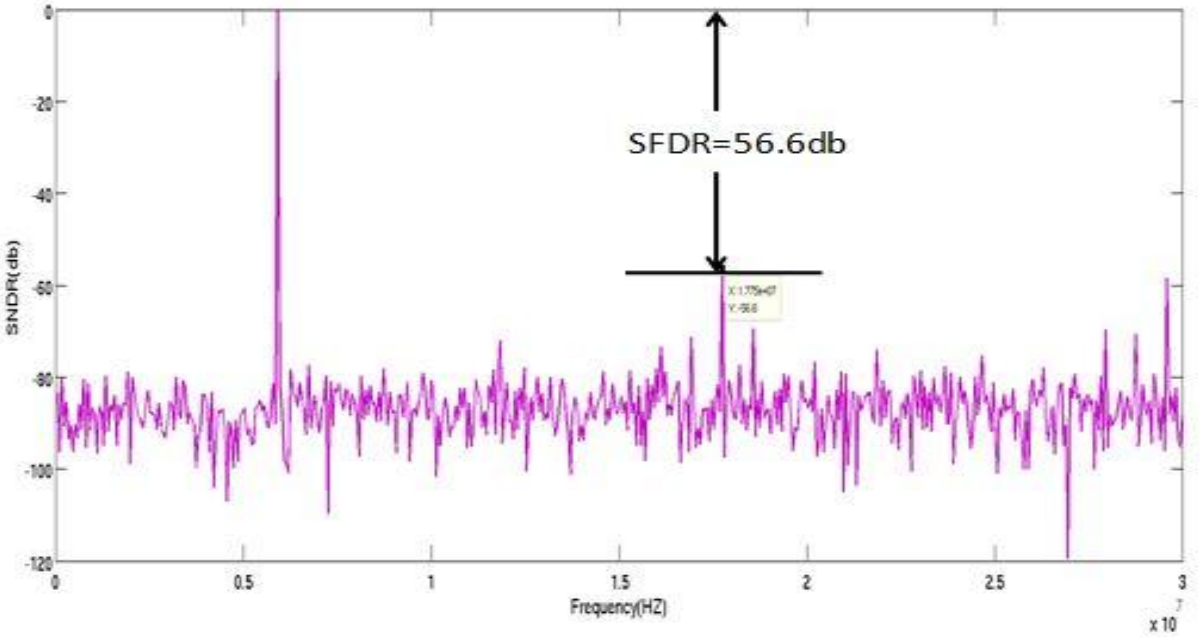


Figure 7.13: Dynamic behaviour of ADC at 60MHZ

6. Input frequency=29.82MHZ, Sampling frequency=60MHZ

SNDR = 51.25 dB, ENOB= {(SNDR-1.76)/6.02}=8.22, SFDR=56.6db

Total power consumption of ADC = 8.62mw

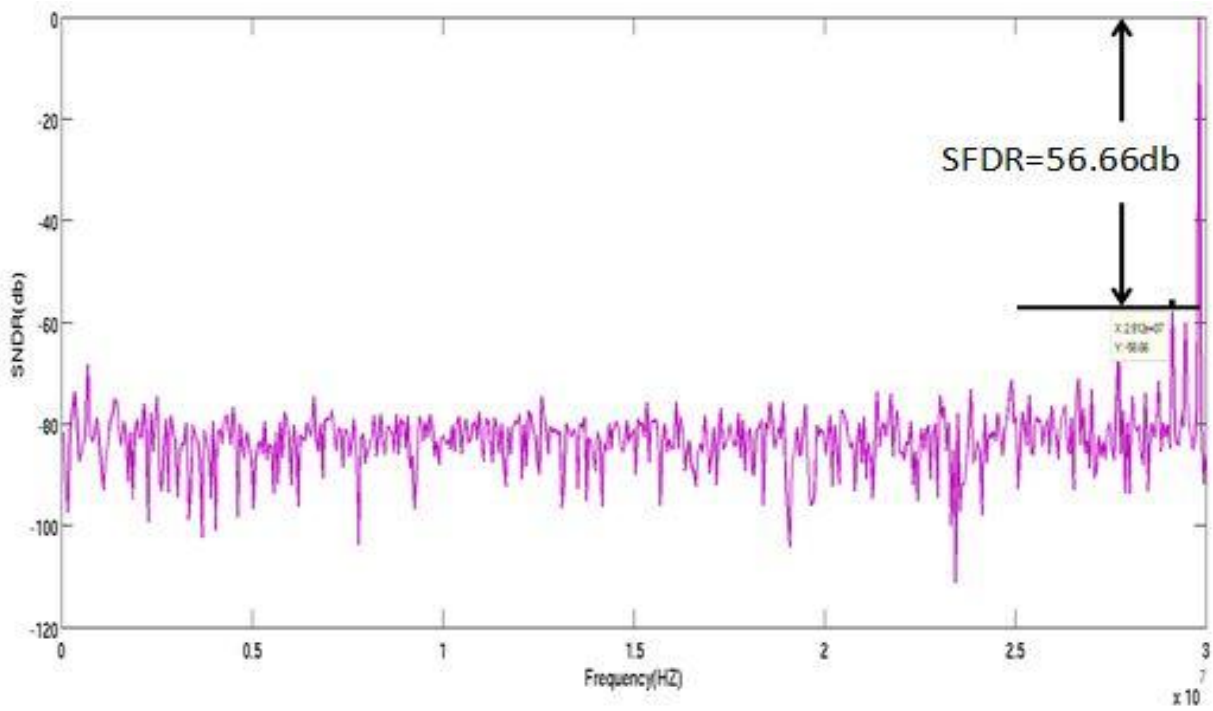


Figure 7.14: Dynamic behaviour of ADC at 60MHZ

Comparison table:

References	CMOS process	Fin	Fs	SNDR	ENOB	Total power	SFDR	FOM
Ref.[2]	0.18um	39.5MHZ	60MHZ	59.7db	9.63	28mw	76db	589fJ/conv-step
Ref.[3]	0.18um	10MHZ	100MHZ	54db	8.67	29mw	65db	711fJ/conv-step
Ref.[4]	0.18um	24.5MHZ	50MHZ	56.2db	9.03	12mw	72.7db	459fJ/conv-step
This work	0.18um	19.88MHZ	40MHZ	55.1db	8.86	5.59mw	65.7db	300fJ/conv-step
This work	0.18um	24.85MHZ	50MHZ	53db	8.51	7.2mw	57.64db	395fJ/conv-step
This work	0.18um	29.82MHZ	60MHZ	51.25db	8.22	8.62mw	56.6db	482fJ/conv-step

References

[1] An Approach to Improve the Figure-of-Merit (FoM) of a Pipeline Analog-to-Digital-Converter by Sounak Roy

[2] Yin Rui, Liao Youchun, Zhang Wei, and Tang Zhangwen “A 10-bit 80-MS/s opamp-sharing pipelined ADC with a switch-embedded dual-input MDAC”in Journal of semiconductors of, vol. 32(2), Feb. 2011.

[3] Moo-Young Kim , Jinwoo Kim, Tagjong Lee and Chulwoo Kim “10-bit 100-MS/s Pipelined ADC Using Input-Swapped Opamp Sharing and Self-Calibrated V/I Converter” in IEEE transactions on very large scale integration (vlsi) systems, vol. 19, no. 8, August 2011.

[4] Byung-Geun Lee and Robin M. Tsang “A 10-bit 50 MS/s Pipelined ADC With Capacitor-Sharing and Variable-gm opamp ” in IEEE journal of solid-state circuits, vol. 44, no. 3, March 2009

[5] Byung-Geun Lee and Robin M. Tsang “A 10-bit 50 MS/s Pipelined ADC With Capacitor-Sharing and Variable-gm opamp” in IEEE journal of solid-state circuits, vol. 44, no. 3, March 2009

[6] Benjamin Hershberg, Un-Ku Moon “A 61.5dB SNDR Pipelined ADC Using Simple Highly-Scalable Ring Amplifiers” in 2012 Symposium on VLSI Circuits Digest of Technical Papers

[7] Imran Ahmed “A Low-Power Capacitive Charge Pump Based Pipelined ADC” in IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 45, NO. 5, MAY 2010

[8] Ji-Eun Jang “Comparator-Based Switched-Capacitor Pipelined ADC with Background Offset Calibration”

[9] Robert H. Walden, “Analog-to-Digital Converter Survey and Analysis," Solid-State Circuits, IEEE Journal of, vol. 17, pp. 539-550, Apr. 1999.

[10] A. Kitagawa, M. Kokubo, T. Tsukada, T. Matsuura, M. Hotta, K. Maio, E.Yamamoto and E. Imiazumi, “A 10b 3MSample/s CMOS cyclic ADC," in 42nd IEEE International Solid-State Circuits Conference, ISSCC, Feb. 1995, pp.280-282.

[11] S.H. Lewis, P.R. Gray, \A Pipelined 5-Msample/s 9-bit Analog-to-Digital Converter," Solid-State Circuits, IEEE Journal of, vol. sc-22, pp. 954-961, Dec. 1987.

[12] M. Gustavsson, J.J. Wikner and N.N. Tan, CMOS DATA CONVERTERS FOR COMMUNICATIONS, Kluwer Academic Publishers, 2002.

[13] Mikko Waltari, CIRCUIT TECHNIQUES FOR LOW-VOLTAGE AND HIGHSPEED A/D CONVERTERS, Dissertation for the degree of Doctor of Science in Technology, Helsinki University of Technology, 2002.

[14] Mikko Waltari, CIRCUIT TECHNIQUES FOR LOW-VOLTAGE AND HIGHSPEED A/D CONVERTERS, Dissertation for the degree of Doctor of Science in Technology, Helsinki University of Technology, 2002.

[15] D. Haigh and B. Singh, "A switching scheme for switched capacitor filters which reduces the effect of parasitic capacitances with switch control terminals," in IEEE International Symposium on Circuits and Systems, ISCAS, May 1983, pp.586-589.

[17] Nagaraj K, Fetterman H S, Anidjar J, et al. A 250-mW, 8-b, 52-Msamples/s parallel-pipelined A/D converter with reduced number of amplifiers. IEEE J Solid-State Circuits, 1997, 32(3): 312

[18] Chandrashekar K, Bakkaloglu B. A 10 b 50 MS/s opamp-sharing pipeline A/D with current-reuse OTAs. IEEE CICC, 2009: 263

[19] J. K. Fiorenza, T. Sepke, P. Holloway, C. G. Sodini, and H.-S. Lee,"Comparator-based switched-capacitor circuits for scaled CMOS technologies," IEEE Journal of Solid-State Circuits, vol. 41, no. 12, pp. 2658–2668.

[20] I. Ahmed, "Pipeline ADCe nhancement Techniques," Ph.D. dissertation, Dept. lec.Engr. and Com. Sci., Univ. Toronto, Toronto, Canada, 2008.