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CORDIC based Universal Modulator

Lt Parichay Kalra
Department of ECE
NIT, Trichy, India
parichaykalra@yahoo.com

Naresh Vemishetty
Department of ECE
IIT Hyderabad, India
nareshvemishetty@gmail.com

Prof. B Venkatramani
Department of ECE
NIT, Trichy, India
bvenki@nitt.edu

***Abstract*— In the literature, different architectures have been proposed for FPGA implementation of Universal Modulator. The Look up table (LUT) technique is one way of realizing universal modulator. In this paper, a pipelined CORDIC using 2 stages of Multiplexer is proposed for efficient realization of universal modulator. For the purpose of comparison, this universal modulator is implemented on Spartan 3E FPGA and its performance is compared with that of unrolled CORDIC which uses only shifters and adders and unpipelined Multiplexer based CORDIC. The Universal Modulator is used for realizing Amplitude, Frequency and Phase Modulation. From the implementation, it is found that the pipelined multiplexer based Modulator is 5% more area efficient and 4 % more speed efficient than unrolled CORDIC**

***Index Terms*—FPGA, Universal Modulator, CORDIC**

I. INTRODUCTION

The Coordinate Rotation Digital Computer (CORDIC) algorithm is an iterative algorithm based on trigonometrical/geometrical formulae which was proposed by Jack E. Volder [1] in 1959 and later improved by Walther and others [2]. It has already been shown that CORDIC architectures are attractive alternate to conventional multiply, division, shift and add operations [1]. The CORDIC architectures are widely used in different Communication subsystems like Digital Frequency Synthesizers, Synchronizers, Amplitude Modulation, Frequency Modulation, Phase Modulation, Amplitude Shift Keying, Frequency Shift Keying, Phase Shift Keying [3], up/down converters, mixers etc. The same approach of using CORDIC as modulator has been used for Quadrature Amplitude Modulation (QAM)[4] and multicarrier QAM [5] [6] which uses LUT for the realization. The advantage of using CORDIC as modulator over Look up table ROM is that CORDIC directly generates sine and cosine wave rather than using phase to amplitude converter. The CORDIC approach for modulator is more preferred due to its better phase resolution, high precision, cheaper hardware cost, flexibility and performance.

A number of CORDIC architectures have been reported in the literature for realizing universal modulator. Unrolled CORDIC architecture proposed by Jack E. Volder [1] is a hardware extensive architecture used for obtaining sine and cosine of angles. In [7], a Mux based CORDIC architecture has been proposed to obtain the sine and cosine of angles which is less complex in terms of hardware utilization but suffers with same delay as that of [1]. In [8] the pipelined approach for Mux based CORDIC was proposed to obtain the sine and cosine of angles with an improvement in area and delay characteristics. The objective of this paper is to extend the scheme proposed in [3] for the implementation of CORDIC based universal modulator on Spartan 3E FPGA. Its performance is studied by realizing amplitude, frequency and phase modulation schemes.

The paper has been organized in the following sections: Section II gives an overview of the CORDIC Algorithm. Section III describes working of CORDIC as Universal Modulator. Section IV gives the details of CORDIC architectures used in implementation of universal modulator. Section V presents the hardware implementation details of universal modulator. Section VI tabulates the results Section VII presents the conclusion.

II. CORDIC ALGORITHM

A. Introduction

The CORDIC algorithm provides an iterative method of performing vector rotations by arbitrary angles using shifts and adds [1]. In the rotation mode, CORDIC is used for converting one vector in rectangular form to another vector in rectangular form. In the vector mode, it converts a vector in rectangular form to polar form.

B. Rotation Mode of CORDIC

The CORDIC algorithm for this mode is derived from the general rotation transform

$$a_{fn} = a_{in}\cos\phi - b_{in}\sin\phi \quad (1)$$

$$b_{fn} = b_{in}\cos\phi + a_{in}\sin\phi \quad (2)$$

Which rotates a vector in a Cartesian plane by an angle ϕ to another vector with the coordinates . The rotation may be

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achieved by performing a series of successively smaller elementary rotations $\phi_1, \phi_2 \ldots\ldots \phi_n$ such that $\phi = \sum \phi_i$ Fig 1. shows the case where a rotation of a vector of magnitude 1 by an angle ϕ is achieved using three elementary rotations ϕ_1, ϕ_2, ϕ_3

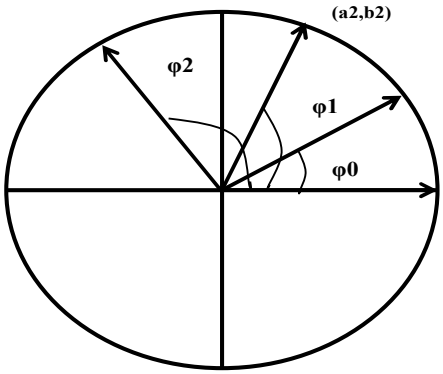

Fig 1: CORDIC Rotations

Rotation of the vector by an angle θ_i can be rewritten as

$$a_{i+1} = a_i \cos\phi - b_i \sin\phi \quad (3)$$

$$b_{i+1} = b_i \cos\phi + a_i \sin\phi \quad (4)$$

$$\frac{a_{i+1}}{\cos\phi} = a_i - b_i \tan\phi \quad (5)$$

$$\frac{b_{i+1}}{\cos\phi} = b_i + a_i \tan\phi \quad (6)$$

The computational complexity of above equations can be reduced rewriting these equations as

$$a_{i+1} = a_i - b_i \tan\phi \quad (7)$$

$$b_{i+1} = b_i + a_i \tan\phi \quad (8)$$

$$(a_{fn}, b_{fn}) = \left(\frac{a_N}{\prod \cos\phi}, \frac{b_N}{\prod \cos\phi}\right) \quad (9)$$

By performing the division by $\cos\phi_i$ together for all the N iterations by dividing the value of (a_N, b_N) by $\prod \cos\phi i$. Further, the value of ϕ_i for i =1, 2,.. N is chosen such that tan ϕ_i is $2^{-i.}$

This reduces the multiplication by the tan ϕ_i to simple shift operation. As the iteration increases ϕ_i becomes smaller and smaller. We may terminate the iteration when the difference between $\tan^{-1}(2^{-i})$, becomes very small for some value of N. The remaining angle by which the vector needs to be rotated after the completion of i iterations is indicated by the parameter z_{i+1} defined by equation

$$z_{i+1} = z_i - \phi_i \quad (10)$$

ϕ_i is considered to be positive when the rotation required is anticlockwise and is negative Otherwise to approximate an arbitrary angle using ϕ_i of the form $\tan^{-1}(2^{-i})$, ϕ_i may have to be chosen to be negative for some values of i. A sign (sgn) of z_i indicates whether in the next iteration, the rotation has to be anticlockwise or clockwise. Since, $\tan\phi$ is $(+2^{-i})$ when ϕ_i is positive and (-2^{-i}) otherwise, the iterative equations may be rewritten as

$$\delta_i = \text{sgn}(z_i) \quad (11)$$

$$a_{i+1} = a_i - \delta_i 2^{-i} b_i \quad (12)$$

$$b_{i+1} = b_i + \delta_i 2^{-i} a_i \quad (13)$$

$$z_{i+1} = x_i - \delta_i \tan^{-1} 2^{-i} \quad (14)$$

III. CORDIC AS UNIVERSAL MODULATOR

The Universal Modulator (UM) consists of phase accumulator, an adder, CORDIC [3] and Digital to Analog Converter as shown in Fig 2. The phase accumulator is used to control the frequency component and the adder provides the phase control in the CORDIC. The CORDIC operating in Rotation Mode works as a universal modulator. The universal modulator is implemented on Spartan 3E FPGA in various modes of modulation for three different CORDIC architectures. The onboard digital to analog LT 2624 converter converts the onboard digital signals into analog form for which output is taken on cathode ray oscilloscope.

The various inputs to the system are x_{in}, y_{in}, which is used for realizing amplitude modulation, Δ_r for frequency modulation and φ(t) for phase modulation

For amplitude modulation (x_{in}, y_{in} φ) is chosen as (1,0,0) and the Δ_r is constant then the unmodulated carriers sinωt and cosωt is obtained as the output. When modulated carriers is required, the modulating signals are applied at x_{in} and y_{in}

For implementing frequency modulation wave at the output (y_{in}, φ) is chosen as (0,0) with x_{in} as constant and Δ_r is variable

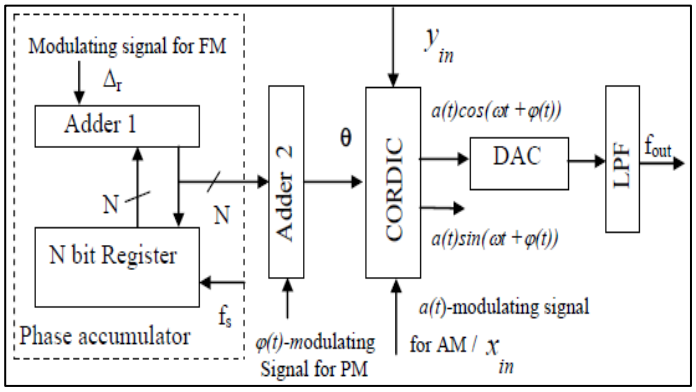

Fig. 2 Universal Modulator

For implementing phase modulation in the universal modulator y_{in} is chosen as (0, 0) with x_{in} as constant and Δ_r is constant φ is variable

IV. CORDIC ARCHITECTURES

There are different types of architectures available for CORDIC each having some tradeoff between speed and the area. However for implementation of UM three architectures have been considered namely:

- Unrolled CORDIC
- Mux Based Unpipelined CORDIC
- Mux based Pipelined CORDIC

Unrolled CORDIC: An 8 stage CORDIC is implemented for universal modulator. All coefficients are taken to be 16 bit wide. As shown in Fig.3, the architecture comprises of adders/ subtractors and shifters [1]. In the uppermost adder/ subtractors an angle is computed for each iteration. The middle and bottommost adder is used for the evaluation of cosine and sine. The initial value of a- vector and b-vector is chosen to be (1/R) and 0. For each stage of iterations the new values of vectors are found to converge towards desired angle. Besides this, there is crosswise addition or subtraction based on angle evaluated in the previous iteration of preceding stage. This crosswise addition or subtraction is represented by sign bit (δ). The value of sign bit depends upon the value of z vector evaluated in the preceding stage.

Mux Based Unpipelined CORDIC: A new 8 Stage CORDIC architecture has been proposed in [7] which have been found to be less complex in terms of hardware. The architecture starts with same set of initial vectors a and b with same initial value as (1/R) and 0. With these initial values, the output from first stage is given as:

$$a_1 = a = (1/R) \quad (15)$$

$$b_1 = a \quad (16)$$

The output from second stage can be given as:

- δ_1 is positive

$$\left.\begin{aligned} a_2 &= a_1 - \frac{a1}{2} = \frac{a}{2} \\ b_2 &= a_1 + \frac{a1}{2} = \frac{3a}{2} \end{aligned}\right\} \quad (17)$$

- δ_1 is negative

$$\left.\begin{aligned} a_2 &= a_1 + \frac{a1}{2} = \frac{3a}{2} \\ b_2 &= a_1 - \frac{a1}{2} = \frac{a}{2} \end{aligned}\right\} \quad (18)$$

Thus the Stage 2 can be replaced with the two multiplexers with the crosswise interchanged values which are shown above. The output of stage 3 can be gives as:

- δ_1 is +ve and δ_2 is +ve

$$\left.\begin{aligned} a_3 &= a_2 - \frac{b_2}{4} = \frac{a}{2} - \frac{3a}{8} = \frac{a}{8} \\ b_3 &= b_2 + \frac{a_2}{4} = \frac{3a}{2} + \frac{a}{8} = \frac{13a}{8} \end{aligned}\right\} \quad (19)$$

- δ_1 is -ve and δ_2 is +ve

$$\left.\begin{aligned} a_3 &= a_2 - \frac{b_2}{4} = \frac{3a}{2} - \frac{a}{8} = \frac{11a}{8} \\ b_3 &= b_2 + \frac{a_2}{4} = \frac{a}{2} + \frac{3a}{8} = \frac{7a}{8} \end{aligned}\right\} \quad (20)$$

- δ_1 is +ve and δ_2 is -ve

$$\left.\begin{aligned} a_3 &= a_2 + \frac{b_2}{4} = \frac{a}{2} + \frac{3a}{8} = \frac{7a}{8} \\ b_3 &= b_2 - \frac{a_2}{4} = \frac{3a}{2} - \frac{a}{8} = \frac{11a}{8} \end{aligned}\right\} \quad (21)$$

- δ_1 is -ve and δ_2 is -ve

$$\left.\begin{aligned} a_3 &= a_2 + \frac{b_2}{4} = \frac{3a}{2} + \frac{a}{8} = \frac{13a}{8} \\ b_3 &= b_2 - \frac{a_2}{4} = \frac{a}{2} - \frac{3a}{8} = \frac{a}{8} \end{aligned}\right\} \quad (22)$$

Mux Based Pipelined CORDIC: This architecture involves two level pipelining of Mux based CORDIC [8] used for universal modulator. For the purpose of implementation 16 bit wide coefficients are used for FPGA implementation. This architecture involves registers being inserted between the succeeding stages. Due to inclusion of pipeline registers the area of the architecture increases with the increase of operating frequency. The pipelined registers are inserted after the Stage 4 and Stage 7 as shown in figure 4.

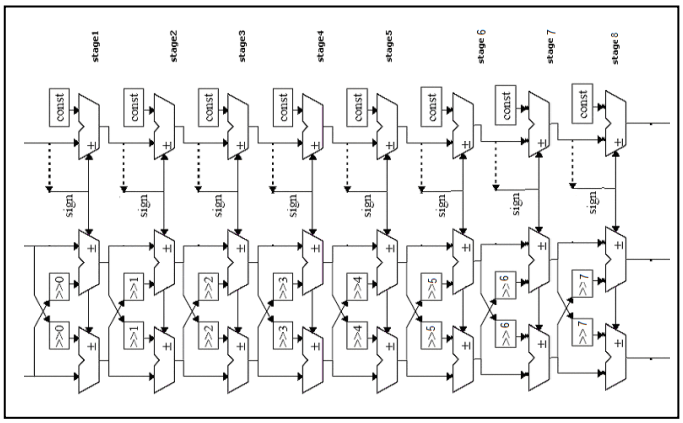

Fig 3: Unrolled CORDIC

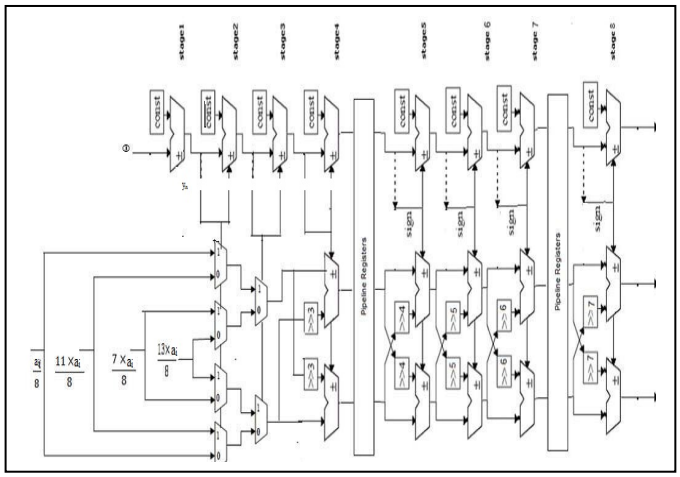

Fig 4: 2 level pipelined CORDIC

V. HARDWARE IMPLEMENTATION

The CORDIC architectures are shown in Fig. 3, Fig. 4. Unpipelined architecture of Fig. 4 has been realized for universal modulator. All coefficients have been chosen to be 16 bit wide. The universal modulator has been realized for amplitude, frequency and phase modulation in Verilog HDL on Xilinx ISE 14.1. The design is synthesized and a programming file (.bit) is generated using Xilinx ISE 14.1. The .bit file is burned to Xilinx Spartan 3E (XC3S500E-4FG320) [9] using iMPACT tool for programming FPGA. The Xilinx Spartan 3E (XC3S500E-4FG320) has an onboard oscillator with the max frequency of 50 MHz. The Xilinx Spartan 3E (XC3S500E-4FG320) has a digital to analog converter (LTC 2624) which is four channel serial digital to analog converter (DAC) for 12 bit unsigned resolution[10].The output of this DAC is taken to Agilent DSO3202A oscilloscope via J5 header. The entire setup and procedure is repeated for all modulation techniques and the waveforms obtained are as shown in Fig. 5-7.

VI. RESULTS

A 16 bit CORDIC has been implemented to obtain the outputs of amplitude modulation , frequency modulation and phase modulation on Xilinx Spartan 3E FPGA [9]. The procedure of programming FPGA is first implemented for amplitude modulation for three CORDIC architectures [1] [7] [8] . The results are obtained from the design summary window in Xilinx ISE 14.1. The implementation results of modulation techniques on Xilinx Spartan 3E (XC3S500E-4FG320) are tabulated below in Table I-III. The Amplitude Modulated, Frequency Modulated and phase modulated wave is shown in Fig 5-7.

TABLE I: Implementation Results for Amplitude Modulation

	Amplitude Modulation		
	Original Unrolled CORDIC	***Mux Based Without Pipeline***	***Mux Based Pipelined***
Slices	963	624	896
LUTs	502	337	476
Critical Path Delay (ns)	103	103	99

TABLE II: Implementation Results for Frequency Modulation

	Frequency Modulation		
	Original Unrolled CORDIC	***Mux Based Without Pipeline***	***Mux Based Pipelined***
Slices	975	632	915
LUTs	511	346	482
Critical Path Delay (ns)	103	103	99

TABLE III: Implementation Results for Phase Modulation

	Phase Modulation		
	Original Unrolled CORDIC	***Mux Based Without Pipeline***	***Mux Based Pipelined***
Slices	986	654	938
LUTs	521	357	493
Critical Path Delay (ns)	103	103	99

From the implementation results obtained for Universal Modulator in all modulation schemes, it is found that the number of slices and LUTs required for 2 level pipelined multiplexer based modulator is less than the unrolled CORDIC based modulator and more than the unpipelined multiplexer CORDIC based modulator. Also the former modulator is more delay efficient as it gives a lesser critical delay value.

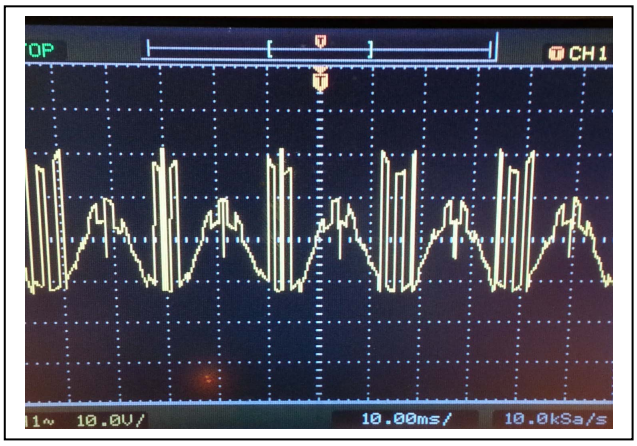

Fig 5: Amplitude Modulation

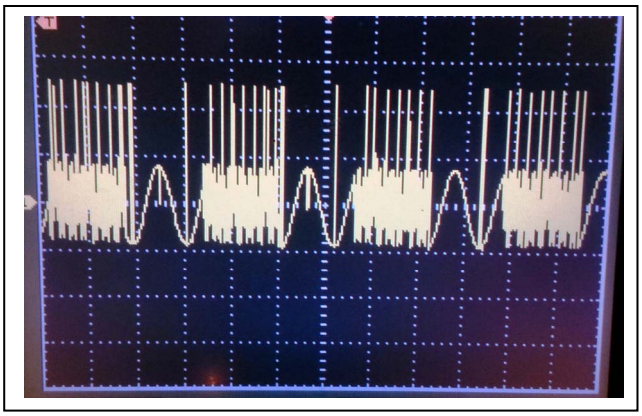

Fig 6: Frequency Modulation

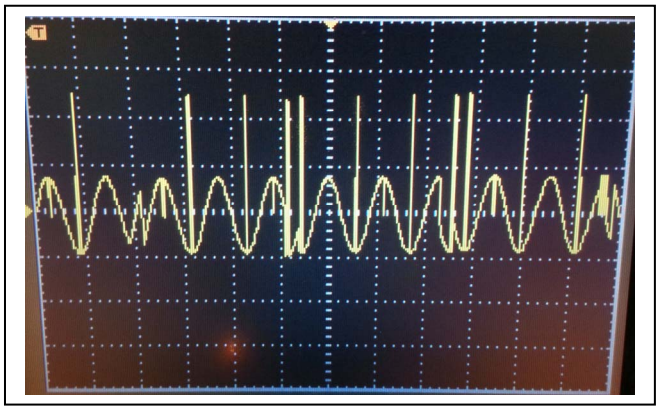

Fig 7: Phase Modulation

VII. CONCLUSION

The universal modulator has been implemented on the Spartan 3E FPGA using three different architectures of CORDIC. From the results it is found that Universal modulator based on multiplexer based two level pipelined architecture is 5\% area and 4\% speed efficient in comparison with the universal modulator based on unrolled CORDIC.

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