Die-To-Die and Within-Die Fabrication Variation of 65nm CMOS Technology PMOS Transistors

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***Abstract*—Study and understanding of transistor and circuit variations caused by the fabrication process has become an important factor for integrated circuits as the device dimensions become smaller. Effects on clock frequency and IC performance caused by die-to-die and within-die variations have made it important to incorporate process variations in circuit simulators to correctly model the working of the present IC technology. This paper demonstrates the microscopic parameter variation modeling of die-to-die and within-die variations for 65nm CMOS fabrication technology by using the HiSIM surface-potential-based compact model. It is found that for accurate variation modeling of V_{th} and I_{on} from die-to-die and within-die primary consideration of only four parameters, namely substrate doping (NSUBC), pocket-implantation doping (NSUBP), carrier mobility degradation due to gate-interface roughness (MUESR1) and channel length change (XLD) is sufficient. In addition to these, modeling of within-die variation requires inclusion of a small variation for a fifth parameter describing the depletion charge contribution for the effective-electric field (NDEP). Variation analysis is done for wide p-MOSFETs (W=10µm) as a function of gate length.**

***Index Terms*—compact model, die-to-die, within-die, MOSFET, fabrication variation, microscopic parameters.**

I. Introduction

Fabrication process variation has become an important factor which must be considered for smaller device dimensions. Extraction of these variations and their incorporation in the circuit simulation is essential. The obtained information can also help as feedback to improve the fabrication process. Co-relating the macroscopic variations like threshold voltage (V_{th}) and ON current (I_{on}) with the microscopic process variation is a challenging task, which has become possible by using the HiSIM2 surface-potential-based compact model [1]. V_{th} is obtained from the constant current method [2]. I_{on} of p-MOSFETs is defined as I_{ds} for V_d=V_g= 0V and V_s=V_b =1.2V. The analysis reported here bridges the gap between circuit simulation and TCAD by enabling the extraction of the microscopic MOSFET parameter variation.

In this paper we analyze 65nm technology based p-MOSFET for fabrication variation within a single die as well as between different die's. The novelty of this paper includes: a) Analysis of within-die microscopic parameter variation using the HiSIM2 model and validating that the modeling process [3] can also be effectively used for within-die variation parameter extraction with incorporating a slight improvement in model. b) Die-to-die as well as within-die variation analysis for down to 60nm drawn gate length. c) This paper also validates that the microscopic parameters identified in the extraction methodology described in [3], can be effectively used to model the variation observed for all MOSFET gate-length. Mathematical formulation of HiSIM2 is not described in this paper as it is very complex and has been published in many papers.

Previously, die-to-die variation analysis using the HiSIM2 model has been reported for n-MOSFETs fabricated in 65nm CMOS technology but the smallest gate length which could be used was 100nm [3].Research to capture the process variation has been done by many groups around the world by applying different methods utilizing ring oscillators [4], reconfigurable ring oscillators [5], flush delay techniques [6] or scan-chain based systems [7]. However, all of these techniques measure the total macroscopic variation observable in the test-circuit properties due to different microscopic effects and neglect a detailed analysis of the microscopic sources of all these variations. This paper provides an in-depth study of all the microscopic parameters responsible for the observed macroscopic process variation.

II. Model parameter extraction

Measurements of the p-MOSFET characteristics are taken on an Agilent Technologies B1500 A semiconductor device analyzer. Altogether 12 p-MOSFET structure are measured, all having different L(gate length), W(gate width) combinations and all the 12 structures are arranged in identical pairs called left and right MOSFET structure. So characteristic measurements of 12·2 p-MOSFETs on a single die are taken for a total of 36 such dies. This means, that 12·2·36=864 p-MOSFETs are used for the experimental part of our study on fabrication variation. The 12 MOSFET-structure combinations are covering the L and W dependence of the variation. For wide W of 10µm the L sizes of 60nm, 85nm, 100nm, 120nm, 150nm, 300nm and 2µm are used to study the L-dependence of the variation. Furthermore, for long L of 2µm the W sizes of 120nm, 180nm, 300nm and 1µm are used to study the W-dependence of the variation. The smallest drawn MOSFET geometry in the studied CMOS technology is L=60nm and W=120nm. Among the 36 dies a nominal die is selected, which has a center position in the measured distribution for the threshold voltage and ON current variation. The characteristic measurements obtained for the nominal die are used to extract the nominal (or typical) parameter set of HiSIM2 model for the studied CMOS technology. For this purpose the IC-CAP parameter-extraction software from Agilent technology and the

open source SPICE3F5 circuit simulator from University of California at Berkeley, both with built-in HiSIM2 model, are used. HiSIM2 is an industry-standard surface-potential-based compact model [8], which accurately models the complete characteristics of a bulk MOSFET with single set of parameters for all gate lengths and width, simultaneously. Some figures are shown below in Fig.1, which compare simulated results with the extracted model card (HiSIM2 parameters) for the nominal die to the measured data. The extracted HiSIM2 model card is used as the basis for our modeling of the die-to-die and within-die fabrication-process variation measured for the studied 65nm CMOS technology.

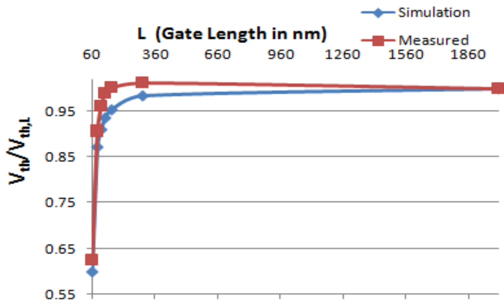


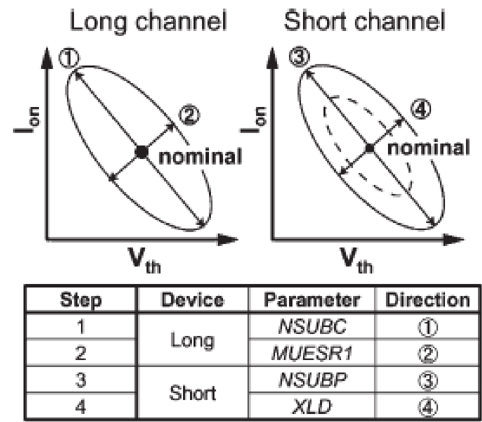
Fig.1. Among many results obtained from IC-CAP with the extracted HiSIM2 model card the above figure shows the dependence of V_{th} on gate length and is normalized with V_{th} of L=2µm.

III. DIE-TO-DIE VARIATION

Die-to-die variation of microscopic p-MOSFET parameters is analyzed with a statistics of 36 different dies, each die having 7 different L, W combinations. For studying the L-dependence of the variation, IC-CAP's HiSIM2 based parameters are set to the extracted nominal-die values and then these physical microscopic parameters are varied to obtain an accurate modeling of the V_{th}-I_{on} pattern. The microscopic parameters which perfectly model the variation pattern are shown in the Fig.2. The method used for modeling the variation pattern is taken from [3].The L-dependence of the die-to-die variation is analyzed for constant W=10µm and for L=60nm, 85nm, 100nm, 120nm, 150nm, 300nm, 2µm.

Device	Parameter	Meaning
Long	NSUBC	Substrate Doping
Long	MUESR1	Mobility degradation(oxide roughness)
Short	NSUBP	Peak Pocket-doping concentration
Short	XLD	Channel-Length Change

Fig.2. Microscopic model parameters found sufficient to model the V_{th}-I_{on} variation. Long refer to L=2µm and Short refers to L=60nm, identifying the p-MOSFET sizes which are mainly used for the variation extraction. These parameter are selected based on a sensitivity analysis for V_{th} and I_{on} and their physical effect on the fabrication process.



Step	Device	Parameter	Direction
1	Long	*NSUBC*	①
2		*MUESR1*	②
3	Short	*NSUBP*	③
4		*XLD*	④

Fig.3. Method used for extraction of the microscopic parameter variation from V_{th}-I_{on} variation data. First the variation of NSUBC and MUESR1 is determined for the Long (L=2µm) transistor, keeping NSUBP and XLD constant. Then variation of the Short (L=60nm) transistor is modeled with NSUBP and XLD. The procedure is indicated in above table.

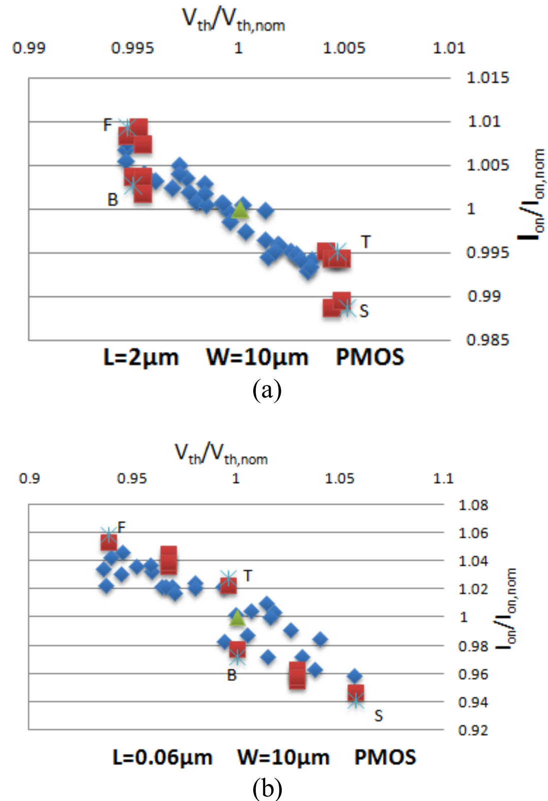


Fig.4. Die-to-die variation of p-MOSFETs: Diamond (blue) denotes the variation of measured data of different dies. Triangle (green) denotes the nominal data. Square box (red) denotes the simulated boundary points to model the variation pattern. Star (light blue) denotes also simulated points capturing the Fast (F), Slow (S), Top (T) and Bottom (B) corners of the variation.

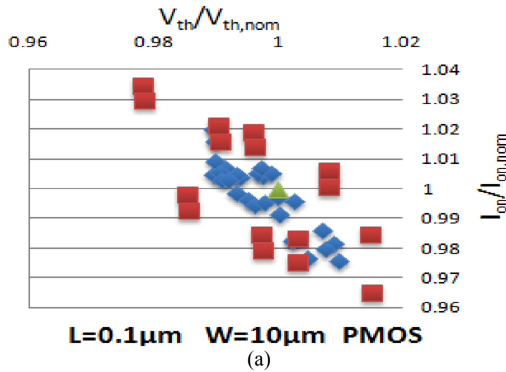
As theses corner points are given by the same microscopic parameter variation for all L, they can be directly used in conventional methodologies for simulating variation effects on circuits.

All together 16 Points are generated to model the measured die-to-die variation. The boundaries of the variation modeled by the points F, S, T and B for all channel length L is given below.

Symbol	Variation Boundary Combinations			
	NSUBC	MUESR1	NSUBP	XLD
F	+0.659%	-1.250%	-2.966%	-5.852%
S	-0.720%	+0.400%	+4.746%	+5.060%
T	-0.720%	-1.250%	+4.746%	-5.852%
B	+0.659%	+0.400%	-2.966%	+5.060%

Fig.5. Symbols represents boundary point of microscopic parameter variation, which are extracted from the variation of 65nm technology devices of dimension L=2µm, W=10µm and L=60nm, W=10µm with the same set of varied parameters.

The method of variation modeling shown in the Fig.3 is capable to model the long and short gate length devices as verified in Fig. 4 for constant W=10µm, simultaneously. The variation of the microscopic parameters as obtained from the long and short gate length device modeling as listed in Fig.5, is also valid to model the variation of the other intermediate gate lengths for constant W=10µm, and the result shows good agreement with the measured variation as verified in Fig. 6.



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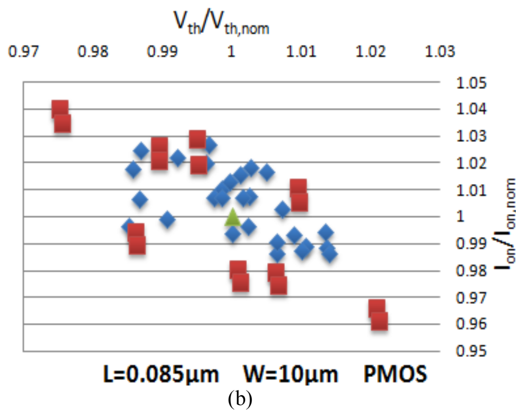

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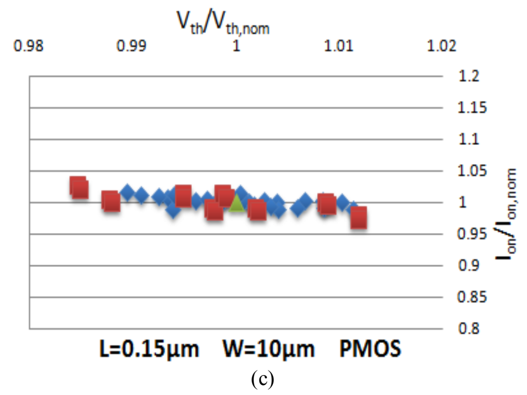

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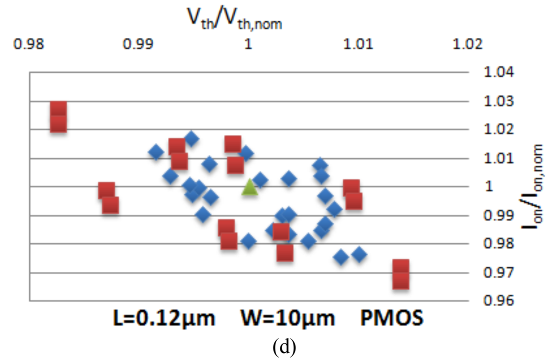

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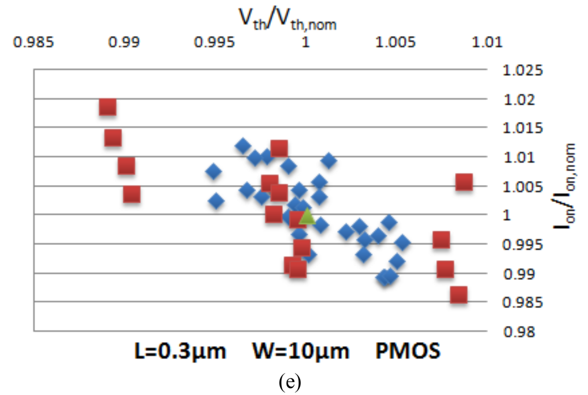


(e)

Fig.6. The parameter variation obtained from modeling of L=2µm,W=10µm and L=60nm,W=10µm, is used to model the above dimension devices. As can be seen the results fit for all intermediate gate lengths as well. Diamonds (blue) denote the variation of measured data over different dies. The triangles (green) denote the nominal data. Square boxes (red) denote the simulated points for the 16 combinations of the microscopic parameter variation boundaries to model the variation pattern.

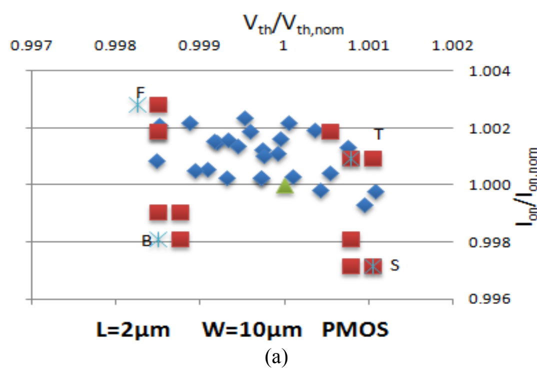
IV. WITHIN-DIE VARIATION

The differences of V_{th} and I_{on} for right and left transistors are measured for each particular combination of L and W and for all the 36 dies. These difference data (with a multiplication factor of root 2 to compensate for the variation statistics of 2 independent measurements) are then added to the corresponding values of the nominal die with the same L, W combination to derive the within-die variation of that particular L, W combination. In this way within-die variation of all the 12 L, W combinations are obtained. For modeling the within-die variation data, the same procedure is taken as explained in Fig.3 of section III for the die-to-die variation. As

the within-die variation reproduction obtained with this procedure was not completely satisfactory, the variation contribution of the NDEP parameter, which covers the depletion-charge contribution to the electric field, was included to further improve the reproduction results. So in this within-die modeling methodology, variation is first modeled with only 4 parameters up to best fitting result and then NDEP parameter is very finely tuned to get the perfect fitting result. For total variation modeling permutation of only 4 parameters are taken (same as in die-to-die modeling) and 5th parameter is varied just to improve the obtained result, so it gives total of 16 variation modeling points. The HiSIM2 parameters for modeling and analyzing the within-die variation are summarized in Fig. 7 below.

Device	Parameter	Meaning
Long	NSUBC	Substrate Doping
Long	MUESR1	Mobility degradation(oxide roughness)
Long	NDEP	Depletion charge contribution on effective-electric field
Short	NSUBP	Peak Pocket-doping concentration
Short	XLD	Channel length change

Fig.7.Microscopic model parameters used to model the V_{th}-I_{on} variation. Long refers to L=2μm and Short refers to L=60nm. These parameters are selected based on a sensitivity analysis for V_{th} and I_{on} and their physical effect on fabrication variation.



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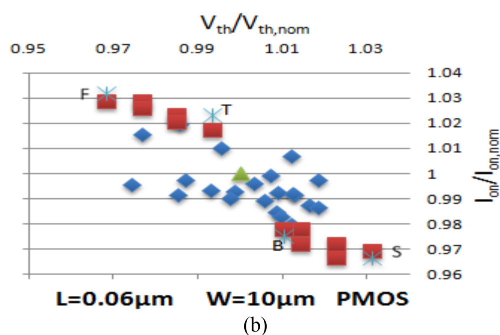


(b)

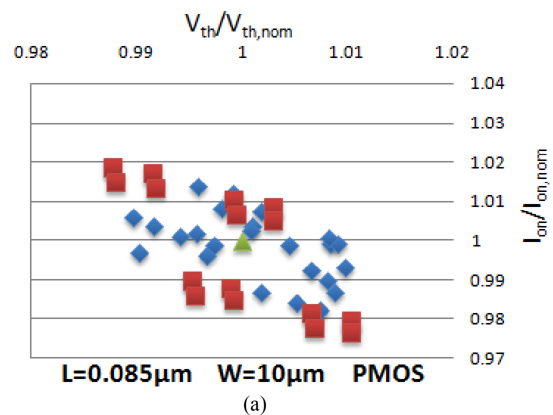
Fig.8. Within-die variation of p-MOSFETs: Diamonds (blue) denote the variation of measured data of different dies. Triangles (green) denote the nominal data. Square boxes (red) denote the simulated points to model the variation pattern. Stars (light blue) are also simulated points to model the extreme boundaries of the variation pattern, and are denoted with the letters F, S, T, B as in the case of the die-to-die variation.

All together 16 points are generated to model the measured within-die variation of long and short gate length devices as shown above in Fig.8. The boundaries of the variation are modeled by the points F, S, T and B.

Simulated Variation	Variation Boundary Combinations				
Symbol	NSUBC	MUESR1	NDEP	NSUBP	XLD
F	+0.15%	-0.56%	-0.19%	-1.78%	-3.93%
S	-0.21%	+0.56%	+0.19%	+2.54%	+3.14%
T	-0.21%	-0.56%	+0.19%	+2.54%	-3.93%
B	+0.15%	+0.56%	-0.19%	-1.78%	+3.14%

Fig.9. Boundary point variation of microscopic parameters, which are used to model the variation of 65nm technology devices of dimension L=2μm, W=10μm and L=60nm, W=10μm with the same set of varied parameters.

The microscopic parameter variation obtained from modeling of long and short gate length MOSFETs, as shown in Fig.9 is used to model the within-die variation of the other intermediate gate length MOSFETs. The obtained result is depicted in Fig.10 and verifies that simulated variation with 5 microscopic parameters completely models the measured within-die variation for all intermediate gate lengths as well.



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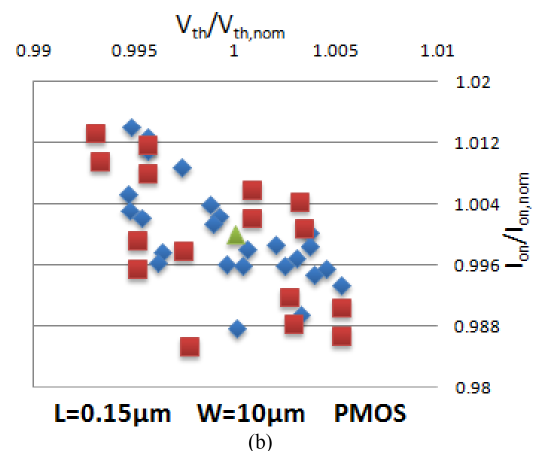

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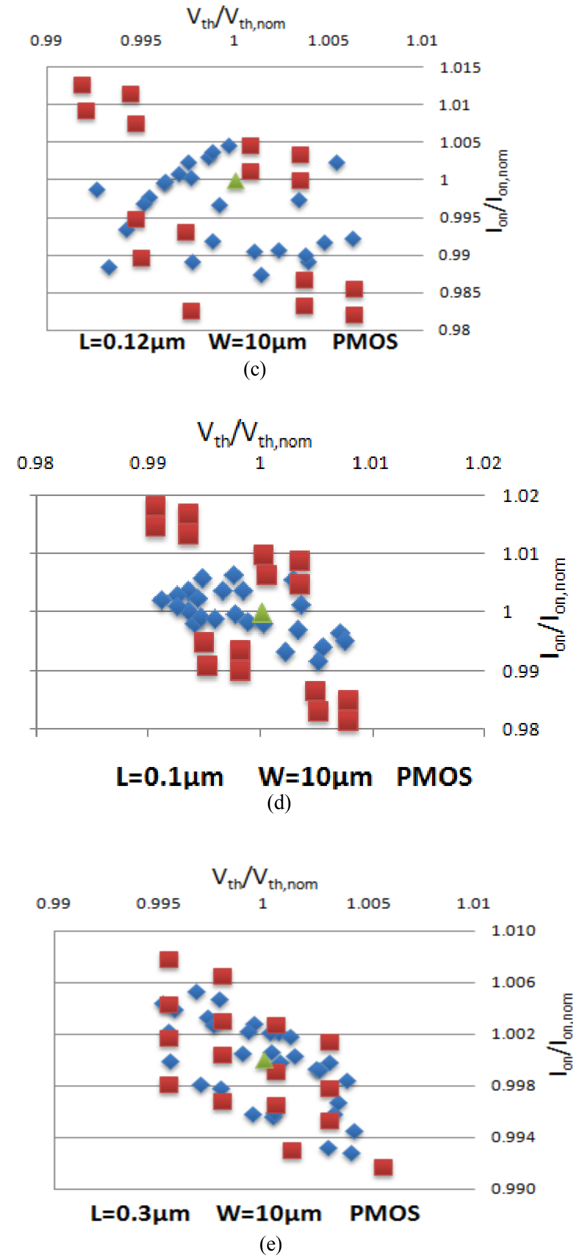

Fig.10. The parameter variation obtained from modeling of L=2µm, W=10µm and L=60nm, W=10µm, is used to model the above dimension devices, which reproduces the macroscopic variation at these gate lengths as well. Diamonds (blue) denote the variation of measured data of different dies. Triangles (green) denote the nominal data. Square boxes (red) denote the simulated points of all combinations of the parameter boundaries to model the variation pattern.

V. DISCUSSION OF RESULTS

L_{min} (XLD) refers to gate-length change of the minimum-gate-length device with L=60nm and W=10µm.

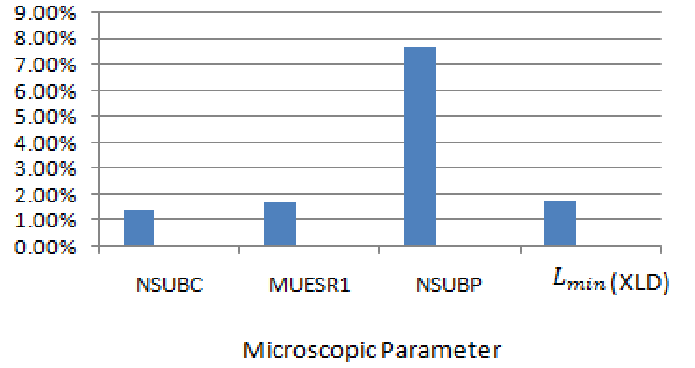

Fig.11. Overall percentage variation of microscopic parameters to model the die-to-die V_{th}-I_{on} variation.

From Fig.11 it can be seen that the die-to-die variations of the 3 microscopic parameters NSUBC (1.379%), MUESR1 (1.65%), L_{min}(XLD) (1.74%) are relatively small and contribute only moderately to the die-to-die variation. On the other hand, peak pocket-doping concentration NSUBP (7.712%) is found to vary substantially and is the main reason for high die-to-die variation increase at smaller gate length L.

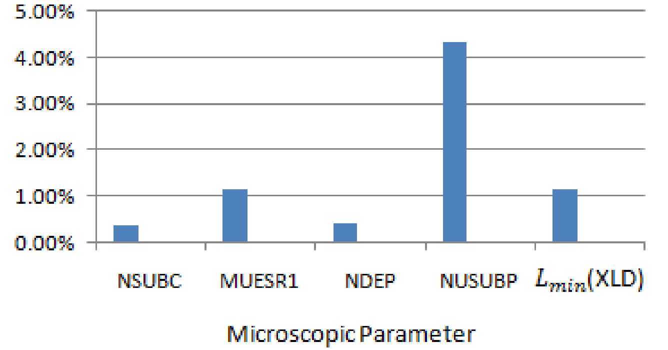

Fig.12. Overall percentage variation of microscopic parameters to model the within die V_{th}-I_{on} variation.

The variation-modeling method shown in the Fig.3 with only 4 relevant parameters does not give sufficient results for the within-die variation. However, by including a small variation for the additional NDEP parameter, quite good fitting result of the measured within-die variation could be achieved. As compared to the case of die-to-die variation the microscopic parameter variation is smaller in the case of within-die variation, which is expected from the closer proximity of the p-MOSFETs during the fabrication procedures. From Fig.12 we find that NSUBC (0.36%), MUESR1 (1.12%), NDEP (0.38%), L_{min}(XLD) (1.13%) show also quite small within-die variation, but the NSUBP (4.32%) variation, although smaller than for die-to-die variation, gives

again the dominant contribution also for the within-die variation.

VI. CONCLUSION

Our results demonstrate that only 4 microscopic parameters are required to model the die-to-die variation for the p-MOSFETs of a state-of-the-art 65nm CMOS technology. For sufficient accuracy of the within-die variation modeling, additionally the inclusion of the NDEP parameter variation is found to be necessary. Variation of NDEP signifies that the doping concentration is not uniform in the bulk but instead has a very small gradient in the direction perpendicular to the channel. The within-die NDEP variation is determined as 0.38%, which is quite small. When die-to-die variation is evaluated using NDEP with 0.38% variation, it shows no appreciable change of the result described in section III. Therefore, it can be concluded that die-to-die variation modeling with only the 4 main microscopic parameters is sufficient.

It can also be seen from the results that the microscopic parameter variation obtained from modeling the variation of large and short gate length MOSFETs is sufficient to model the variation of all the intermediate gate length MOSFETs as well. This finding is true in case of die-to-die as well as within-die variation, which verifies that the method of variation modeling shown in [3] is effective for both die-to-die as well as within-die variation modeling. This paper successfully shows the correlation between the macroscopic variation of V_{th}-I_{on} and microscopic parameter variation obtained with the HiSIM2 surface-potential-based compact model. The above results are expected to be very useful for including the fabrication-variation effects of p-MOSFETs in the simulation methodology for designing integrated circuits.

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