Targeted cooling with CVD diamond and micro-channel to meet 3-D IC heat dissipation challenge

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***Abstract*—Thermal simulation of a stack consists of three IC layers bonded "face up" is performed. It is shown that by inserting electrically isolated thermal through silicon via (TTSV) having Cu core and CVD diamond as a liner shell that extends across the layers to substrate, significant temperature reduction up to (103K) 62% can be achieved which also reflected through almost 60% reduction in thermal resistivity. Additionally simple microchannel integration with IC 3 layer and allowed fluid flow through the channel show transient temperature reduction. TTSV is also shown to be effective in mitigating severe heat dissipation issue facing 3-D IC bonded "face down" and logic layer stacked on memory substrate.**

Keywords—3-D IC; CVD Diamond; Micro-channel; Heat dissipation; through silicon via.

I. INTRODUCTION

3-D stacking of two or more IC layers is a promising way to ensure continued performance growth when geometrical scaling alone (coupled with performance boosters in recent nodes) is facing fundamental and economical scaling barriers [1]. However, power dissipation, which is known to negatively impact 2-D chip performance and reliability, is expected to be exacerbated further in 3-D IC as heat generated by each IC layer must be dissipated through a smaller 3-D chip foot print [2-5]. This results in a sharp increase in power density and is a potential killer to 3-D IC development if left unmanaged.

Long back Lee *et al* [6] improve thermal problem in IC, by using thermal via. It is shown that as the size of thermal via islands increases, more heat removal is achieved at the expense of Si area that can be utilized for ICs. Rahman *et al* [3] suggested that Cu thermal via could help to relieve heat dissipation problem in 3-D ICs. Goplen *et al* [6] assigned specific areas of a 3-D ICs and used to adjust their effective thermal conductivities. The thermal via placement method makes iterative adjustments to these thermal conductivities in order to achieve a desired maximum temperature objective. With a simple 3-D circuit model, it is shown that via density strongly affects the spatial temperature distribution. Singh and tan [5] showed significant reduction of top layer temperature using TTSV and also found that there is no heat dissipated by electrical TSV. However, they have done quit comprehensive study on the effect of thermal through silicon via (TTSV) on the temperature profile of a multi-layer 3-D ICs but they have only consider all level as logic level. One of the strong attractions of 3D IC integration is heterogeneous integration which can stack logic along with memories. Herein in this work, a additional thorough thermal analysis of a vertical stack consists of three IC layers bonded face up (FU) is carried out. The objective is to examine the effectiveness of thermal through silicon via (TTSV) and targeted cooling with CVD diamond liner in mitigating heat dissipation challenge in 3-D IC and using simple microchannel.

II. 3-D IC THERMAL MODELING

Commercial FEM tool is used in thermal analysis. At steady state, constant properties and uniform heat generations in homogeneous media the FEM simulator solves the general heat equation for conduction expressed as:

$$-n.(-k\nabla T) = q_o + h(T_{\inf} - T) \quad (1)$$

Where k is the thermal conductivity of material, q_o is the inward heat flux (W/m^2), h is the heat transfer coefficient of materials, n is the normal vector to the boundary and $T_{\inf}$ is the constant ambient temperature. Adiabatic boundary condition is applied on four side walls as well as on top surface.

The simulated 3-D stack with TTSV is schematically illustrated in Fig. 1. TTSV consists of Cu core and SiO_2 liner shell. In this proposed model, we assume a uniform heat flux (generated by devices and interconnects joule heating) across the entire chip. Unless otherwise stated, all IC layers are logic blocks with power density of 70 W/cm^2 each. In addition, we also assume that heat sink is sufficient to keep the bottom substrate at temperature 358.3K (85^{o}C). Material properties used in FEM analysis are given in Table I.

III. RESULTS AND DISCUSSION

A. TTSV for cooling the IC layers

In 3 stacked IC layer heat generated in the upper layers cannot be dissipated effectively to the substrate. This problem can be mitigated by the insertion of TTSV that extends through the

Table I. Properties of materials used in the simulation.

Material	*Thermal Conductivity (W/m.K)*	*Density (kg/m^3)*	*Heat Capacity (J/kg.K)*	*Dielectric Constant*
Air	0.048	0.524	1055	1
Silicon	163	2330	703	12.1
Silicon Oxide	1.38	2203	703	3.9
Copper	400	8700	385	-
Polyimide	0.15	1300	1100	2.4-3.2
CVD Diamond	1100	3515	502	2- 3.4

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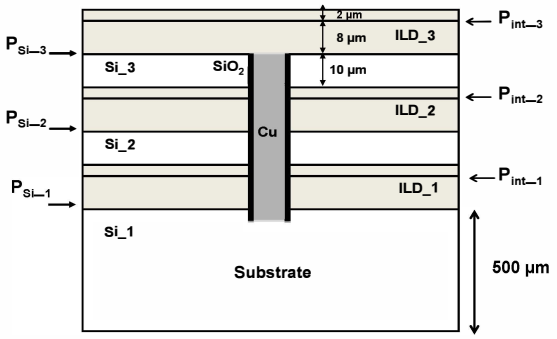

Fig. 1: Schematic of heat removal model using TTSV across different IC layers to substrate. Si substrate thickness is 500µm and other Si layers are 10µm thick. Carbon doped oxide (CDO) is used. as ILD with thermal conductivity of 0.39W/mK. TTSV diameter is 20µm, which consists of Cu core (18µm) and SiO_2 shell liner (1µm). P_{Si} is heat flux at top surface of each Si generated due to device power while P_{int} is heat flux due to joule heating in metal wires embedded in ILD layers. TTSV extends 10µm into Si substrate. Simulated area is 200 µm x 200 µm

IC layers to the substrate. Cooling effect with TTSV is shown in Fig. 2. It suggests that TTSV results in significant reduction in maximum chip temperature of 62K or 37% with reference to sink temperature. It suggests that trap heat at ILD layer gets conducted through TTSV this is also observed earlier [5].

B. Targeted cooling by using CVD Diamond

The dielectric liner of TTSV provides electrical insulation between Si and Cu core and its property is extremely important in heat dissipation. Besides SiO_2, polyimide and CVD diamond (CVDD) are also evaluated. Due to its high thermal conductivity and electrical resistivity [3] which allow to conduct heat from Si substrate to TTSV (earlier block by poor thermal conductivity of SiO2 or polymide liner), CVDD liner makes TTSV extremely effective in cooling as shown in Figs. 3 and 4 along the horizontal and vertical direction of IC layers respectively.

With its promising cooling property, CVDD can be used selectively for targeted cooling of IC layers on a 3-D stack. We demonstrate this in Fig 5. By using CVDD at any selected IC layer, one can provide greater cooling to layers which are at higher temperature. Fig. 6 shows the effective thermal resistance of the layers on 3-D stack with TTSV using a combination of liners. TTSV, when coupled with CVDD, reduces the effective thermal resistance significantly by more than 60% as compared no TTSV.

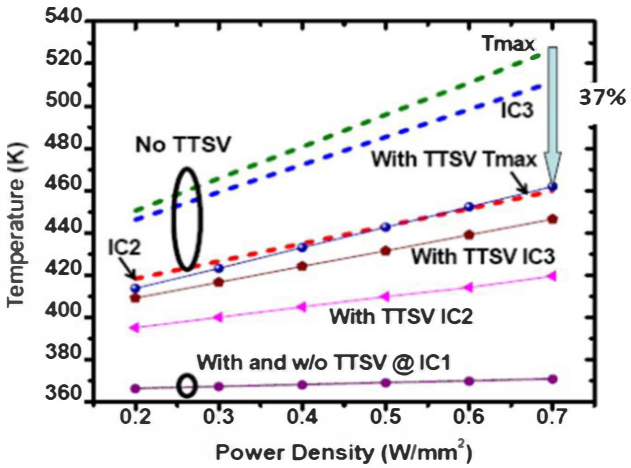

Fig. 2: A comparison of IC layers temperature with the introduction of TTSV (18 µm Cu core and 1 µm oxide liner). Significant temperature reduction is clearly seen with 37% using sink temperature as reference.

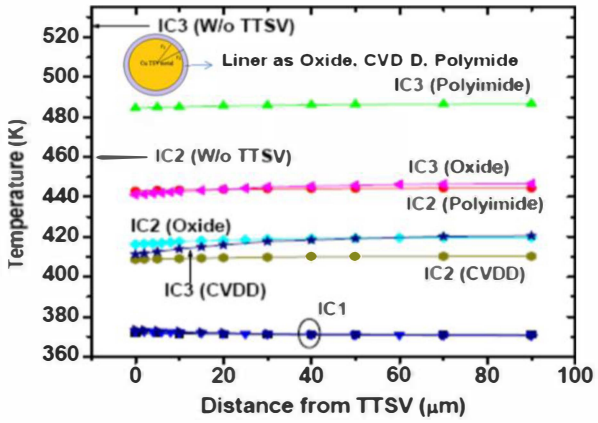

Fig. 3: Temperature profile with various dielectric liners. CVD diamond demonstrates the best cooling capability.

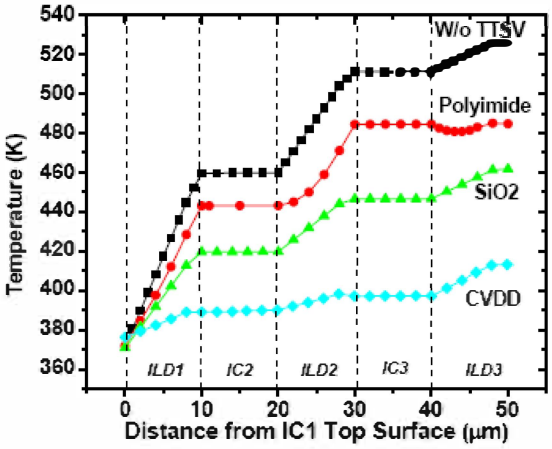

Fig. 4: Significant cooling improvement can be achieved by using liner with higher thermal conductivity such as CVDD. Significant cooling observed about 62% by application of CVD Diamond wit respect to constant sink temperature.

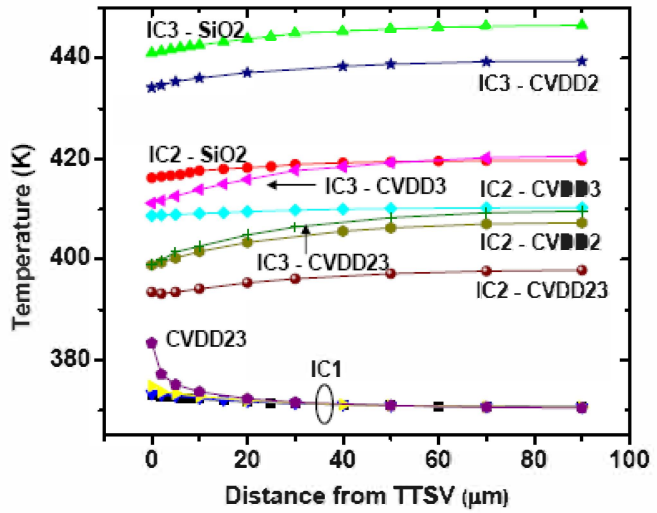

Fig. 5: CVDD liner can be applied selectively to achieve targeted cooling at a desired IC layer. For example, using CVDD at IC3 only [IC3-CVDD3] provides better cooling in IC3 compared with the use of CVDD at IC2 only [IC3-CVDD2].

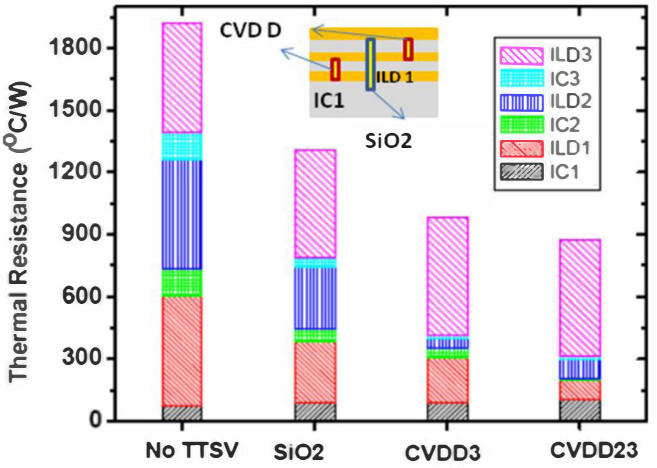

Fig. 6: Extracted effective thermal resistance values. Thermal resistance of IC layers improves with the insertion of TTSV. Further reduction is expected when CVDD is used in IC3 [CVDD3], and when CVDD is used in both IC2 and IC3 [CVDD23].

C. *Transient Targeted cooling by using micro-channel*

Conventional simple single micro-channel structures (Hydraulic diameter 8um and length-200um) at IC bottom of IC layer was investigated with different liquids (water, silicone oil, and fluorinert) without TTSV. Transient response of different liquid is tabulated in table 2. We can observe the transient temperature rise in case of liquid is much better however very small. It's noteworthy that the channel dimension is very small and it covered very small fraction of total cooled area. But it showed the potential to cool the localized area in at different layer depending on stacking of ALU block. Ongoing work is mitigate the heat both targeted and bulk is on.

Table II. Transient temperature in IC3 level with varying different liquid using simple microchannel.

Transient Time (sec)	Transient Temp (K)			
	W/o µ-channel	Water	Silicon oil	Fluorinert
1	293.93	294.04	294.04	294.04
1.2	603.32	603.23	603.43	603.36
1.4	912.02	911.81	912.19	912
1.6	1220.6	1220.3	1220.9	1220.7
1.8	1529.3	1528.8	1529.6	1529.6

D. *Technology choice and impact of heat on IC layers*

Due to several processes stacking option (facing up (FU) and facing down(FD)), it is important to investigate the heat impact and there mitigation on different stacking scheme. . However, temperature increases in top IC layers due to thicker total ILD layer compared with FU stack. This can be circumvented effectively with TTSV as evidenced from. Figure 7 it is evident that even without TTSV temperature of FD stacking is higher for IC3 level as compared FD due to thicker ILD layer in FU scheme. However after application introduction of TTSV the temperature TTSV drop dramatically owing to thermal conductive path provided by TTSV. However still temperature in at each IC layer more in FD scheme. So it is evident that FD is useful as compared to FD in term of heat mitigation and device reliability.

E. *Heterogeneous Integration and Heat Impact*

One of the salient features of 3-D stacking is possibility of potential heterogeneous integration of chips. Probably first one to get tested is integration of memory to logic. In 3 layers stacking various combinations of logic and memories stacking is possible. We have investigated for two logics and one memory as well logic and two memories and their combination. We have ruled out the case for logic in between to memoirs as well memory in between two logics, seeing the fabrication complexity. As memories generate less heat we have taken power density for memory is at 5W/cm^2. Less temperature rise is observed (see Fig 8) when logic block is close to the substrate due higher heat source is nearer to sink. However in this configuration input power to logic required longer interconnects which moderately impact the advantage of newer architecture and also it required electrical via which will cross across all the layer exposing the memories layer with high electric field resulting degrades it reliability. So by reversing the configuration this problem can be handled however the due to isolate from sink rise the temperature of IC layers. This can be encounter by our earlier finding of targeted cooling such as CVD Diamond or using micro-channel flow at targeted area. Top logic block can be cooled by using TTSV, with CVDD targeted cooling if needed, hence making thin logic on memory substrate a compromise between thermal and electric field management in 3-D IC as shown in Fig. 9.

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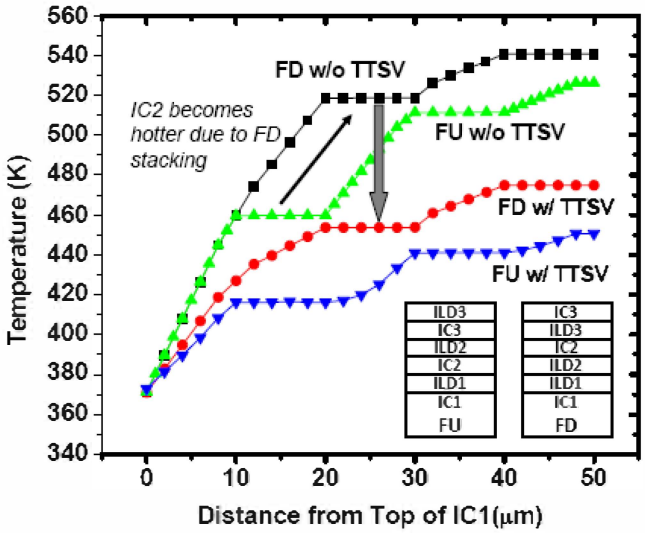

Fig. 7: Impact of heat and TTSV to mitigate different integration technology i.e impact bonded facing down (FD) compared with facing up (FU).

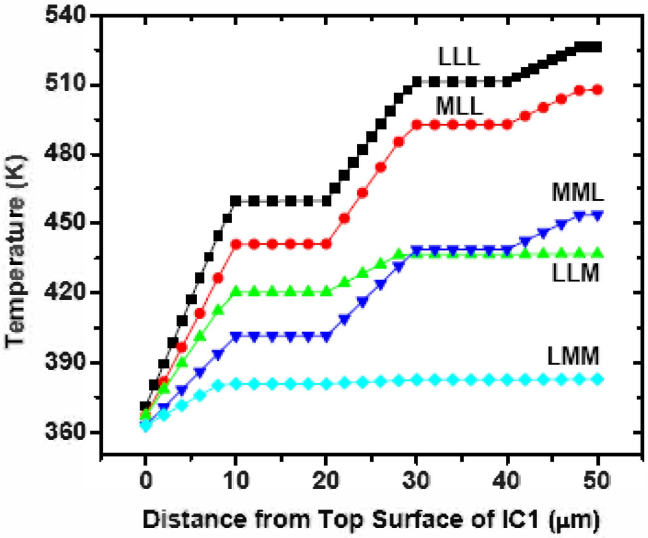

Fig. 8: Various combinations of logic and memory stacking and the resulting temperature cross section. By placing logic on memory substrate (MLL or MML), logic block is isolated further from heat sink and experiences huge temperature rise compared with LLM or LMM.

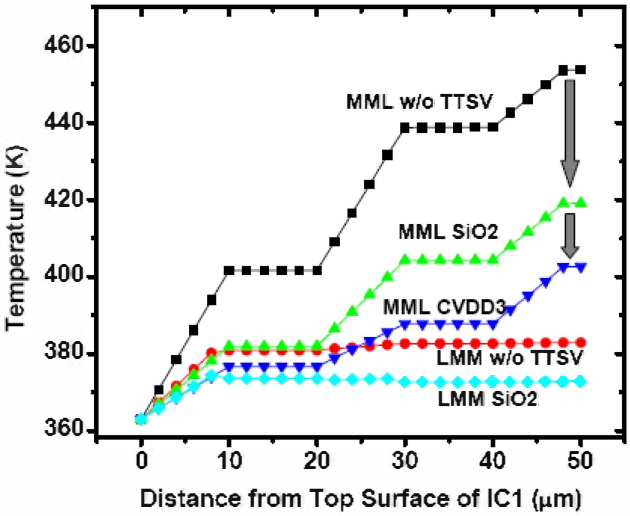

Fig. 9: By using logic block as the substrate, one can control the 3-D chip temperature effectively as heat from logic block can spread in Si substrate and dissipate through heat sink [LMM w/o TTSV]. However, I/O and power pins to the logic block (formed by ETSV) must cut across the memory chips hence reducing memory area density and inducing high electric field that causes reliability concern to memory block. To overcome these, logic block is placed on top and directly next to the package but one ends up with high temperature at the top logic layer [MML w/o TTSV]. TTSV can mitigate this problem by providing 37.7K of cooling [MML SiO_2]. By placing CVDD selectively in the logic layer [MML CVDD3], one can expect even higher temperature reduction of 51.1K.

IV. CONCLUSION

Targeted and bulk thermal modeling of 3 IC layers stack has been carried out and observed that chip temperature can go very high without managing it. It is observed that TTSV with conductive liner such as CVD diamond is very useful to mitigate heat from different IC levels. We have observed about 120 K temperature difference after application of CVDD as a liner material which is about 52% reduction in temperature. In heterogeneous integration of logics and memories was also evaluated and found that with the help of targeted cooling using CVD Diamond MML or MLL configuration can be used for stacking for future application as it turns out best shielded with thermal and electrical affects. We have observed that due to CVD D liner in TTSV reduced the temperature by 51 K in case of MML configuration. Present results will be useful to design the TTSV as well arrangement of stacking of Memories and logic for future application.

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REFERENCES

[1] P. Emma, E. Kursun, "Is 3D Chip Technology the Next Growth Engine for Performance Improvement?" *IBM J.Res & Dev.* Vol. 52, No. 6, 2008,pp. 541–551.

[2] Im and K. Banerjee, "Full Chip Thermal Analysis of Planner (2-D) and vertically Integrated (3-D) High Performance ICs," *Int. Electron Device Meeting*, 2000, pp. 727-730.

[3] A. Rahman and R. Reif, "Thermal analysis of three-dimensional (3-D) integrated circuits (ICs)," *Proc. IITC*, 2001, pp. 157–159.

[4] Shiv Govind Singh and Chuan Seng Tan, "Thermal mitigation using thermal through silicon via (TTSV) in 3-D ICs", IEEE IMPACT conference Taiwan, 2009, pp 182-184.

[5] Shiv Govind Singh and Chuan Seng Tan, "lmpact of thermal through silicon via (TTSV) on the temperature profile of multi-layer 3-D device stack", IEEE 3 D IC conference 2009, 978-1-4244-4512-7/09.

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