IoT Enabled Communication Device with Mixer Less Low Complex QPSK Based Transmitter Architecture for Low Frequency Applications

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***Abstract*—Technological development in the area of wireless communications lead to the requirement of tight integration of both the digital and analog functional units. Integrating mixers is a challenging task, especially in mixed signal design. IoT communication devices require low design complexity as we expect millions of devices connected. In this paper we propose a mixer less low complex QPSK based transmitter architecture targeting low frequency applications which reduced the complexity in transmitter design. A prototype has been developed using Bipolar Junction Transistors (BJTs) and FPGA as the base band controller. The design can easily be adapted to MOSFET technology and modulation is achieved without the need of generating the carrier externally. The prototype developed was tested successfully by generating frequencies of range varying from 1 KHz to 120 MHz. The proposed architecture can also be used for any other digital modulation scheme such as BPSK, FSK etc.**

***Keywords*—QPSK, BJT, Mixer, FPGA, Modulator.**

I. Introduction

In recent years, the design methodologies for wireless technologies has undergone many changes. The complexity in designing of mixers, impedance matching methodologies and mixed signal design techniques has been reduced. Still designing the mixers is a challenging task due to the difficulty in integrating the analog design with the digital functional units. In [1], authors have discussed various issues that have to be encountered in mixed signal designs. Due to the growing number of connected devices leading to hyper connected scenario, development of IoT communication devices with low complexity and low power consumption is the need of the hour [2]. In this paper we propose a mixer less low complex transmitter architecture for low frequencies, which reduces the complexity by avoiding the use of mixers in the design. Most of the functional units present in the architecture can be implemented all digital, with only one analog functional unit. Primary advantage of digital functional units is in the ease of design and power savings that can be achieved.

Designing of mixer involves consideration of many factors which affect the performance such as conversion gain, IIP3 (Third Order Intercept Point), noise figure and gain conversion etc. This makes the design more complex. There are two kinds of mixers in practice, passive and active mixer. Active or passive implementations are decided depending on the application, and there are advantages and disadvantages. As an example, a passive implementation that uses diodes as nonlinear elements or FETs as passive switches, exhibits a conversion loss rather than gain. This may impact the overall noise performance of the system, so in this case an LNA is usually added prior to the mixer. Passive mixers are widely used due to their simple construction, wide bandwidth, and good intermodulation distortion (IMD) performance. Active mixers are mostly used for RFIC (Radio Frequency Integrated Circuit) implementation. They are configured to provide conversion gain, good isolation between the signal ports, and requires less power to drive the LO (Local Oscillator) port. They can be monolithically integrated with other signal processing circuitry and are less sensitive to load-matching, which is the primary factor affecting the power transfer efficiency. Different architectures of mixers were proposed such as [3] & [4], in which the performance of the mixer has been evaluated. In [3], the authors used a double balanced mixer, which is a modified version of the Gilbert mixer. The major disadvantages of the Gilbert mixers are the requirement of high LO drive and ports are highly sensitive to reactive loads. In [5], the QPSK modulation is achieved using a balanced modulator. The proposed architecture, however does not use a mixer, makes use of an analog bank which converts the digital samples to modulated analog signal. In IoT and M2M scenarios, where billions of devices are expected to be connected, the design of low complex and low power consuming communication devices leading to very low maintenance are required. Hence there is a need for low complex architectures for communication devices. The result of the low complexity in the proposed architecture is due to the absence of mixers which primarily raise issues in mixed signal designs. The proposed architecture can also be adapted for any digital modulation schemes such as BPSK, QAM and FSK with a little implementation changes which greatly aids in Software Defined Radio (SDR) scenario. In SDR, the components which are implemented in a dedicated hardware can be implemented using software on an embedded system with required capabilities which can improves the ease of reconfigurability. In the proposed architecture, the modulation scheme can be changed through a minor reconfigurability of the samples generation, which makes it suitable for SDR scenarios.

The rest of the paper is organized as follows. Section II revisits the QPSK modulation and discusses the architecture of the proposed low complex QPSK based transmitter. Section III discusses the performance analysis of the proposed architecture and section IV concludes the paper.

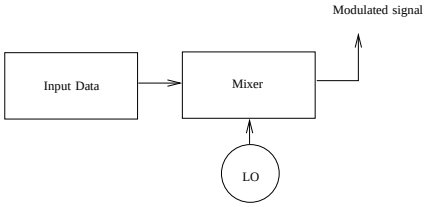

Fig. 1: Proposed architecture of low complex QPSK modulator

II. Proposed architecture of the mixer less QPSK modulator system

Fig. 1 shows the traditional transmitter architecture which most of the architectures employ. It generally consists of a LO stage which generates the carrier signal and mixer which up-converts the base band signal to pass band. In this section we discuss the architecture of the complete low complex QPSK based transmitter system which is shown in Fig. 2. In the following subsections each of the functional units involved in the proposed low complex architecture has been described briefly.

A. QPSK modulation

Digital modulation bridges the transmission of digital symbol into wireless medium [6], [7] & [8]. A sequence of digital symbols are used to alter the characteristics of the carrier. The bandwidth and bit rate depends on the modulation scheme we use. In QPSK we use two quadrature carriers (sine and cosine). Each of the message symbol is divided into two phases, in phase and quadrature phase components which uses the two carriers for modulation. The number of bits transmitted in each of the phases are same. The mathematical definition of the QPSK signal can be stated as shown below

$$S_i(t) = \begin{cases} \sqrt{\frac{2E}{T}} cos(2\pi f_c t + \theta_i), & 0 \leq t \leq T \\ 0, & otherwise \end{cases} \quad (1)$$

$$\theta_i = (2i-1)\frac{\pi}{4} \quad (2)$$

In (1), $S_i(t)$ indicates the modulated wave, f_c represents the carrier frequency or center frequency and i varies from 1 to 4 indicating the message symbol. θ_i denotes the phase associated with the i^{th} message symbol, T is the symbol duration and E is the transmitted signal energy per symbol. Upon expanding (1), it results in the following form

$$\begin{aligned} S_i(t) = &\sqrt{\frac{2E}{T}} cos\left[(2i-1)\frac{\pi}{4}\right] cos(2\pi f_c t) \\ &- \sqrt{\frac{2E}{T}} sin\left[(2i-1)\frac{\pi}{4}\right] sin(2\pi f_c t) \end{aligned} \quad (3)$$

The constellation diagram can be realized as shown in Fig. 3 and the signal space characterization is shown in TABLE I. In Fig. 3, all possible phase transitions have been indicated with the arrows. The maximum phase shift possible is 180° which are indicated by the diagonal arrows. All the possible input message symbols are represented with S_1, S_2, S_3 and S_4 in the constellation diagram. For a detailed description on the QPSK system, one can refer to [6] & [9].

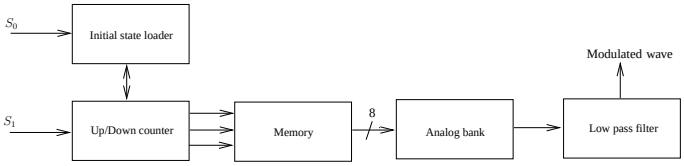

Fig. 2: Proposed architecture of low complex QPSK modulator

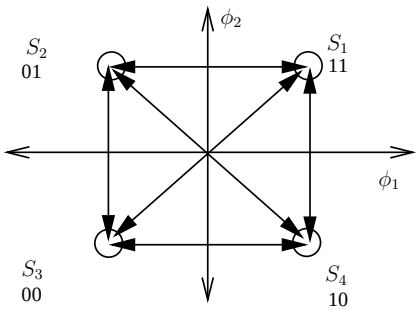

Fig. 3: Constellation diagram for QPSK system

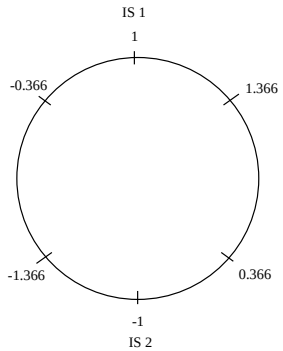

Fig. 4: Symbol cycle of a QPSK system

In the rest of the paper we assume the carrier frequency to be f_c. Upon using a sampling rate of $6f_c$, symbol energy of T in a single period of modulated signal we can have six discrete samples of the modulated signal. Considering the first case where the message symbol is 10, the sampled signal and the discrete sample values of the modulated signal can be represented as below.

$$\begin{aligned} &S(n) = cos(2\pi f_c n T_s) - sin(2\pi f_c n T_s) \\ &S(0) = 1, S(1) = -0.366, S(2) = -1.366, \\ &S(3) = -1, S(4) = 0.366, S(5) = 1.366 \end{aligned} \quad (4)$$

Now sampling the modulated wave for all four message symbols, each of them results into the following samples as shown in TABLE II in a single period of the modulated signal.

B. Symbol cycle

In TABLE II, all the six samples are same for all the 4 message symbols. The only difference is in the occurrence of those samples in the time series. The message symbols 11 and 10 has the same first sample '1' and the rest of the samples

Input symbol	Phase of QPSK signal	Coordinates on constellation diagram
10	$\frac{7\pi}{4}$	$\left(\sqrt{\frac{E}{2}}, -\sqrt{\frac{E}{2}}\right)$
00	$\frac{5\pi}{4}$	$\left(-\sqrt{\frac{E}{2}}, -\sqrt{\frac{E}{2}}\right)$
01	$\frac{3\pi}{4}$	$\left(-\sqrt{\frac{E}{2}}, \sqrt{\frac{E}{2}}\right)$
11	$\frac{\pi}{4}$	$\left(\sqrt{\frac{E}{2}}, \sqrt{\frac{E}{2}}\right)$

TABLE I: Signal space characterization for QPSK system

Input symbol	Modulated signal	Set of samples
11	$S_1(t) = cos(2\pi f_c t) - sin(2\pi f_c t)$	{ 1, 1.366, 0.366, -1, -1.366, -0.366 }
10	$S_2(t) = -cos(2\pi f_c t) - sin(2\pi f_c t)$	{1, -0.366, -1.366, -1, 0.366, 1.366 }
01	$S_3(t) = -cos(2\pi f_c t) + sin(2\pi f_c t)$	{-1, 0.366, 1.366, 1, -0.366, -1.366 }
00	$S_4(t) = cos(2\pi f_c t) + sin(2\pi f_c t)$	{-1, -1.366, -0.366, 1, 1.366, 0.366 }

TABLE II: Samples of modulated signal corresponding to individual message symbol

Input symbol	Initial state
11 & 10	IS1
01 & 00	IS2

TABLE III: Initial states corresponding to individual message symbol

are reverse in order for message symbol 10 compared with the message symbol 11. The symbol cycle for the QPSK system for a symbol energy of T is shown in Fig. 4. In the symbol cycle IS-1 denotes the initial state 1 and IS-2 denotes initial state 2. Initial state can be defined as the first discrete sample when the input message symbol changes. Whenever a new message symbol from the available symbols comes as an input, the first sample of the modulated signal is one of these two initial states. The choice of initial states are shown in TABLE III.

The initial state depends only on the I phase component of the message symbol and the following samples in the modulated signal depends on the Q phase component of the message symbol. If the Q phase component of the message symbol is 0, the symbol cycle is traversed in anticlockwise direction else the symbol cycle is traversed clockwise with reference to the initial state. The same set of six samples are periodically repeated for the entire symbol duration which results in the discrete QPSK modulated wave as shown in Fig. 5. For modulating a digital symbol now the process can be of generating these samples at a periodic intervals continuously after deciding the initial state and the symbol cycle traversal.

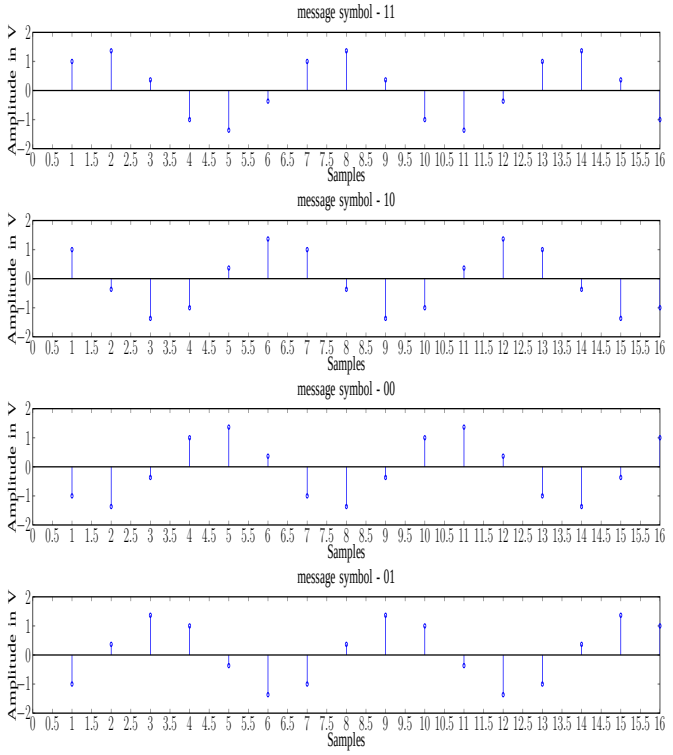

Fig. 5: Sampled signal of the QPSK modulated wave for 4 symbols

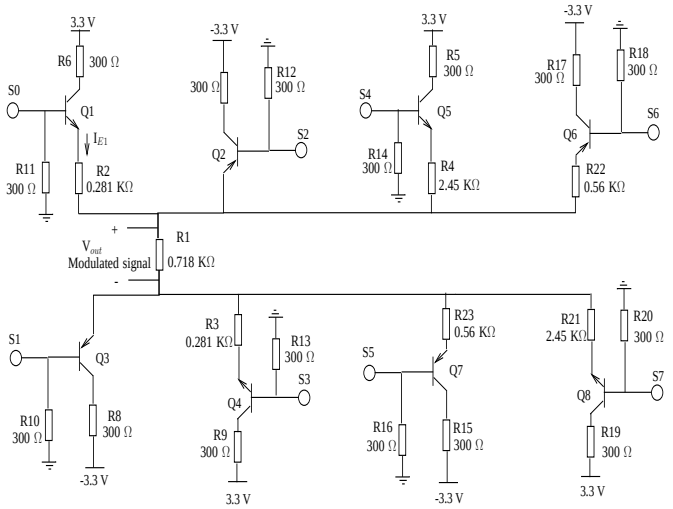

Fig. 6: Proposed architecture of analog bank

C. Analog bank

The analog bank generates all the six individual samples based on an eight bit keying sequence as input. It is developed using BJTs, which aids in a low complex design and low cost. The in house developed analog bank at IIT Hyderabad is shown in Fig 6. The main aim in developing using the BJTs is their ease of fabrication and the low power consumption. From the technology point of view the fabrication process of BJTs is well studied and established. Other advantage of the analog bank is to reduce the complexity of integration in the mixed signal design (digital base band and RF). The analog bank operates in co-joint with the counter controlled memory unit which operates using LVCMOS33 standard. All the transistors used in the construction of prototype for the analog bank are operated in the common emitter configuration and requires 3.3 V dual power supply. The prototype for analog bank is constructed with the 2N2222A NPN transistors [10], 2N3702 PNP transistors [11] and resistors. It does not consists of any storage elements which makes the fabrication much easier and

Address location	Input keying sequence S[0:7]	Output amplitude
000	10100110	1.36602
001	01101010	0.36602
010	01010010	-1
011	01010110	-1.36602
100	01100101	-0.36602
101	10100100	1

TABLE IV: Address location for the keying sequence and corresponding output sample produced by analog bank

low area.

The keying sequence provided at the 8 bit input of the analog bank decides the output voltage across the resistor R_1. The output voltages for the corresponding input keying sequence are shown in TABLE IV. If the keying sequence provided by the memory unit is 10100110, voltages at S0, S2, S5 and S6 are 3.3 V whereas at S1, S3, S4, S7 are 0 V. The transistors Q2, Q4, Q5, Q6, Q7 and Q8 will be in cut-off region. Transistors Q1 and Q3 will be in active region. The current passing through the resistor R1 is then equal to I_{E1}. Value of I_{E1} can be calculated as shown below.

$$\begin{aligned} &V_{S0} = 3.3\ V, V_{BE1} = 0.7\ V, V_{BE2} = 0.7\ V \\ &I_{E1} = \frac{V_{S0} - V_{BE1} - V_{BE2}}{0.281K + 0.718K} = 1.90mA \\ &V_{out} = I_{E1}R_1 = 1.36V \end{aligned} \tag{5}$$

Upon providing a proper keying sequence, we can generate the necessary amplitudes. Using the analog bank we can now generate the samples for the modulated wave. For providing the keying sequence for the analog bank we use the memory which is controlled by a counter and initial state loader.

D. Memory

Memory generates the keying sequence for analog bank depending on the input fed by the counter. The keying sequences for all the six samples are stored in successive memory locations. Based on the input address provided to the memory functional unit, proper output sequence can be generated. The output sequence generated then triggers the analog bank to generate the required output sample. The memory used is of 8 bit width and 6 bytes depth. TABLE IV shows the address location of the memory storage and the corresponding data stored in the address. LVCMOS33 standard is used for the memory output, logic level 1 is represented with 3.3 V and logic level 0 is represented with 0 V. The transition width during switching should be made as small as possible to achieve better accuracy for the modulated wave.

E. Up/Down counter

It is used for selecting the appropriate memory location which can generate the required samples at the output from analog bank. The functionality of the up/down counter is to count the values in the range of 0 to 5 in up or down fashion. The selection of up or down counting depends on the Q phase component of the message symbol. If the Q phase component is 0 the counting is in down fashion else it is in up fashion with reference to the initial state of the counter. The main aim of the counter is to organize the output samples according to the input message symbol. If the input message symbol is 11 the symbol cycle is traversed in clock wise direction. When the Q phase component is 1 the counter is up fashion and generates the analog samples from analog bank which implicates the symbol cycle being traversed in the clockwise direction. The initial state of the counter is loaded using the initial state loader. The clock frequency for the counter is the sampling rate we use, which depends on the center frequency we are targeting for the application. If we change the input clock frequency for the counter, the center frequency changes. The calculation of center frequency is given below

$$\begin{aligned} Sampling\ frequency &= f_s \\ Center\ frequency &= f_c \\ f_c &= \frac{f_s}{6} \end{aligned} \tag{6}$$

In the above equation, f_s is the sampling frequency and it is assumed to be six times the center frequency f_c. If we change the sampling frequency the center frequency of the modulated wave changes. Here the sampling frequency is determined by the clock frequency with which the counter operates. Targeting to a center frequency of 120 MHz will require a clock speed of 720 MHz for the counter.

F. Initial state loader

The initial state loader aids to reset the counter to an initial state every time the message symbol changes. If the message symbol is 11 the first sample in the modulated wave is 1.33 V, which can be generated by feeding the keying sequence stored in the memory location 000. When the message symbol changes to 11 at the input of the transmitter section, the counter should point to the memory location 000. The initial state loader points only to two states, IS-1 and IS-2. The keying sequences required to generate IS-1 and IS-2 are stored in memory locations 000 and 011. The initial state loader will only initialize the counter with any of these two values. The input to the initial state loader is the I phase component of the message symbol. If the I phase component is 1, the counter is initialized with the value 000 else it is initialized with 011.

G. Low pass filter

The low pass filter is a simple RC filter which eliminates the noises at high frequencies. It's primary use is to remove stair cases generated from the signal acquired from analog bank and generate a smooth continuous modulated signal, thereby eliminating co-channel interferences.

III. PERFORMANCE ANALYSIS

A hardware prototype shown in Fig. 7 for the proposed architecture described above is developed in IIT Hyderabad. The center frequency targeted is 208.3 KHz, which requires a sampling rate of 1.25 MHz. The frequency supplied to the counter is 1.25 MHz. Architecture of the hardware prototype is shown in Fig. 8. All the digital functional units have been implemented using Spartan 3E FPGA and the analog bank is developed in IIT Hyderabad. Fig. 10 shows the modulated signal acquired from the analog bank of the developed hardware prototype. From Fig. 10 one can infer the distortion in the signal at the hold positions, which are mainly caused due to the presence of the distortion in the keying sequence

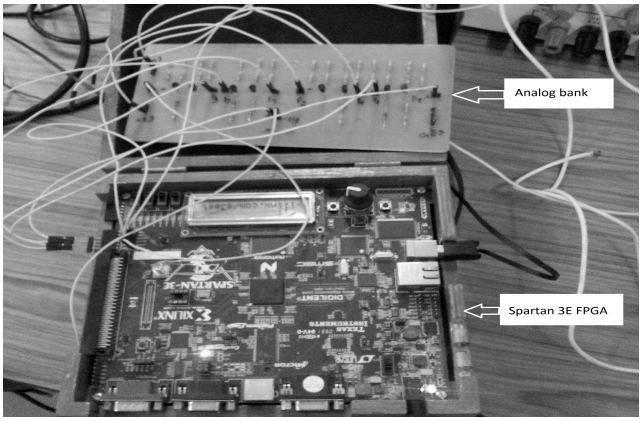

Fig. 7: Hardware prototype of the proposed low complex QPSK based transmitter architecture developed in IIT Hyderabad

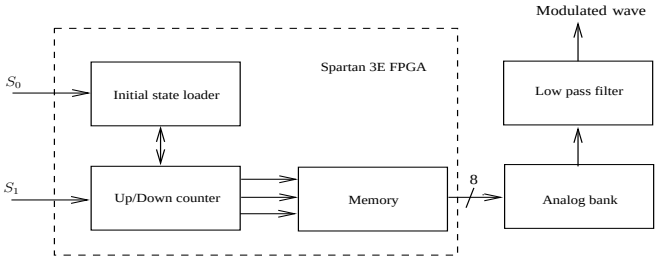

Fig. 8: Architecture of the hardware prototype

generated from the memory unit and can be eliminated upon using a low pas filter. The modulated signal generated after smoothening using a low pass filter is shown in Fig. 9. The analog bank is level sensitive to the keying sequence generated by the memory unit on the FPGA. The logic level high generated by the memory unit should have to maintain a voltage level of 3.3 V without any distortion. A better signal with higher frequency can be generated upon generating a good quality keying sequence from the FPGA, which is a limitation in the Spartan 3E FPGA. The prototype developed is observed to be a low complex due to the elimination of mixers. Due to rapid growing number of devices which may lead to hyper connectivity scenario, these low complex communication devices with less maintenance can aid for easy deployment in IoT and M2M applications. The prototype has been tested by generating various frequencies ranging from 1 KHz to 120 MHz, which resulted in similar performance as discussed above.

IV. Conclusion

In this paper we proposed a low complex mixer less QPSK based transmitter architecture using BJTs as primary elements in the analog bank which can greatly aid for IoT and M2M applications where the less design complexity is an important aspect. The architecture can also be developed using the MOSFET technology, with minor changes in the functional units of the architecture. A hardware prototype for the architecture proposed is developed in IIT Hyderabad and the generated modulated signal at a center frequency of 205.8 KHz has been

Fig. 9: Modulated signal acquired from the analog bank of the developed hardware prototype at IIT Hyderabad

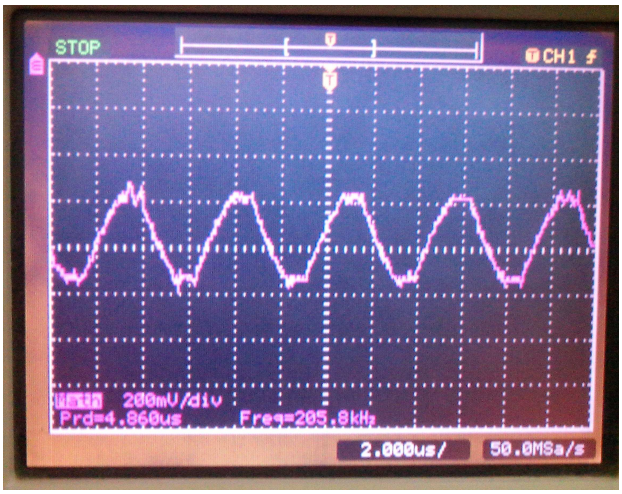

Fig. 10: Modulated signal generated from the developed hardware prototype at IIT Hyderabad after low pass filter

analyzed. The quality of the modulated signal mainly depends on the quality of the signal generated by the memory unit. Lesser the distortion at the output of the memory unit, greater the quality of the modulated signal. The prototype developed is of low complex due to the elimination of mixers in the design. The other advantages of the proposed architecture are the ease of integration between digital functional units and the simple analog bank. In addition to limit bandwidth by any means of pulse shaping techniques, the same architecture proposed can be used in cascade with an analog pulse shaping filter. The prototype developed at IIT Hyderabad has been successfully tested for generation of various frequencies ranging from 1 KHz to 120 MHz. With the enhancement of technology, even higher frequencies upto GHz range can be generated.

Acknowledgment

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