Integrated 16-channel Transmit and Receive Beamforming ASIC for Ultrasound Imaging

Chandrashekar Dusa, Samiyuktha Kalalii, P. Rajalakshmi, Omkeshwar Rao
Department of Electrical Engineering
Indian Institute of Technology Hyderabad, India
Email: {ee12m1014, samiyuktha, raji, omkesh}@iith.ac.in

***Abstract*— In commercial ultrasound systems, the multi-element transducer array is connected to analog front end electronics using long-wire high voltage coaxial cables. This paper presents the circuit design of 16-channel Transmit (Tx) and Receive (Rx) beamforming ASIC (Application Specific Integrated Circuit) that can be integrated in ultrasound probe head which reduces the number of coaxial cables. The proposed modular design for programmable 16-channel transmit beamformer operates at medical frequencies in pulse-echo mode and provides user control of transmit parameters such as transmit pulse length, pulse pattern, transmit frequency, and mode of excitation. The receive beamformer implements delay and coherent sum of the digitized echoes from 16 adjacent transducer elements to form scanlines required for image reconstruction. The proposed architecture of the Rx beamformer design provides great flexibility for beamforming, such as receive focusing with predetermined delay profile. Each transmit channel can be programmable to give a maximum delay of 163.85 μs with 1.25 ns delay resolution. The proposed design implements dynamic receive focusing with minimum time delay resolution of 3.125 ns for 40 MHz input data rate. The proposed ASIC of integrated Tx and Rx beamformer is implemented in UMC 130 nm technology using Synopsys ICC and Design Compiler. The implementation reports show that the area is 5.29 mm^2, power dissipation is 38 mW.**

***Index Terms*— Transmit beamforming, Receive beamforming, ASIC implementation, Design compiler, Integrated circuit compiler.**

I. Introduction

Medical diagnostic applications using ultrasound systems are becoming prominent in diagnostic surgeries, investigating cardiovascular diseases in ambulatory and hospital divisions [1]. These applications requires handheld ultrasound scanning systems for instant diagnose of patient conditions which are battery driven and needs low power ASICs for ultrasound imaging. In ultrasound systems the digital beamformer typically generates necessary logic pulses with proper timing and phase to enable electronic steer and focus of the acoustic beam. However, these systems often have "closed" architecture that provides limited access to the researchers to perform digital ultrasound beamforming [2]. Current generation ultrasound systems are using arrays of transducer elements that are connected to front end electronics using long wire coaxial cables [3]. So, we have proposed the architecture for Tx and Rx beamforming ASIC which can be integrated in ultrasound probe head.

In the past, several digital beamformer architectures have been proposed to meet the requirements of high performance ultrasound imaging systems. In [4] authors discussed the evolution and basics of digital beamformers. Hu et al. have presented the design and development of 16 channel digital beamformer for high frequency linear array transducers in [5]. In [3] John et al. have proposed the architecture for 8 channel transmit beamformer ASIC integrated with high voltage pulser. The existing methodologies does not provide much user reconfigurability of the transmit parameters for beamforming and limited for dynamic configuration of number of active channels.

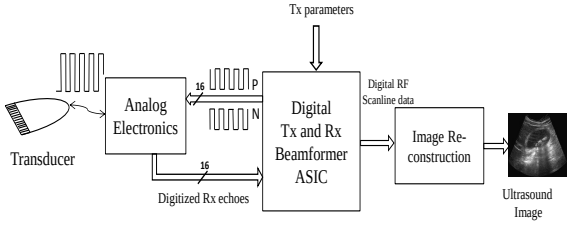

Fig. 1: The ultrasound imaging system architecture with the proposed digital beamformer

In this paper, we have designed the 16-channel Tx and Rx digital beamformer ASIC for ultrasound imaging which can address some of problems above discussed. The ultrasound system architecture with the proposed digital beamformer is shown in Fig. 1. The modular design of Tx beamforming is provided with high speed DDR (Double Data Rate) technology based serial interface to configure the Tx parameters such as transmit frequency, pulse length, number of active channels and mode of excitation. The proposed digital beamformer is having a provision to choose number of active channels which can be used to implement Synthetic Transmit Aperture (STA) [6] beamforming algorithm for ultrasound imaging.

The Rx beamforming architecture acquires digitized echoes of each channel that are delayed for pre-determined delay profile and coherently summed to form digital RF (Radio Frequency) scanline data. The time delays applied

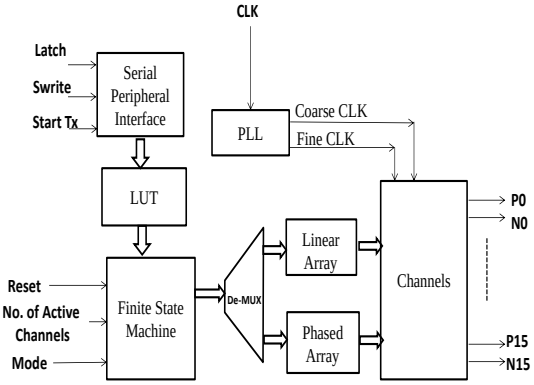

Fig. 2: Architecture of proposed transmit beamforming circuit

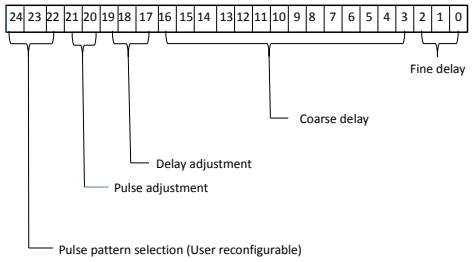

Fig. 3: Bit structure of configurable delay register

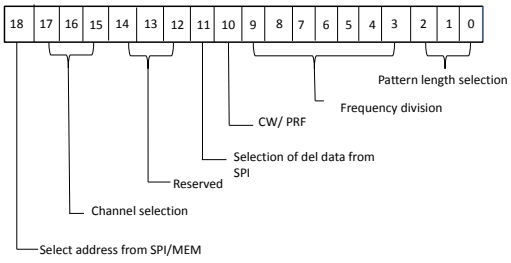

Fig. 4: Bit structure of configurable control register

to real-time echo signal samples as a combination of coarse delay and fine delay. The coarse delay is integer multiples of ADC sampling period and the fine delay is a fractional time delay. The digital RF scanline data is further processed for image reconstruction to acquire ultrasound image of patient tissue. The ASIC for the proposed the design is implemented using UMC 130 nm technology using Synopsys ICC and Design Compiler.

To further discuss, the efficacy of the paper is organized as follows, section II explains the architecture of ultrasound Tx beamforming and simulation results. Section III explains the architecture of ultrasound Rx beamforming and simulation results. Section IV discusses about ASIC implementation of proposed design. Section V concludes the paper.

II. Transmit Beamforming Architecture

The ultrasound imaging involves a typical acoustic beamsteering called as Tx beamforming which can be achieved by applying time delay of excitation to series of transducer elements [7], [8]. The modular design of transmit beamforming architecture is shown in Fig. 2. The proposed modular architecture for complete beamforming process with a reference clock of 20 MHz achieves a minimum delay resolution of 1.25 ns from each individual reconfigurable channels. The Start Tx control signal is used to enable transmit and receive modes of ultrasound sensors. The design has a provision to configure different Tx parameters such as mode of transducer selection, the number of active channels, and a programmable register to choose the transmit parameters such as pulse width adjustment, pulse pattern control, and modes of transmissions like continuous wave and pulse repetition frequency that provides an ease of user accessibility for transmit beamforming.

The complete proposed architecture consists of SPI (Serial Peripheral Interface) module, FSM (Finite State Machine), channel module, LUT (Look Up Table) for storing the delay profile for acoustic beam steering. A high speed DDR technology based SPI is provided which can reduce the time required to configure the internal registers and programme data into LUT. A combination of coarse and fine delay strategy is implemented through a 17 bit programmable counter for time delay generation. Fig. 3 shows the bit structure of the configurable delay profile register in which starting from LSB delay [2:0] are used for fine delay count, delay [16:3] are used for coarse delay count. A maximum time delay of 163.85 μs is achieved by programming the delay register. Here fine delay is used to obtain the fractional phase delay in increments of $(1/8)^{th}$ of the coarse clock time period. The coarse delay (100 MHz) and fine delay (800 MHz) source clocks are generated using PLL (Phase Locked Loop).

The Tx beamforming design is provided with a 19-bit control register to control the modes of operation such as like Pulse Repetition Frequency (PRF) and Continuous Wave (CW) mode. Fig. 4 shows the bit structure of the control register which can be configured depending on the application. The first three bits Control[2:0] represents the transmit pulse pattern length selection i.e., number of pulse bits to be transmitted. Bits Control[9:3] are to dynamically change the frequency of the pulse pattern. Control[10] bit is to choose the mode of operation like pulse-echo and doppler

mode. Control[11] and Control[18] are configured to access data through SPI or LUT memory block, wherein $12^{th} - 14^{th}$ bits are "reserved" for future purpose. Control[17:15] is to select the number of active channels to be configured. For B-mode imaging, the delay profiles required for beamsteering in the field of view from -90° to $+90^\circ$ are programmed into the LUT through SPI which can be configured by the Control[18] and Control[11] bits of register.

A. Serial Peripheral Interface (SPI)

SPI module in the design controls the transmit pulse patterns and delay profile settings that are programmed in and read out through each individual channel. UART (Universal asynchronous receiver/transmitter) controller is also been programmed for establishing serial communication to the SPI from the external environment. Upon receiving serial input through SWR (Serial Write), SPI generates a five bit address, one write/read signal, twenty five bit delay register and a nineteen bit control register. With reference to the address generated, corresponding data is accumulated into the internal registers only when SLE (Serial Latch Enable) and Start Tx control signals are active low. Fig. 5 shows internal architecture for SPI module with DDR technology. The serial data is routed to individual channels with the help of controller upon programming the control register bits.

B. Finite State Machine (FSM)

The FSM is incorporated to configure different modules depending on the application that can suitable for both phased array and linear array beamforming. It provides a wide range of options to select the number of channels and the type of transducer beamforming. Fig. 6 shows the state machine chart of the controller module. From the state machine chart we can infer that upon reset at active high, the system remains in IDLE STATE. System enters into the CHANNEL STATE when the address is between 1 to 16. Once after write (W/R) operation is completed, system again reaches to IDLE STATE. If the address increments to 17, the system will be in CONTROL STATE and retains IDLE STATE once WR operation is over. When the system is in CHANNEL STATE, it first checks the operation to be performed by the user with the help of SWR control signal. If it is "Write" operation, the controller enables all the channels to trigger out the pulses with delay profiles. And when the status is "READ" mode, data is serially loaded from SPI.

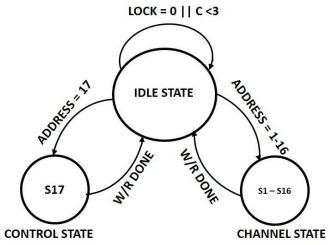

Fig. 6: State Diagram of FSM

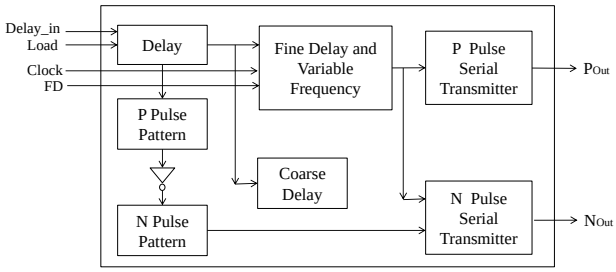

Fig. 7: Internal Architecture for channels

C. Channel module

Each individual 16 channels consists of a separate Delay counter, P-pulse and N-pulse registers. The 25 bit data register can be accessed by programming through SPI. Delay[24:22] bits are for selecting pulse pattern, Delay[21:20] bits are for pulse adjustment, Delay[19:17] are for adjusting the delay width. The remaining 17 bits are

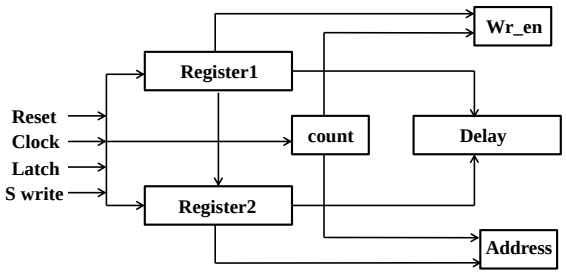

Fig. 5: Architecture of high speed serial interface (DDR-SPI)

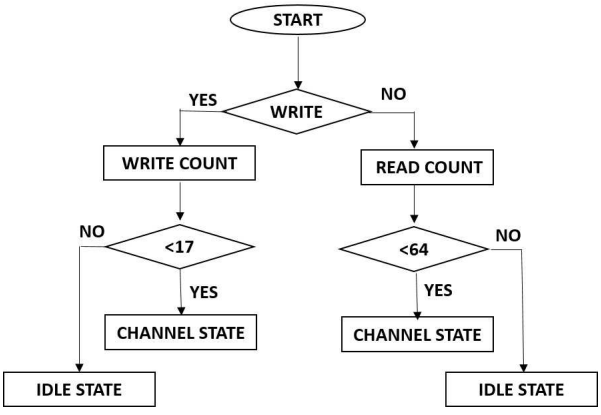

Fig. 8: Flow Chart for accessing channels

used to assign coarse and fine delays.

For generating the transmit pulses through each channel, the delay data has to be configured for coarse delays and fine delays. In the proposed design a 17 bit programmable register is used to account for the coarse and fine delays. A coarse clock with a frequency of 100 MHz is used for accounting the coarse delays and a fine clock of 800 MHz is used to generate fine delays. For accurate timing control of the pulses from each channel, fine clock is chosen as $(1/8)^{th}$ of the coarse clock. Upon configuring pulse pattern register each P and N pulse channels are programmed with a 64 bit data automatically. Once the complete cycle of coarse and fine delays are completed, SLE and Start Tx are triggered high for firing the pulse bursts from each individual channels.

Fig. 7 represents the internal architecture designed for pulse generation from P and N individual channels. Fig. 8 shows the flow chart of channel configuration. From the flow chart, we can observe that whenever the system is in channel state, it first checks the operation to be performed by the user with the help of W/R signal. If it is "Write" operation, the controller loads the data from the SPI to the designated channels. Fig. 9 shows the simulation results of proposed Tx beamforming design for two individual channel outputs which are time delayed by 4-coarse delays and 2-fine-delays.

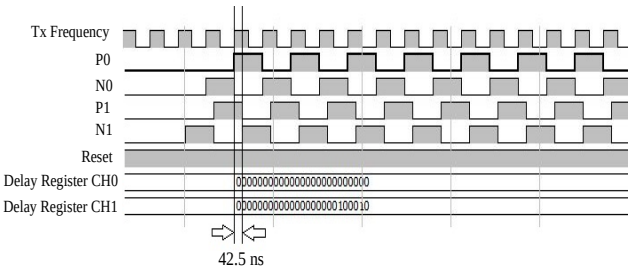

Fig. 9: Simulation result of Tx beamforming design.

III. Receive Beamforming Architecture

The digital receive beamforming is essential for attaining good image quality by increasing signal-to-noise ratio (SNR), improving spatial resolution and reducing sidelobe artifacts [9]. The received echoes of each transducer elements are connected to ADC (Analog to Digital Converter) after signal conditioning further the digitized echo signal is time delayed by predetermined delay profile and coherently summed to form RF scanline data. The RF scanline data is then processed for image reconstruction to acquire ultrasound image. Fig. 10 shows the simple geometry of transducer elements and field of view to the focal point [10]. The delay profile for each transmission to perform dynamic receive focus is obtained from equations (1), (2) for transducer physical parameters which are stored as LUT in the design. Average ultrasound velocity (c) in tissue is considered as 1540 m/s.

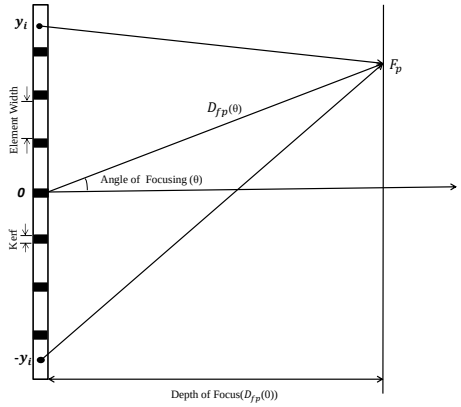

Fig. 10: Calculations of delay profile for a focusing angle (θ°)

$$t_i = \frac{\sqrt{D_{fp(\theta)}^2 + y_i^2 - 2y_i D_{fp(\theta)} sin(\theta)}}{c} \quad (1)$$

where $D_{fp(\theta)} = \frac{D_{fp(0)}}{cos(\theta)}$

$$T_i = t_{max} - t_i \quad (2)$$

$F_p \rightarrow$ Focal point.

$D_{fp(\theta)}, R_{fp(0)} \rightarrow$ Distance from center element to point F_p.

$t_i \rightarrow$ Time required for wave front to reach point F_p.

$y_i \rightarrow$ Co-ordinate of i^{th} element.

$t_{max} \rightarrow$ Max time required for wave front to reach point F_p.

$T_i \rightarrow$ Delay for i^{th} element.

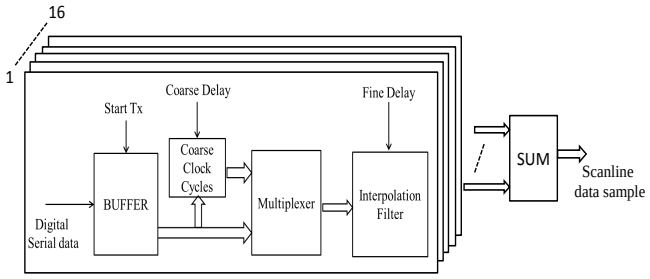

Fig. 11: Modular architecture for proposed Rx beamforming

Fig. 11 illustrates the proposed modular architecture for receive beamforming. The design buffers real-time digitized echo samples per each channel from analog electronics at a rate of ADC sampling frequency (40 MHz). The delays are applied to the real-time echo samples in terms of coarse

delay and fine delay. The coarse delays are integer multiples of the clock periods and the fine delays are applied with a interpolation filter [11]. The dynamic receive focusing is implemented based on state machine which updates delay values and the interpolation filter coefficients according to the steering angle of acoustic beam. The scanline data which is fed to image reconstruction can be obtained by coherent sum of delayed echo samples of each channel.

The modular design buffers the echo signal samples in receiving mode, which is controlled by Start Tx control signal. The coarse delay applied in terms of integer multiples of ADC sampling period (0.25 μs) and an interpolation filter is implemented by a factor of 8, which enables a minimum fractional delay of $(1/8)^{th}$ of the ADC sampling period (3.125 ns). Fig. 12 shows the simulation result of Rx beamforming design for four individual channels. The input data samples are fed at a rate of 40 MHz which is latched for every rising edge of the clock. The input data is delayed by number of samples according respective delays and summed to form RF scanline data samples.

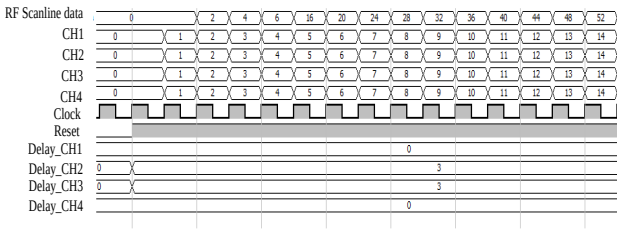

Fig. 12: Simulation result of Rx beamforming design.

IV. ASIC Implementation

Area, power dissipation and speed are the most important factors when it comes to implementation of high end systems in VLSI domain [13]. The integrated design of 16-channel Tx and Rx beamformer has been simulated using Synopsys VCS (Verilog Compiler Simulator), synthesized using DC (Design Compiler) and implemented the complete physical design using ICC (Integrated Circuit Compiler). Fig. 13 shows the Gate level simulation (GLS) obtained for the proposed architecture. Here the two individual channel logic outputs of Tx beamformer are simulated according to the delay profile programmed in delay registers. The ASIC implementation of the design is carried out in UMC 130 nm 3.3/1.2V 8 metal layer CMOS process technology and fabricated as DIL-16 (Dual in-line package). An area of about 5.29 mm^2, 292 K equivalent gates dissipates 38 mW (from 1.2V) while operating at 20 MHz. TABLE I shows the chip characteristics of the proposed design. Fig. 14 is the final layout of the integrated 16-channel Tx and Rx beamformer.

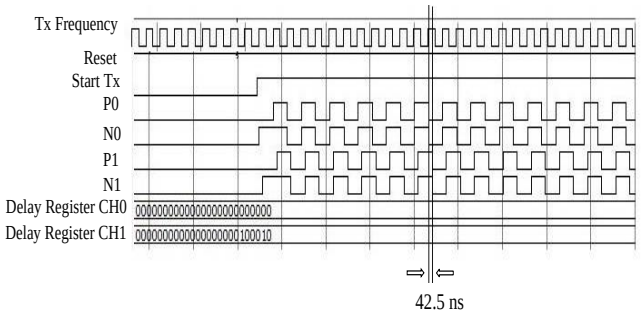

Fig. 13: Gate level simulation results in Design Compiler.

TABLE I: Chip characteristics

Technology	UMC 130 nm 3.3/1.2V
Area of chip	5.29 mm^2
Reference Frequency	20 MHz
Power dissipation	38 mW
Number of logic gates	292K
Package	DIL 16

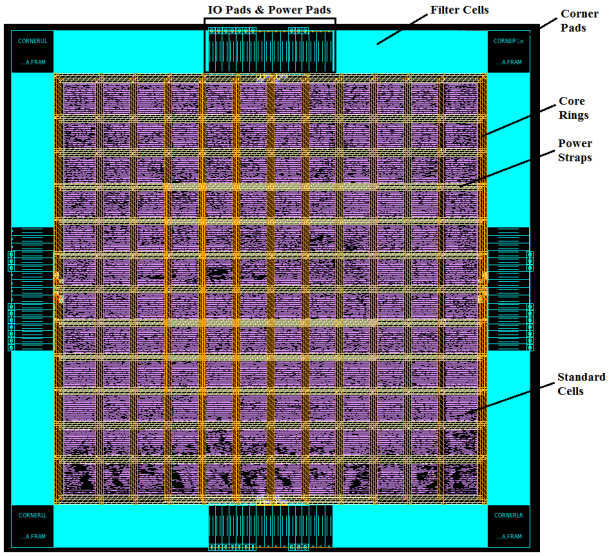

Fig. 14: Layout of ASIC of proposed architecture for integrated Tx and Rx beamformer.

V. Conclusion

We have designed the integrated 16-channel Tx and Rx beamforming ASIC for portable ultrasound imaging. From the results we can infer that the design achieves a relative timing difference between two individual channels with a

minimum delay resolution of 1.25 ns and maximum of 163.85 μs for Tx beamforming. While the dynamic receive focusing with the smallest time delay resolution of 3.125 ns for the 40 MHz echo signal samples. The fabricated chip for the proposed design with area 5.29 mm^2, 292 K equivalent logic gates dissipates 38 mW (from 1.2V) while operating at 20 MHz which accomplishes the design suitable for portable ultrasound imaging systems.

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