Platform Independent, Illumination aware Reconfigurable Switch Capacitor based 3.3 Volt Energy Harvester IC

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Dedication

To Humanity, Late Father Shri Sunil Kumar Ji Joshi &

Great Grandpa Late Shri Madan Lal Ji Joshi

Abstract

This dissertation presents a platform independent illumination aware fully on chip microscale energy harvester for powering 3.3V sensor nodes and smart IOT devices. The programmable switched capacitor DC-DC converter for fully on chip applications is discussed and implemented. The reconfigurability assist the converter to provide 3.3V regulated output with high efficiencies of upto 84% for wide range of inputs lying between 0.4 to 1.8V. A nano-watt illumination sensing unit is used to automatically sense the input voltage and programme the step up ratio of the converter. For SC converters the key power consuming assist circuit is the clock generator. Thus, we operate the clock generator at lower voltage of 1.8V which significantly reduces the power invested in MPP tracking. To squeeze maximum power from PV cell, a novel platform independent, power head adjustable, fractional open circuit MPPT technique is proposed and discussed along with existing techniques. The proposed MPPT circuit improvises the VCO based feed forward technique using error correction feedback mechanism. In virtue of the self correcting feedback, operation of the proposed technique is insensitive to solar characteristics, converter topology and semiconductor process variations. Operating frequency of clock generator is the controlling parameter for the fraction of power invested in maximum power point tracking. This technique enhances the harvested energy by adaptive frequency and power adjustment of the clock generator depending on incident illumination. Verilog A model of PV cell is used to replicate a three PV cell array. Verification of accuracy of MPP tracker is done against variation in PV cell characteristics, semiconductor process parameters and various converter topologies. Post layout simulations indicate the error lying within 3%. A start up circuit is used to trigger the energy scavenging from totally drained out condition of zero battery voltage and 200mV input. To increase the lifetime of the battery we use a state of art low power battery protection circuit which protects the battery voltage from going out of safe voltage range i.e. 2.2 to 3.4V .A 50 μf capacitor is used to simulate the battery. The system is designed using UMC 0.18 μm process and post layout simulations are presented. The harvester interface occupies 65μmX65μm of space on die and is suitable for wearable and compact biomedical applications.

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Chapter 1

System and design Aspects

1.1 Introduction

Exponential increase in the level of logic and circuit integration on silicon has led to an ecosystem of devices where humans and machines are surrounded by sensors and tiny computers. The technological advancement has exchanged the roles of humans and computers . Instead of computers surrounded and guided by humans the present day computers are computationally and footprint wise capable of assisting humans. The present as well as the coming era projects a lot of advancements in tiny intelligent devices . Such devices constitute to an ecosystem known as internet of things(IOT) [1]. Apart from these recent class of devices the definition of such devices are also applicable on wireless sensor nodes [2] which became a topic of interest for the very first time in late 90s . Increase in possible micro and nano-scale integration has led to enormous research on such devices. However, the intensity of computation as well as the performance both are limited by the power consumption [3]. Systems like miniaturized smart health care devices , industrial smart sensors, smart dust sensors are typical examples where energy requirement is not only localized to each node separately but also represents the reliability of such systems. Due to remote locations, continuous operation for months and a swarm of sensors incorporated, regular battery replacement in such system is extremely expensive and hence limits the amount of sensors and processed data which can be used in particular application. Micro scale energy harvesting from surrounding ambient such as solar , thermal, vibrational and rf sources is emerging as a promising solution to replace the battery as the primary source of power [4]. Several works on energy harvesting has been published recently [5–8] introducing the typical architecture of a energy scavenger. These systems consist of

multiple energy sources (similar or dissimilar) followed by a scavenging circuit (consist of converter, Maximum Power Point Tracking , Power management). The type of source and harvester is chosen on basis of application and surrounding ambience.

In addition to the aforementioned platforms there is lot of space for advancements in such systems. Few of them with respect to PV cell energy harvesting will be discussed in this chapter as well as in entire thesis. Increasing attraction towards System on chip (SOC) [9] integration has also set the constraints for energy harvesting systems to be as monolithic as possible. Also for the energy harvesting systems to succeed in present day computationally intensive and tiny sized sensor nodes the harvester unit must adapt to the conditions in which they operate. This demands for a illumination aware scavenger which must be capable of optimizing its performance depending on surrounding conditions. Considering the market of energy transducers and its future expansion we must also focus on systems which are built independent of traducers (PV cells).
In this thesis we discuss these design issues and propose solutions with respect to PV cell energy harvesting. In this work we center these issues and around a Platform independent, illumination aware 3.3V Fully on chip energy harvester for micro scale energy harvesting .

1.2 3.3 Volt design importance

Output voltage ranges for some typically used device loads such as sensors,SOC, wireless sensor nodes range around 1.8-3.3V. Also ZigBee sensor nodes [10–12] have recently became a topic of intrest due to their lower power consupmtion compared to other protocols. These WSN generally operate around 3.3 V. This is a motivating fact behind recent energy scavenging works around this voltage range. Each sensor node has analog and digital subsystems . Scaling of supply voltages for analog subsystems like AFE and RF chain are not as straightforward as that of digital signal processing sections of design. In high reliability applications such as ECG transmission and industrial sensors placed at hazardous locations the designer has small margin of performance to trade off. In addition to the supply voltage, power required by RF chain is also a matter of concern. Where the transmitted power directly controls the maximum possible distance between two sensor nodes. This leads to a demand for 3.3V scavenging systems which can work for wide range of conditions. In subsequent sections we intend to introduce one of the same kind.

1.3 Fully-on-chip

One very key feature of a energy harvesting system is its footprint. The scavenging system is intended to harvest energy and not to process data. Hence minimum possible fraction of sensor area must be occupied by scavenger. Inductor based buck, boost and buck-boost converters are very popular due to simple architectures and high efficiency operation. However, these are not suitable for monolithic integration because the inductor values involved in efficient boost operation are high, leading to an off chip inductor. Moreover, in applications like biomedical implants such as [13] where the area of the implant play a huge role in its realization . For a artificial retinal implant like [14] the self powered version cannot consist of a off chip inductor. As the industry pushes towards system on a chip (SOC) solutions, many different circuit functions have already been integrated onto a single die and the power converters occupy an increasing proportion of printed circuit board (PCB) area. In contrast to the boost converter, a Switched Capacitor (SC) DC-DC converter [15–18] requires only capacitors, which have a significantly higher power density and can be integrated more easily than inductors. Given an area of $1mm^2$ in today's CMOS technology, a capacitance of about 10nF can be obtained to achieve an energy density of 5nJ at 1V of operation. On the other hand in order to integrate a planar spiral inductor on chip we may need to sacrifice efficiency by upto 35% as compared to a off chip case [19]. However, SC converters comes apart with several design challenges specifically when the major focus is on area and power throughput in parallel. Design of SC-DC DC converters is based on area-efficiency trade off. A larger stage capacitance leads to better power throughput. However, a large value of capacitance results into occupation of larger area. Thus, proper optimization of pumping capacitors has to be done during design. One such modelling of this trade-off was done in [20] . With scaling technologies it has became possible to integrate capacitors in lesser areas and come up with better converter efficiencies. Some recent works [21–24] on 3.3V fully switched capacitor converters have achieved efficiency upto 88% which is competent to the some novel works on inductive scavenging platforms [5,25]. This motivates us to explore more on switched capacitor(SC) based energy scavenging and incorporate a SC DC-DC converter in our design which would be discussed in subsequent chapters.

1.4 Illumination aware harvester

The key concern while planning the architecture of an energy harvester interface is its performance under wide range of surrounding conditions. Considering the kind of operation a energy scavenger

is having we cannot characterize and design it for some pre specified set of illumination ranges. Instead for sensor nodes and biomedical application one would expect not only the sensors but also the harvester to respond and adopt to operating conditions. Consider a self sufficient harvester interface designed for biomedical implants in such cases the harvester must operate in outdoor as well as low indoor light intensity. Performance of switch capacitor DC-DC converter is very sensitive to the illumination or the input voltage which is applied to it [23] . The key design parameters while choosing SC converter are stage capacitance C and step up ratio N. The former is chosen on basis of power throughput while later is chosen on basis of range of voltage levels one need to work with. However, such design approach results in a dedicated converter design optimized for small range of illuminations. Thus the converter topology and no of stages must be configured as per the intensity to which converter is subjected . We would be discussing one such converter topology incorporated in this work in subsequent chapters.

Apart from efficient scavenging one expects a harvester to be self sufficient i.e., the control blocks intended to operate the system must run from a fraction of harvested power itself. Considering a fixed power head of control circuits, for very low illuminations the system will invest a large fraction of harvested power in maintaining itself and thus the effective harvested power will be very less. Thus, the power in control units of energy harvesting systems must be adjustable with incident illumination. In most of the cases the key investment of power is in maximum power point (MPP) operation. This is because a MPPT unit is active continuously for long run. Also the operating frequency of SC converter is decided by MPP unit which also decides the operating frequency of crucial power consumers like clock drivers of converter. Thus the frequency of the source clock generator must be adjusted as per incident illumination for optimal and reliable operation. In this work we turn up with a illumination aware MPP tracker for SC energy harvesting.

1.5 Platform independent

Apart from being aware of surrounding conditions a energy harvesting system must be adjustable to the change in characteristics of transducer. Specifically for PV cell based energy harvesting the MPP operation which ensures the maximum power squeeze from a PV cell at given intensity and is very crucial concerning the throughput at output. The MPP operation has to be insensitive to PV cell characteristics and converter topology and this has been well achieved in complex MPPT techniques such as hill climbing or perturb and observe methods [26]. However, the complexity and power head involved in these methods may incur a large budget for micro scale harvesters. For this

it is feasible to apply a simpler fractional open circuit [15] method at the PV cell- converter interface. A little deviation in PV cell parameters can deviate the system from MPP points these changes can be due to ageing and operating conditions. In addition to this PV cell vendors are market players, varying in terms of size, doping , material etc. Thus, a MPP dedicated to a particular PV cell would bound user to use a particular PV cell only. Also the semiconductor process variations would lead to failure of MPP tracking in many cases. In our research where we aim to operate with wide range of converter topologies the insensitivity of MPP operation to converter architecture (i.e. topology, no of stages) is also a matter of concern. Thus, in this work the key motivation is to propose a MPP tracker which is platform independent or in other words, self correcting to such variations. Chapter 3 discusses a novel pilot cell less and low power head MPP tracker for micro scale energy harvesting.

1.6 Literature survey

The literature survey of recent novel works on energy harvesting for self powered 1.8-3.3 V applications are shown in Table 1.1. This review motivates us to come up with a fully on chip SC harvester in this voltage range with a battery protection.

Table 1.1: Comparison of proposed harvester with previous literatures

Feature	[22]	[25]	[23]	[5]	[7]
Technology	AMS 350nm	350nm	130nm	350nm	NA
Function for battery	SC Harvester	Inductive Harvester	SC Harvester	Inductive Harvester	Inductive Harvester+ Battery protection
Battery Protection	No	No	No	No	Yes
Self sustaining & Fully in chip	No, Yes	Yes,No	Yes, Yes	Yes,No	Yes, No

1.7 Full scheme and thesis organization

The functional diagram at higher abstraction level of the proposed system is shown in Fig. 1.1. The system consist a illumination aware SC DC-DC converter. An topology similar to [27] is used. In Chapter 2 utility of this converter architecture is discussed for wide range of input (0-1.8) and high output voltages (3.3V). The sensitivity of SC converters to input voltage is discussed with math-

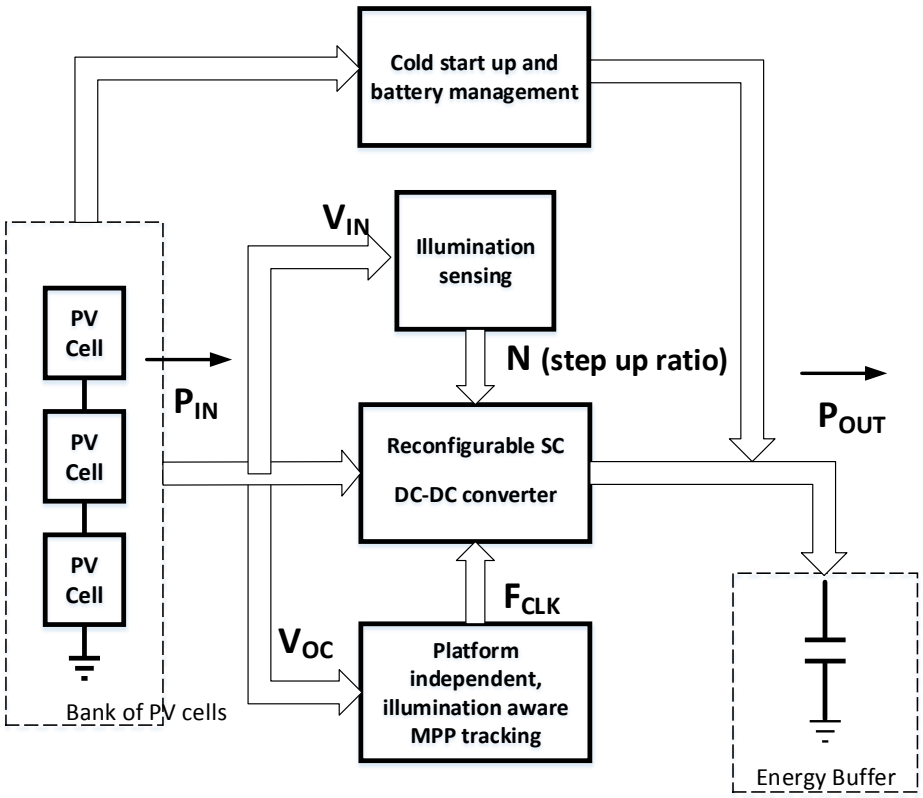


Figure 1.1: Proposed harvester scheme

ematical model. A clock distribution scheme is discussed to reconfigure the converter to various modes.

A platform independent , illumination aware, pilot cell free MPP tracker is dicussed in Chapter 3 with detailed theoretical discussion and its comparison with existing MPP methods is done. In Chapter 4 in the first part we discuss system level operation of harvester and assisting subcircuits like battery management and cold start up. In second part we thoroughly discuss detailed post layout simulations, operating condition and system verifications against various illuminations, process variations, PV cells and converter topologies. Chapter 5 concludes the work along with novelties which can be added in future.

Chapter 2

Reconfigurable illumination aware switched capacitor DC-DC converter

2.1 Motivation

The voltage levels available at output of solar cells are not sufficient to drive self-powered devices or to recharge a battery. Thus, in micro scale energy harvesting systems a DC-DC converter is used to step up the voltage level and bring it in desired range. Also, the amount of solar energy available usually varies with the time and sunlight. Energy available under strong sunlight is high, while it is low under weak sunlight. Thus the output voltage of solar cell varies over a wide range depending upon intensity of light. As discussed in Section 1.3, switched capacitor (SC) DC-DC converter although are amenable to monolithic, on chip integration. Their operation is highly sensitive to the value of input solar intensity . Most SC DC-DC converters operate in a given small range of input voltage. This leads to an unreliable operation when it comes to tackling energy scavenging for crucial systems where supply down can be fatal. To power such system for wide range of input voltages $(0 - 1.8\text{V})$ a dedicated converter with a fixed step up ratio is not suitable . This motivates us to analyze the SC converters across various topologies, step up ratios and thus incorporate a illumination aware converter which has capability to reconfigurable optimally to an dedicated architecture for given intensity. Hence in this chapter we discuss the utility of a reconfigurable switched

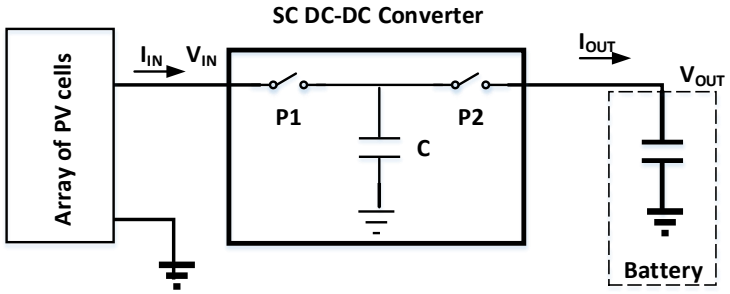


Figure 2.1: Functional diagram of SC DC-DC converter

capacitor DC DC converter.

2.1.1 Performance of SC converters across various step up ratios

The functional block diagram of a switched capacitor converter (charge pump) is as shown in Fig. 2.1. The circuit of a charge pump is characterized in terms of its step up ratio (N) and topology i.e linear, tree ,fibonacci, exponential etc. Analysis and discussion of these charge pump topologies are done in [16,17,28–31]. Before fixing gain and topology of converter one has to characterize its performance across various intensities . The efficiency or the output power at given intensity depends strongly on converter gain N . In this Section we characterize optimal gain ratios of the converter across various input intensities . As per the analysis done in [28] we can easily calculate the power output P_{OUT} for various values of N. The output power expression comes out to be of the form

$$P_{OUT} = \gamma\ CF_{CLK}(V_{IN} - V_{OUT}/N)V_{OUT} \tag{2.1}$$

Here F_{CLK} represents the operating frequency of CP, V_{IN} is the input voltage to converter, C is the stage pumping capacitance and γ is a constant dependent on step up ratio . The expressions are tabulated for various vaules of N in Table 2.1 .

Also, from classic charge pump theory we know that during regulated operation (V_{OUT} regulated to constant voltage) the minimum step up ratio required to boost the input voltage V_{IN} to regulated output voltage (V_{OUT}) is

$$N \geq \frac{V_{OUT}}{V_{IN}} \tag{2.2}$$

Eqn. 2.1, Table 2.1 and Eqn. 2.2 reveals following intresting facts

Table 2.1: P_{OUT} across various step up ratioes N

N	P_{OUT}
2	$7CF_{CLK}(V_{IN} - V_{OUT}/2)V_{OUT}$
3	$\frac{12}{7}CF_{CLK}(V_{IN} - V_{OUT}/3)V_{OUT} \approx 1.714F_{CLK}(V_{IN} - V_{OUT}/3)V_{OUT}$
4	$\frac{3}{4}CF_{CLK}(V_{IN} - V_{OUT}/4)V_{OUT} \approx 0.75F_{CLK}(V_{IN} - V_{OUT}/4)V_{OUT}$
5	$\frac{3}{7}CF_{CLK}(V_{IN} - V_{OUT}/5)V_{OUT} \approx 0.429F_{CLK}(V_{IN} - V_{OUT}/5)V_{OUT}$
6	$\frac{6}{23}CF_{CLK}(V_{IN} - V_{OUT}/6)V_{OUT} \approx 0.26F_{CLK}(V_{IN} - V_{OUT}/6)V_{OUT}$
7	$\frac{3}{16}CF_{CLK}(V_{IN} - V_{OUT}/7)V_{OUT} \approx 0.188F_{CLK}(V_{IN} - V_{OUT}/7)V_{OUT}$
8	$\frac{1}{7}CF_{CLK}(V_{IN} - V_{OUT}/8)V_{OUT} \approx 0.143F_{CLK}(V_{IN} - V_{OUT}/8)V_{OUT}$

- As we go on choosing a converter with higher gain, γ decreases. This implies that the output power of converter decreases with increase in N at an arbitrary input voltage V_{IN}. At very high step up ratios the gain severely decreases and converter becomes non functional
- There is a minimum required step ratio for a range of input voltages below which converter is unable to boost the input voltage to an regulated voltage (V_{OUT}) at the output.

Hence there exist an optimal N for which the output power is maximized at given intensity . In other words, for each N there exist a input voltage at which the output power is maximized.

2.2 Literature review: Table

Table 2.2: overview of charge pumps used for energy harvesting

Architecture	Technology	Peak Efficiency	V_{IN}	V_{OUT}	P_{OUT}
Nested 3X Charge pump [21]	CMOS 180nm	88%	1-1.5 V	3-3.5V	0-29μW
Charge pump,based [22]	AMS 350nm	NA	2.1-3.5 V	3.6-4.4V	100-775 μW
Tree Charge pump	IBM 65nm	20% Improvement over conventional Lin CP	0-.4V	1V	190-681μW
This Work	CMOS 180nm	86%	.45-1.8V	3.3V	12-681μW

Although inductive converters has been favourites for years. increasing interest towards SOC integration is drawing attention of researchers towards SC DC-DC converters. Few novel works exclusively done on SC energy harvesting are listed in Table 2.2. The previous research reveals

that there is a strong need of converter architectures meant to regulate loads at 3.3 V. However as discussed, the challenge lies in extracting considerable amount of power for wide range of voltage . Our comparison with the listed literature depicts that we not only achieve peak efficiency comparable to the discussed converter architectures but also are able to extract it for wider range of input voltages.

2.3 Illumination aware Scheme with circuit Diagrams and Device dimension

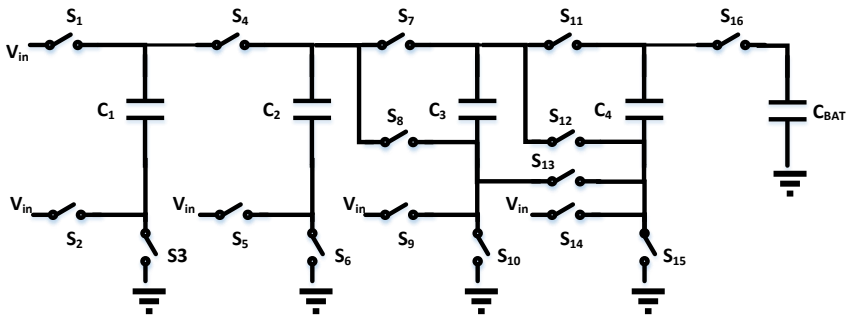


Figure 2.2: Programmable gain SC DC-DC converter

Considering the analysis in previous section we design a illumination aware reconfigurable DC-DC converter discussed in [32] considering 3.3V design in our case. The circuit is shown in Fig.2.2. The step up ratio of converter is programmable across ($N = 2-8$) using a variable clock distribution scheme. The control signal of each switch is indicated as S_i, where each switch can be controlled to four states i.e S_i: 'always on' ,'always off' 'clock phase 1 'clock phase 2' which are indicated by '$\surd$', 'X', 'ϕ_1 ,ϕ_2 respectively. Where 'ϕ_1' and 'ϕ_2' are non overlapping clock phases. The switches are implemented using CMOS pass transistor switches to tackle wide range of input voltage required in our design. To enhance the power handling capability we keep the switch width of 200μm and length tp 0.18μm (minimum length given in a technology can be chosen for other process node). The flying capacitors were implemented using MOSCAPs to accommodate the converter in given silicon space. Values of these capacitors were chosen to be 500 pf each. The clock distribution is handled by pass transistor multiplexers with switches sized equal to that of the converter switches. Table 2.3 shows the required clock distribution to each switch for various desired step up ratios.

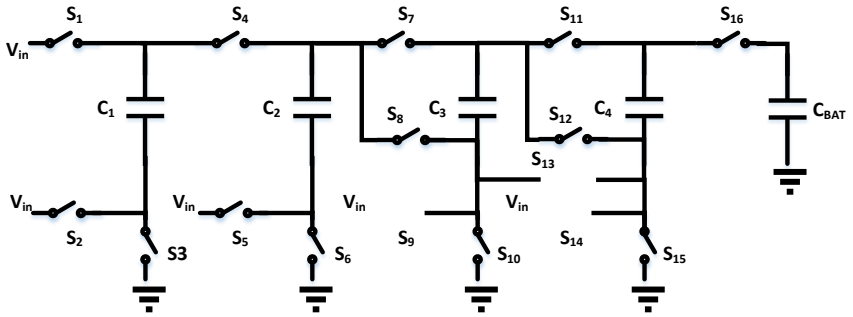
Table 2.3: Clock distribution scheme to programme the step up ratio of converter shown in Fig. 2.2

N	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	S_{13}	S_{14}	S_{15}	S_{16}
2	ϕ_1	ϕ_2	ϕ_1	$\surd$	ϕ_2	ϕ_1	$\surd$	X	ϕ_2	ϕ_1	$\surd$	X	$\surd$	ϕ_2	ϕ_1	ϕ_2
3	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1	ϕ_2	$\surd$	X	X	ϕ_2	$\surd$	X	$\surd$	ϕ_1	ϕ_2	ϕ_1
4	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1	X	ϕ_2	ϕ_1	$\surd$	X	$\surd$	ϕ_2	ϕ_1	ϕ_2
5	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1	ϕ_2	X	ϕ_1	$\surd$	X	$\surd$	X	ϕ_2	ϕ_1
6	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1	ϕ_2	X	ϕ_1	ϕ_2	X	X	ϕ_1	ϕ_1	ϕ_2
7	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1	X	ϕ_2	ϕ_1	ϕ_2	ϕ_1	X	X	ϕ_2	ϕ_1
8	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1	ϕ_2	X	ϕ_1	ϕ_2	ϕ_1	X	X	ϕ_1	ϕ_2

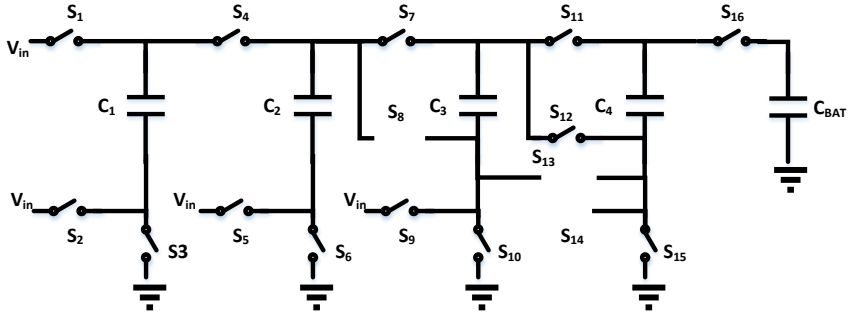
Let us now understand the circuit operation for various step up ratios. Effective converter architecture for a converter gain of of N=8,7,3 are shown in Fig. 2.3 (a),(b),(c) respectively . To achieve $N = 8$ the last two stages of converter are configured to fibonnaci mode i.e. gain of each fibonacci stage is F_{N+2} (where, F_N is N^{th} fibonacci number) S_{12} and S_8 are configured to $\surd$ state while S_9, S_{13} and S_{14} are configured to X state. To achieve $N = 7$ we convert the third stage to linear mode by configuring S_8 to X state. To decrease the N to lower values like 3 we merge various stages in parallel so as to reduce effective no of stages. Various switches and capacitors come in parallel to reduce the no of stages. This is depicted in Fig. 2.3(c).

2.4 Conclusions and Possible improvement

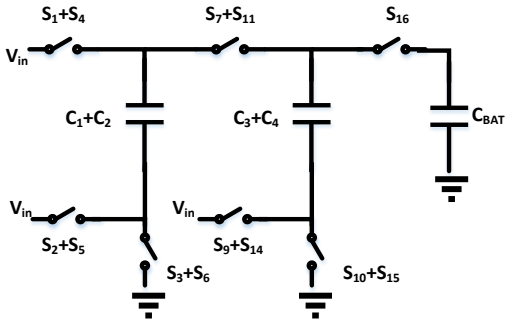
The detailed simulation results of the converter are discussed in Chapter 4. By using aforementioned programmable architecture we were able to achieve a minimum efficiency of 48% to a maximum of 86% in our range of operation i.e. 0.45-1.8V. Hence we were able to perform illumination aware energy scavenging leading to optimized converter operation for wide range of input voltages. Hence leading to a more reliable energy yet fully integrable energy harvesting system. However, some design considerations can be added to make this architecture to increase its utility and that is to extend its operation to an user selected output voltage mode of 1.8/3.3 Volts.



(a) $N = 8$



(b) $N = 7$



(c) $N = 3$

Figure 2.3: Effective converter architecture and switch states for various step up ratioes

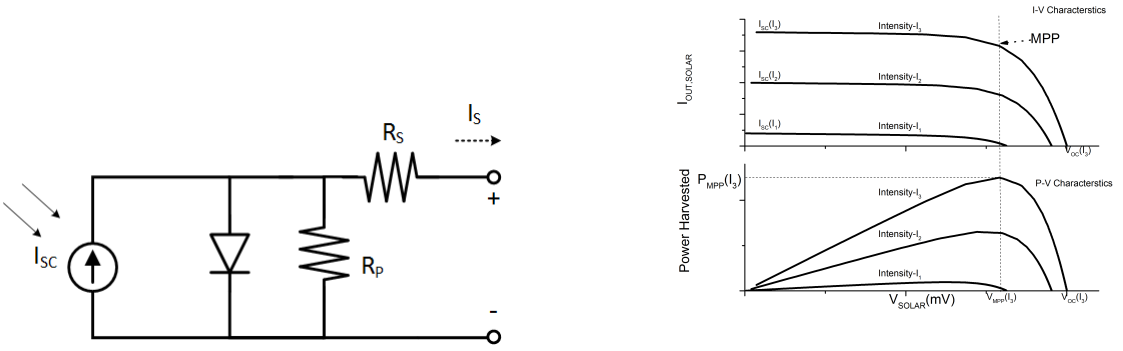
Chapter 3

Platform Independent Maximum power point tracking

3.1 Motivation

In a micro scale energy harvesting systems operating in indoor light condition the output power from PV cell is very small(few hundred μwatts) and thus it is necessary to extract maximum available power from PV cell . An PV cell can be modelled electrically using the model shown in Fig.3.1. Depicted by Fig.3.1(a), at given intensity there exist a effective load impedance (operating point) at output of solar cell at which effective power is maximized. This point of operation is known as Maximum Power Point(MPP) [33] for given solar cell at given intensity. Maximum power point tracking(MPPT) is a technique to maximize the output of PV cell ensuring that the PV cell is optimally loaded and pumps maximum power into the converter. Considering a micro scale fully on chip harvester the charge pump appears directly as a load to the PV cell and hence a MPPT tracker has to direct converter input impedance to MPP.

MPPT methods are broadly classified in two ways, true and approximate MPPT methods [33]. In a true MPP Hill climbing approach power is periodically monitored and an algorithm is implemented using a micro-controller or logic sub block to direct converter input impedance to MPP [26]. Such methods involve complex power hungry current sensors, micro-controllers or logic algorithms and therefore result in a high power head. Thus, these methods are infeasible for single cell applications. Approximate methods are simple and based on the approximation that MPP voltage, V_{MPP} of a PV cell is a fraction k of open circuit voltage of V_{OC}. These approximate methods are majorly divided in



(a) Electrical model of PV cell

(b) Power-Voltage characterstics of PV cell

Figure 3.1: Tracking error across various PV cells and converter topologies

two categories: Pilot cell less methods such as feed forward (FF) MPPT [34, 35] , fractional voltage sampling (FVS) [5] and pilot cell based methods such as fractional open circuit voltage (FOCV) [15], fractional short circuit current (FSSC) MPPT [36]. Feed forward technique eliminates the use of a pilot cell. However, the MPPT operation is sensitive to PV cell characteristics. Thus, this method is ineffective to track changes in characteristics due to solar cell ageing and various PV cell sources. This has been described in detail in section II.

Pilot cell based FOCV [15] and FSSC methods majorly use reference cell with SC converter which increases the size and cost of system such as luminance controlled oscillator (LCO) based MPPT [36], duty cycle based MPPT [37]. Also there may be imperfect matching between the reference pilot cell and that of directed PV cell, thus pilot cell approach is not suited for wearable biomedical applications. Next, in duty cycle based FOC MPP tracking technique irrespective of illumination, clock generator has to operate at a particular frequency ($F_{MPP,max}$) corresponding to highest illumination. Thus, this method fails to adjust the controller frequency with varying illumination. Hence, the extracted power is not optimized. The ineffectiveness of this method has been discussed in detail in section III.

Therefore the FOC sampling - MPPT unit for SC converter has to be platform independent, power head adaptable and must be pilot cell free. In this chapter an error correction based PV cell independent MPP tracking has been proposed. A VCO similar to [34] is used which operates at an optimal clock frequency F_{MPP} irrespective of PV cell characteristics and converter gain N.

3.2 Literature review and artifacts in existing techniques

3.2.1 Feed forward MPP tracking approach

The feed forward MPP tracking unit based on an optimally designed VCO is discussed in [34] and [35] and is shown in Fig. 3.2. As discussed in [34] at the given intensity (V_{OC}), the relation between PV cell output voltage (V_{SOLAR}) and clock frequency (F_{CLK}) of a converter (with step up ratio N) is given by:

$$F_{CLK} = I_{SAT} \frac{\exp\left(\frac{V_{OC}}{\eta V_T}\right) - \exp\left(\frac{V_{SOLAR}}{\eta V_T}\right)}{\left(\frac{N}{N-1}\right)(NV_{SOLAR} - V_{OUT}) + \beta} \tag{3.1}$$

where I_{SAT} is reverse saturation current, V_T is thermal voltage and β is a constant parameter (dependent on charge pump converter losses. From (3.1) it is clear that V_{SOLAR} decreases with frequency (F_{CLK}). As F_{CLK} moves to zero, V_{SOLAR} tends to V_{OC}. Linear approximation of V_{MPP} can be written as :

$$V_{MPP} = \alpha.V_{OC} \tag{3.2}$$

Replacing V_{SOLAR} by V_{MPP} and V_{OC} by $\frac{V_{MPP}}{\alpha}$ in (3.1) and it gives :

$$F_{MPP} = I_{SAT} \frac{\exp\left(\frac{V_{MPP}}{\alpha\eta V_T}\right) - \exp\left(\frac{V_{MPP}}{\eta V_T}\right)}{\left(\frac{N}{N-1}\right)(NV_{SOLAR} - V_{OUT}) + \beta} \tag{3.3}$$

PV cell dependency of feed forward approach

Above equation relates V_{MPP} with corresponding F_{MPP}, the nonlinear relation in (3.3) can be approximated by a standard second order polynomial as:

$$F_{MPP} = af(V_{MPP}) + bf(V_{MPP}^2) \tag{3.4}$$

In feed forward approach [34] the VCO is designed based on (3.4) and in [35] it has been extended to higher order approximation. For a given solar cell-converter interface F_{MPP} at the given intensity is related to V_{MPP} as per (3.3). F_{MPP} has a strong dependency on I_{SAT} which depends on the area, doping concentration and material properties of PV cell. Further F_{MPP} depends on converter gain N (converter topology and stages) and this dependency increases for lower values of N (2-10). Since in [34, 35] MPP VCO described by (3.4) is implemented considering a predefined I_{SAT} and N , hence the feed forward MPP hardware becomes functional only for specified PV cell. This has been illustrated by simulations for two different solar cells, CELL-2, CELL-3 having I_{SAT} values

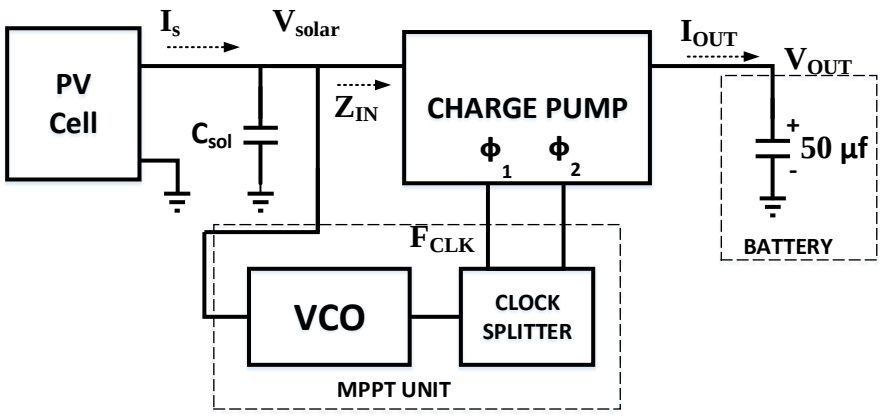
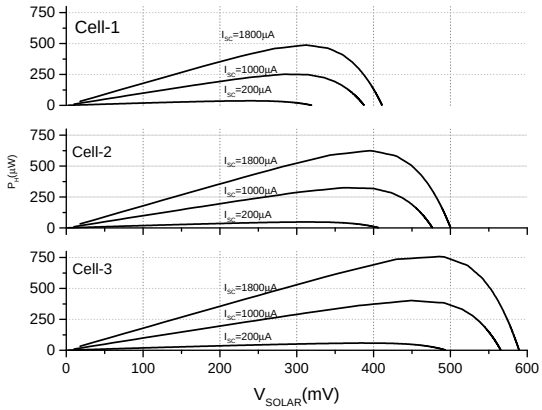


Figure 3.2: Feed Forward MPP unit

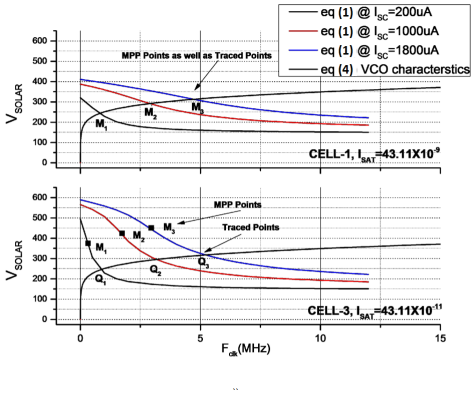
of 43.11 nA, 431 pA respectively. Later in simulation of proposed MPP unit we have extended simulations for error calculations to CELL-1:(I_{SAT}=4.311 nA). P-V characteristics of three different solar cells (CELL-1, CELL-2, CELL-3) are shown in Fig. 3.3(a). MPP VCO has been designed for CELL-2 and a four stage tree charge pump using (3.4) and thereafter as shown in Fig. 3.3(b), for CELL-2 VCO characteristics intersects the converter's voltage-frequency characterstics at MPP points (M_1:240 mV, M_2:290 mV, M_3:310 mV) for various light intensities represented in terms of short circuit current of PV cell (I_{SC}=200, 1000 and 1800 μA respectively). However, when CELL-2 is replaced by CELL-3 the VCO characteristics intersect at points (Q_1:245 mV, Q_2:302 mV, Q_3:330 mV) but actual MPP points for this cell are located at (M_1:380 mV, M_2:425 mV, M_3:450 mV). The traced points for CELL-3 deviate significantly from MPP points, therefore this method is not feasible for other PV cells.

3.3 Duty cycle MPP approach

Duty cycle based MPP tracking scheme proposed in [37] is shown in Fig. 3.4. The two hysteresis comparators compare V_{SOLAR} with $V_{MPP,max}$ and $V_{MPP,min}$ respectively. Both $V_{MPP,max}$ and $V_{MPP,min}$ are obtained from the pilot PV cell. To understand the operation let us first assume V_{SOLAR} tries to exceed $V_{MPP,max}$ in this case the upper comparator produces a logic high while lower comparator produces a logic low. This sets the SR latch and EN signal goes high and connects PV cell to the converter and it draws current from PV cell thus the voltage across input capacitor drops. As V_{SOLAR} drops below $V_{MPP,min}$ the converter is disconnected from PV cell pumping charge into C_s and thus V_{SOLAR} rise. Therefore, in steady state V_{SOLAR} toggles around V_{MPP} in



(a) Power-Voltage characterstics of PV cells under test



(b) Deviation from MPP verified through simulations

Figure 3.3: Tracking error across various PV cells and converter topologies

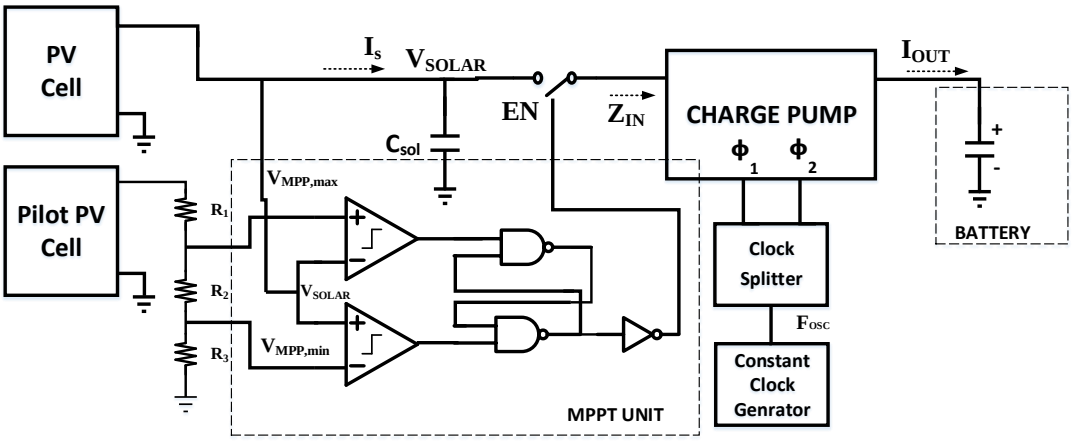


Figure 3.4: Hystresis comparator based Duty cycle MPP tracking unit

a window between $V_{MPP,max}$ and $V_{MPP,min}$ and established the system at MPP. However, clock generator is operating at fixed frequency F_{osc} and the duty ratio (D_{MPP}) of operation of charge pump varies in accordance to the illumination. In steady state the converter operates at effective converter frequency F_{MPP}:

$$F_{MPP} = F_{OSC}.D_{MPP} \tag{3.5}$$

With a duty ratio lying between 0-1, to track MPP for possible range of illumination the clock generator has to operate at highest illumination frequency ($F_{MPP,max}$) . However if solar intensity drops below highest illumination point a clock generator operating at lower clock frequency can also serve the purspose of MPPT . In this method the clock geneator frequency being fixed at $F_{MPP,max}$,

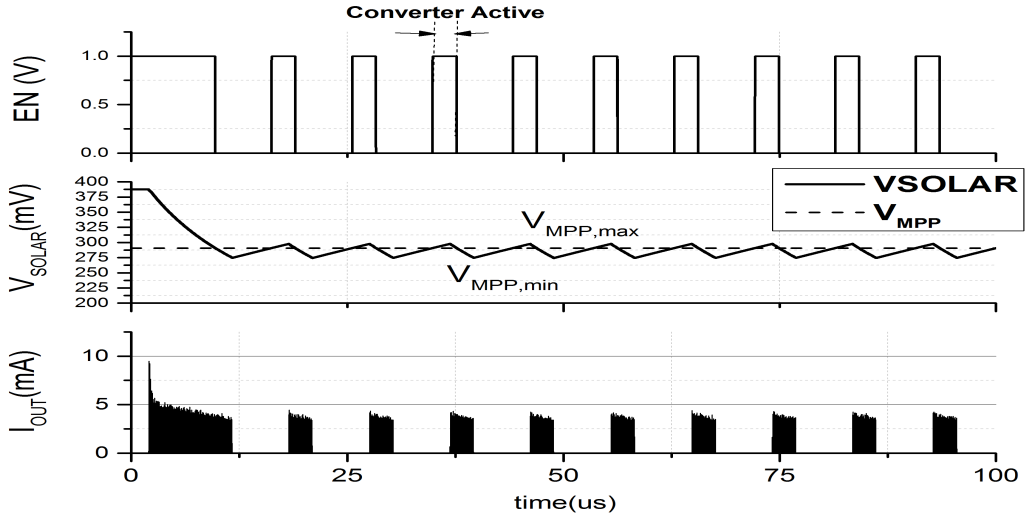


Figure 3.5: Simulations for duty cycle based MPP tracking unit

this method fails to efficiently cater the change in illumination.

A brief review of functional comparison of proposed MPPT with existing MPPT techniques existing in survey is given in Table 3.1

Table 3.1: Functional comparison of various MPP Tracking techniques

MPPT Technique	Pilot cell Free	Platform independent	Illumination aware	low power head
Hill climbing [26, 38]	Yes	Yes	No	No
FOC [15]	No	Yes	Yes	Yes
FSSC [36]	No	No	Yes	Yes
Duty cycle [37]	No	Yes	No	No
Exponential Feed Forward [34, 35]	Yes	No	Yes	Yes
Porposed MPPT Technique	Yes	Yes	Yes	Yes

3.4 Proposed MPP unit

3.4.1 System architecture

Architecture of proposed MPP tracking is as shown in Fig. 3.6. P_1 and P_2 are non overlapping phases. During phase P_1, the converter is disconnected from PV cell by deactivating the clock, hence V_{SOLAR} reaches V_{OC} and value of V_{MPP} (kV_{OC}) is sensed through a resistive divider and sampled on capacitor C_s. During P_2 the clock is supplied to the charge pump and MPP operation

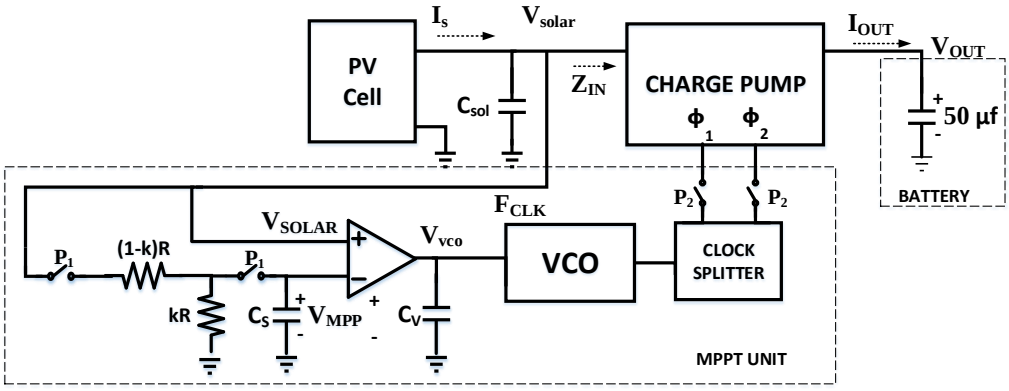


Figure 3.6: Proposed platform independent MPPT unit

takes place. The clock which controls the input impedance of the charge pump is generated by a low power ring VCO. The error between V_{SOLAR} and V_{MPP} is amplified and applied to VCO control voltage, V_{VCO} to adjust the operating frequency of charge pump for MPP operation. In steady state V_{SOLAR} is settled at V_{MPP} and circuit stays at its MPP till next sampling phase P_1 arrives. An off chip capacitor C_{SOL} is connected as an input of converter to reduce the ripples in V_{SOLAR} due to converter switching. The value of this capacitor also decides the MPP settling time (T_{MPP}) and thus we choose value of this capacitor to be 4.7 μf. Duration of phase P_2 is chosen significantly larger than P_1. However, the duration ($T_{sampling}$) of P_1 must be sufficient to charge the sampling capacitor C_S to V_{MPP}. The required VCO in [34, 35] is a non linear VCO so as to meet solar MPP reqirement as explained by Fig.3.3(b), This leads to a higher power consumption than a non linear VCO. Subject to higher loop control and lower power consuption we use a linear VCO explained in Section 4.1.1 .

3.4.2 Platform independent operation

As discussed earlier during P_1 V_{MPP} is sampled on C_S durin/g P_1, at the onset of phase P_2, the voltage on inverting and non-inverting terminal of op amp (error amplifier) are V_{MPP} and V_{SOLAR} respectively. The difference between V_{MPP} and V_{SOLAR} is an error from MPP point and can be expressed as:

$$\epsilon = V_{MPP} - V_{SOLAR} \tag{3.6}$$

So voltage at the output of amplifier (with differential gain A_d) can be written as:

$$V_{VCO} = A_d \epsilon \tag{3.7}$$

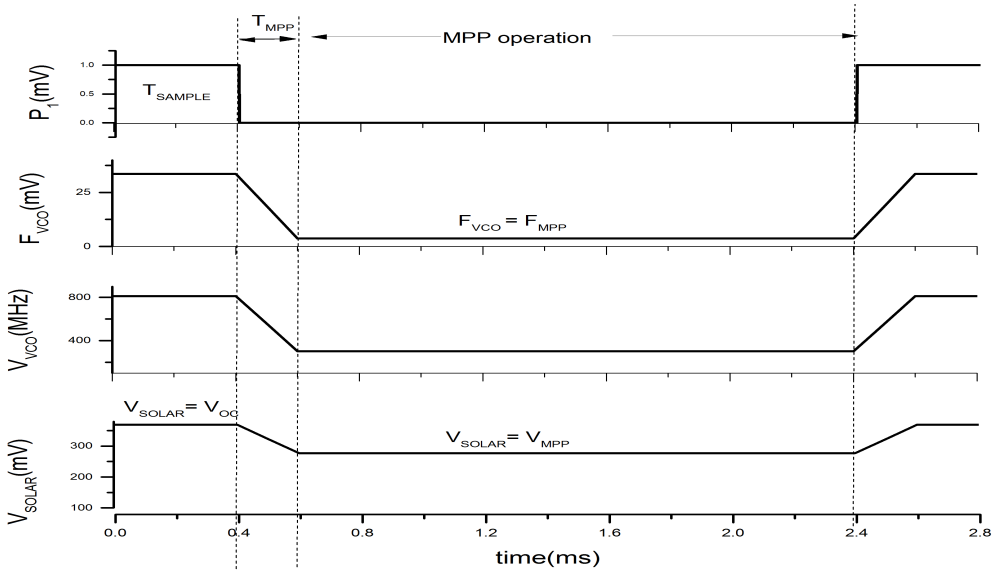


Figure 3.7: Operation of Proposed MPP tracking unit

Assuming VCO to be linear in voltage range of operation with sensitivity K_{VCO}, clock frequency supplied to the charge pump is given by:

$$F_{CLK} = K_{VCO} A_d \epsilon \tag{3.8}$$

As discussed in [36] the DC input impedance Z_{IN}, of a switched capacitor converter is inversely proportional to converter operating frequency F_{clk} :

$$Z_{IN} = \frac{K_i}{F_{CLK}} \tag{3.9}$$

Where K_i is constant dependent on converter total capacitance C_T. From above equation it is clear that the proposed circuit performs a negative feedback based impedance matching between the solar cell and the converter and pulls Z_{IN} to $Z_{IN} = \frac{K_i}{F_{MPP}}$ The operation of MPPT is independent of PV cell property and converter step up ratio. In ideal case A_d is infinite and ϵ approaches zero irrespective of topology. However, if A_d is finite and chosen significantly large the error, ϵ remains very small, irrespective of converter topology, VCO variations and solar cell characteristics. Also, this MPPT technique adjusts clock frequency with varying illuminations (V_{OC}). Therefore, this method is suitable for platform independent low power head applications.

3.5 Conclusions and possible improvements

This chapter demonstrated a platform and process independent, power head adjustable, pilot cell less MPP tracking unit which is independent of PV cells (size, type, etc.) as well as the converter step up ratio (N). The proposed MPP unit is a utility in inductor less single solar cell, charge pump based miniaturized energy scavenging systems, especially for wearable bio-medical applications with reduced form factor. Despite the method being independent on variations in PV cell size, area ,doping the fractional voltage constant α may vary and that has not been considered in aforementioned literatures as well as in this work. However the possible solution of variation in this constant involves a adaptive resistor divider which pre-calibrates its α on basis of PV cell applied. The present technique can also be extended to TEG applications (α close to 0.5) . However, the directed converter input impedance values are very small in such applications and design considerations need to be made for the same.

Chapter 4

3.3 Volt Fully-on-chip Energy Harvester

A reliable energy harvesting system apart from being illumination aware and platform independent must also be intelligent enough to sense and react to energy conditions around it. The control units (drivers, VCO, etc.) live on a fraction of harvested energy itself. To make the system functional these units must be powered not only with low power head but must also be distributed power intelligently. There must be a mechanism to start the system from cold (totally drained out) condition. The energy buffer has to be operated in voltage ranges which are safe and boost its performance lifetime. As this work is focussed on high voltage (3.3V) energy harvesting, we aim to budget the power efficiently among control blocks. In first half of this this chapter we would be discussing all such sub blocks which result in a self sufficient, intelligent energy harvesting system.

The system is thoroughly simulated post layout and details of each block are discussed comprehensively in this chapter. Model of PV cells as described in [33] is used with parameters from data sheet of industry standards [39] .Process simulations are very crucial for MPP tracking unit as a little variation in process parameters leads to a dramatic shift in MPP points. We also simulate a cold start up circuit using a concept of regeneration. Then we discuss simulations of a battery management circuit which operates so as to protect battery from over voltage and under voltage protection. In later sections we present detailed simulation of each sub block and finally compare out work with recent novel architectures.

4.1 Sub blocks description

4.1.1 Harvester interface

The entire interface is shown in Fig. 4.1. The harvester interface in our work consist of converter ,MPPT unit. Moreover, to sense the illumination in order to programme the step up ratio of converter we also require a illumination sensing unit .

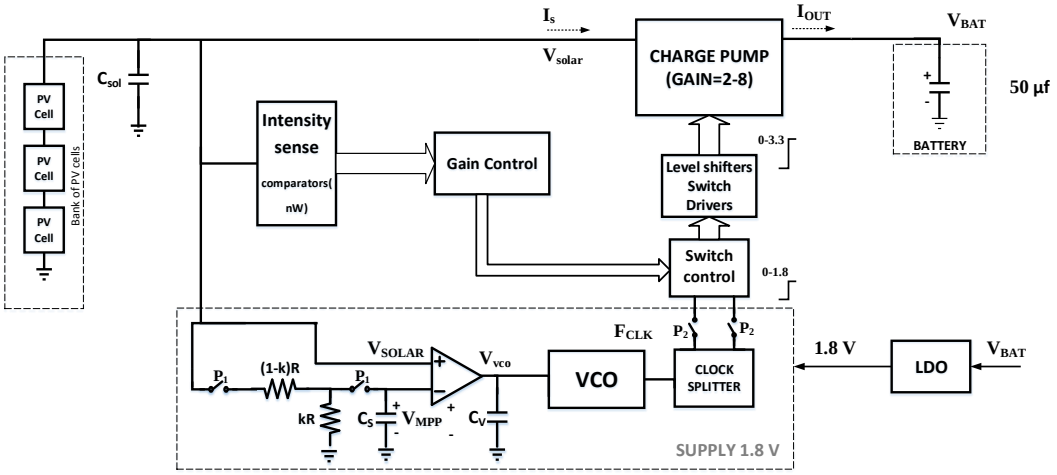


Figure 4.1: Programmable gain SC DC-DC converter

We use array of three PV cells as the natural energy sources which generates a voltage V_{SOLAR} in range of 0-1.8V. The reconfigurable converter discussed in Chapter 3 boost the voltage to 3.3 V at the output (V_{OUT}). To drive the converter efficiently it has to be driven by non overlapping clock signals with clock amplitude of at least 3.3 V. As the switch sizes are huge to handle larger power the load capacitance seen by the clock is high, thus to drive this capacitance we need to place drivers designed to operate with 3.3 V supply this supply is driven from battery itself. However, as the MPPT and clock generation involves a frequency generation it is not to operate them at 3.3V supply . To avoid this we have powered the MPPT control unit using 1.8V regulated supply . The 1.8V supply is maintained using an LDO. After MPP frequency (F_{MPP}) generation at the output of VCO two non overlapping phases of clock are generated using a clock splitter. A level shifter converts amplitude of clock to 3.3V so as to make it suitable to drive switches. The drivers of charge pump are made using 3.3V devices. However they are sized to work also at 1.8V supply at bit lower frequencies ($F_{CLK} \leq$ 5MHz). This separation of power domain saves upto 50% power head involved in clock generation and MPP tracking.

Let us now discuss the operation of reconfigurable converter. The information about light intensity

lies in the open circuit voltage of PV cell this information is used to choose step up ratio and MPP frequency of the harvester interface. To begin with the non ovelapping signals P1 and P2 sample the open circuit voltage V_{OC} of three PV cells i.e $3.\alpha.V_{OC}$ on a sampling capacitor C_s. This value is used to sense intensity using a array of nano watt sub threshold comparators and resistive divider (flash ADC structure) and converted to a thermometer code. This is converted to a switch control bit pattern so as to distribute the clock states (ϕ_1,ϕ_2,$\surd$,X) as per Table 2.3. To switches $S_1 - S_{16}$ of the converter. This fixes the optimal gain of converter for given input intensity. Once the step up ratio is set the converter topology is fixed.

After programming gain of the converter we use the value stored on C_s i.e $3.\alpha$. V_{OC} to fix the MPP point .The OP-amp-VCO-CP feedback loop now locks to the MPP point. Once the MPP point is achieved we are assured of two points.

- Maximum possible power is squeezed from the PV cell at given intensity. This is ensured by MPP tracking irrespective of converter topology and PV cell manufacturer .
- Through programming the converter to optimal step up ratio we maximize the efficiency of converter at given intensity

From above two facts we can state that for wide range of intensities we harvest maximum possible power at output (P_{OUT}).

Further we use a feed back MPP approach. Thus, unlike that of an exponential MPP approach we do not require a non linear square law VCO used in [34, 35] . We instead operate with a linear VCO for better loop controllability and lesser power consumption. Fig. 4.2 shows the circuit of VCO used in this work. Inverters I_1 to I_5 form a five stage ring oscillator. The current of each stage is

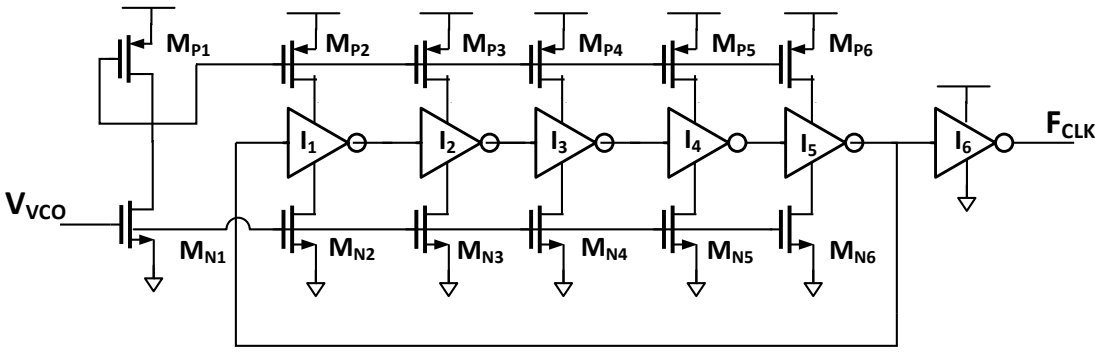


Figure 4.2: VCO used for MPP operation

controlled by copying from the current generator stack M_1 and M_2 . The current in M_1 and M_2 is

controlled by V_{IN} of M_1. Inverter I_6 refines the clock generated at the output of I_5. The frequency vs voltage characteristics are shown in Fig. 4.11(b) along with characteristics of [34].

4.1.2 Start up Circuit

The control circuits involved in the energy harvesting system consist of control units such as clock drivers which must be powered from battery itself . However there exist a practical situation when battery itself is drained out. In such cases arrangements must be made to initially charge the battery so as to power the drivers and controllers and thus start battery charging operation. We incorporate a cold start up circuit so as to charge the battery initially using a low efficiency converter and clock generator. Fig. 4.5 shows the internal diagram of start up circuit for our system. The start-up circuit consist of a chain of voltage doublers which can boost very low solar voltages (200m) to some intermediate range of voltages. The schematic of the voltage doubler circuit is that of a Nakagome charge pump [40] M_1 and M_2 are sized as minimum length and widhth specified by technology library. The moment light intensity reaches so as to produce a 200mV at output of PV cells, the low frequency ring oscillator turns on and supplies a weak clock to a voltage doubler . At each stage of voltage doubler the output amplitude grows so as to supply 1.8V at output. The start up time depends on capacitance of battery as well as the PV cell output power during start up operation.

In Fig. 4.5 the start up circuit block represents the low efficiency doubler chain shown in Fig. **??**. The operation of charge pump can be divided in two phases.

Charging Phase: Initial phase of start up operation is the charging phase .If the battery voltage goes below certain voltage say V_{UV} (V_{UV}=1.8V in our case) start up is enabled ,switches sw_1 and sw_2 are on while switch sw_3 is off . This is done by disconnecting the battery from converter and charging it through start up circuit to some 'take off' voltage(V_{TO}) .

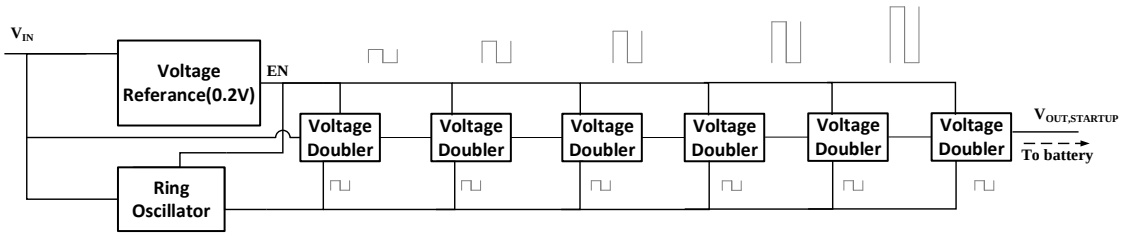


Figure 4.3: Internal diagram of start up circuit

Regeneration phase: After the battery reaches the take off point a Power On Reset circuit (POR) disconnects the battery from start up. This point of operation is known as 'take off' . After the take off the converter drivers are powered from the battery itself. As the voltage is 1.8 V at take off and thus a 1.8V clock is supplied to converter this leads to a higher voltage (greater than 1.8V) at the battery. This greater voltage is supplied to drivers and thus appear as higher amplitude clock (greater than 1.8V) at the charge pump further increasing the battery voltage. This operation can be understood as a positive feed back regeneration as shown in figure.

The regeneration phase falls under the 'safe mode' of battery protection which is discussed in Section 4.1.3. Simulations of start up circuit phases are shown in Section 4.2.3. After the battery voltage reaches 3.3V the circuit comes in full operational mode.

4.1.3 Battery management circuit

The battery management protects the battery from under voltage (UV) and over voltage (OV) conditions. We use a battery management similar to [7] . The circuit of a battery management involves two comparators as shown in Fig. 4.7. To save power we perform battery monitoring in sampling mode, i.e. we sample battery after every 1m second. The battery voltage is sampled as $V_{TEMPCAP}$ on a temporary off chip capacitor of smaller value (500pf). Comparators are enabled using a signal EN and the resistive divider is enabled using a complementary signal EN_bar this value is used to monitor battery condition. A voltage reference generates 1.25V. Three cases can exist depending on the battery voltage being sampled .

Under voltage: A under voltage case exist when battery voltage goes below 2.2V .In such cases battery has to be disconnected from the load. So that it further do not fall. When $V_{TEMPCAP}$ is

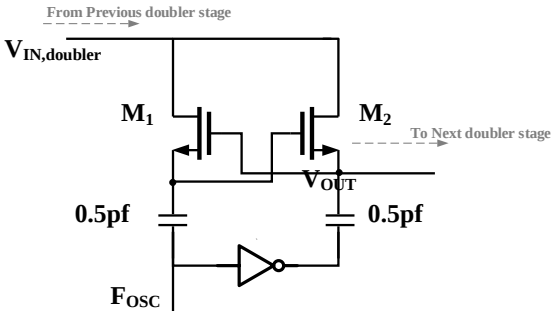


Figure 4.4: Internal diagram of voltage doubler

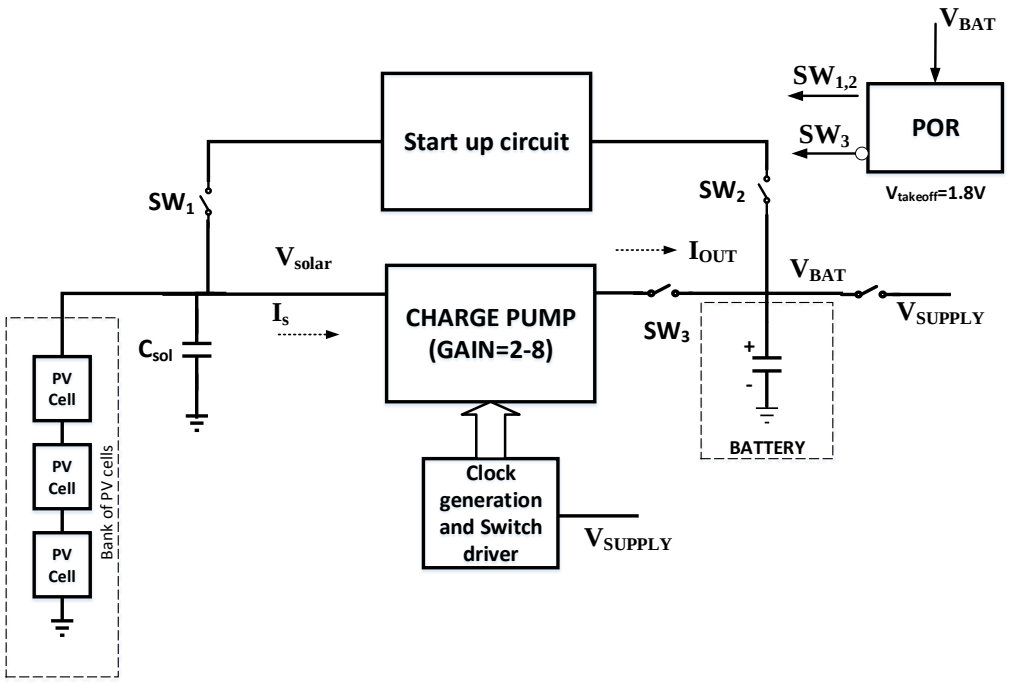


Figure 4.5: Architecture of start up operation

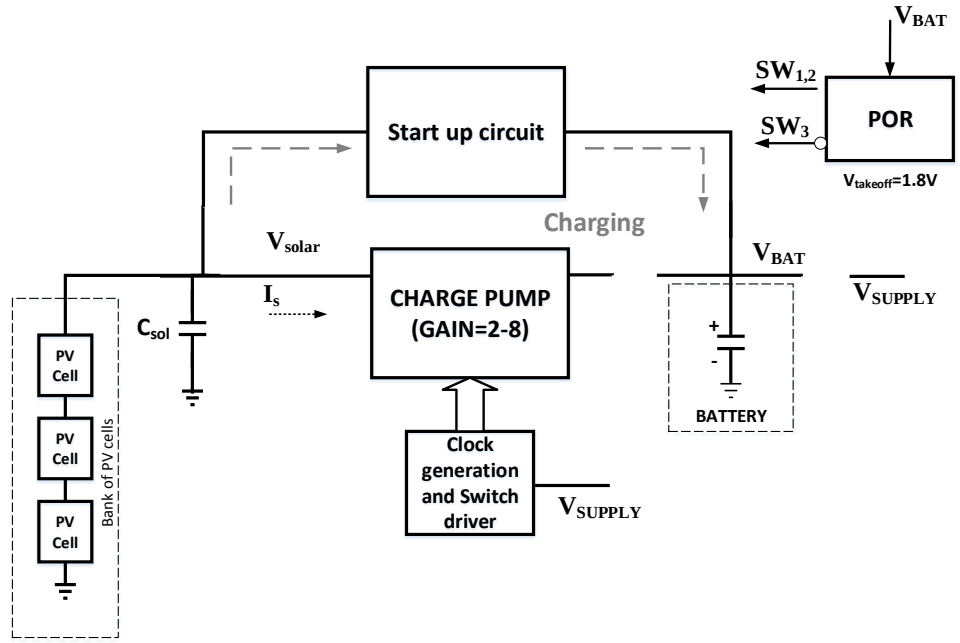
2.2 Volt the voltage, V_{UV} appearing on non inverting terminal of C_2 through the resistive divider is given as.

$$V_{UV} = V_{TEMPCAP}\left(\frac{R_2}{R_1 + R_2}\right) \tag{4.1}$$

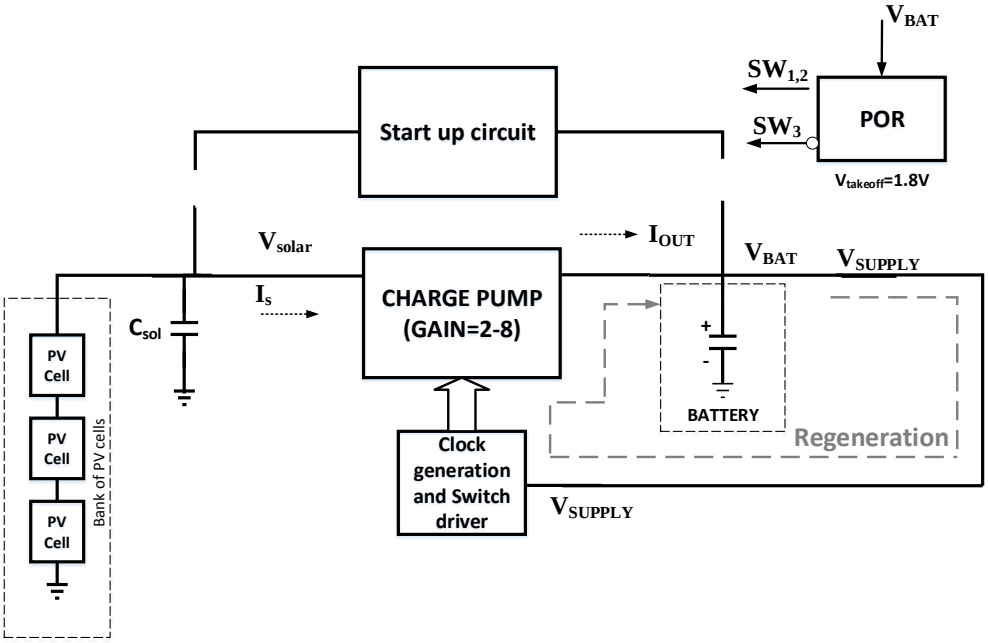
At $V_{TEMPCAP}$ = 2.2V , V_{UV} should be equal toV_{REF} (1.25V) this gives us resistive divider fraction of 0.56 and we choose values of R_1 and R_2 as 6MΩ and 3.5MΩ respectively. The values are chosen in MΩ to avoid leakage through resistive divider during sampling time. When $V_{TEMPCAP}$ fall below 2.2V, V_{UV} falls below V_{REF} and signal UV goes high while OV remains low. This disconnects battery from load until battery comes in safe zone.

Over voltage: A over voltage case exist when battery voltage goes above 3.4V .In such cases battery has to be stopped from further getting charged and must be allowed to power the load. When $V_{TEMPCAP}$ is 3.4 Volt the voltage, V_{OV} appearing on non inverting terminal of C_2 through the resistive divider is given as.

$$V_{UV} = V_{TEMPCAP}\left(\frac{R_3}{R_3 + R_4}\right) \tag{4.2}$$



(a) Charging phase



(b) Regeneration phase

Figure 4.6: Charging and regeneration phase of start up circuit

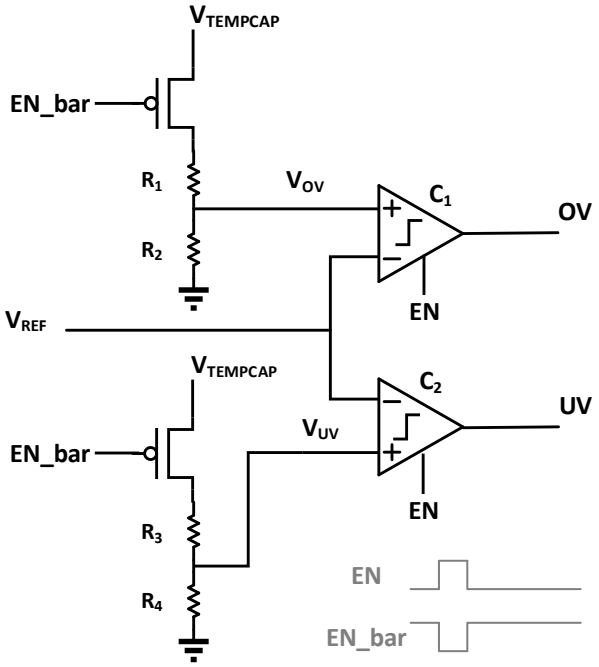


Figure 4.7: Internal circuit of battery over voltage and under voltage protection

At $V_{TEMPCAP} = 3.4$V , V_{OV} should be equal toV_{REF} (1.25V) this gives us resistive divider fraction of 0.36 and we choose values of R_3 and R_4 as 5.6MΩ and 4.2MΩ respectively. When $V_{TEMPCAP}$ rise above 3.4V, V_{OV} rise above V_{REF} and signal OV goes low while UV remains low. This disconnects battery from converter until battery comes in safe zone.

Safe mode When $V_{TEMPCAP}$ lies between $2.2 - 3.4V$ C_1 produces a logic 1 while C_2 produces logic low and battery is in safe mode of operation. This can be termed as 'safe mode' of operation.

4.2 Detailed Simulation

4.2.1 Converter efficiency across various illumination

The converter was analyzed for its efficiency acreoss various illuminations . The regulated efficiency curve were plotted against intensity .The output of converter was regulated to 3.3V. Verilog-A model was written to replicate the model of PV cells in silulations the open circuit voltage of the three PV cell in stack was changed and the efficiency was observed .The gain of converter was programmed for various step up ratios (gains) and the efficiency curve was plotted for various step up ratios across all intensities. And the results are plotted in Fig. 4.8. We can infer from figure that we get optimal

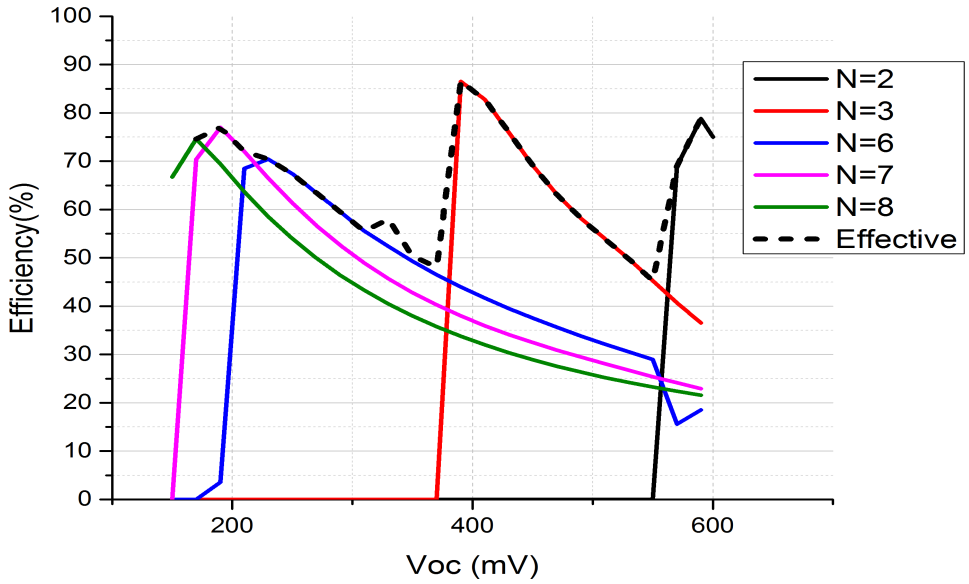


Figure 4.8: Efficiency of the converter for various step up ratios across various light intensities expressed in terms of V_{OC} of single PV cell

possible efficiency across wide range of intensities the minimum achieved efficiency was 48%. The maximum efficiency is achieved at $N = 3$ which is around 86%.

At every N, below some intensity of PV cell under test the converter the efficiency drops to zero as well as it gradually drops after the efficiency maxima. These effects observed in simulations are as per our discussions in Section 2.1.1.

When the illumination sensing unit was enabled. The intensity was swept and eventually the gain changes as per the intensity . This results black dotted curve shows the effective efficiency when converter was operated with a illumination (input voltage) sensing unit. From the simulation results we can infer that a reconfigurable converter is better in a high voltage energy harvesting much reliable than a dedicated architecture discussed in [15, 21, 22]

4.2.2 MPPT simulation and VCO characteristics

The energy harvesting system system was designed using UMC 0.18 μM CMOS technology. Performance details of harvester are given in Table 4.2. The system is self sustaining i.e. the control unit derives the supply from harvested power. A cold start up circuit was incorporated in system to start the converter and control unit from low energy condition ($V_{SOLAR} = 273mV$). A diode based solar model was used to replicate PV cell input (CELL-1, CELL2, CELL3) to the circuit. To verify

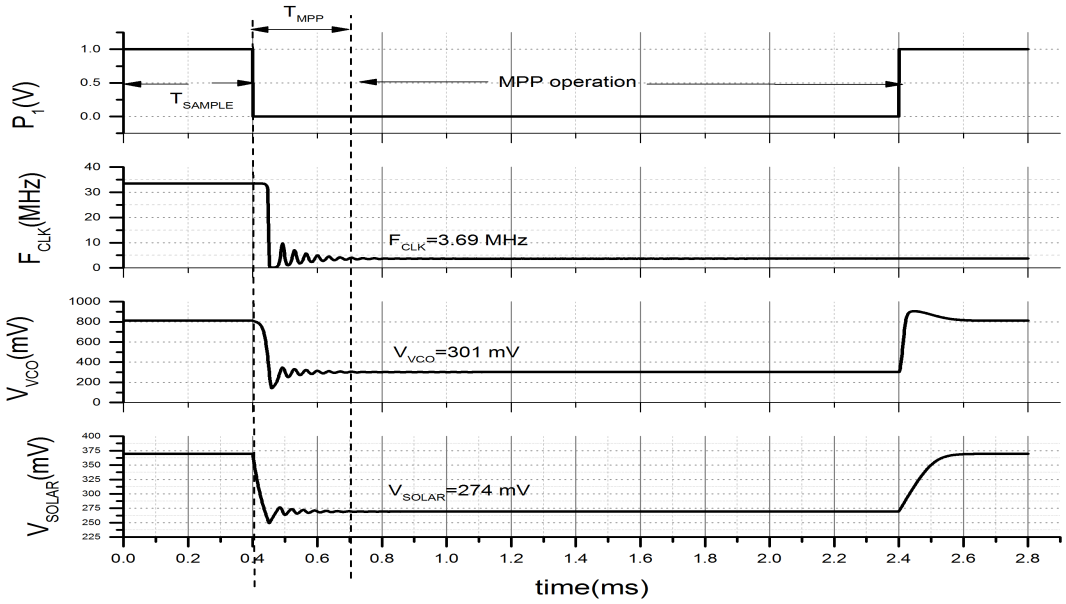


Figure 4.9: Simulation of proposed MPP with N=5

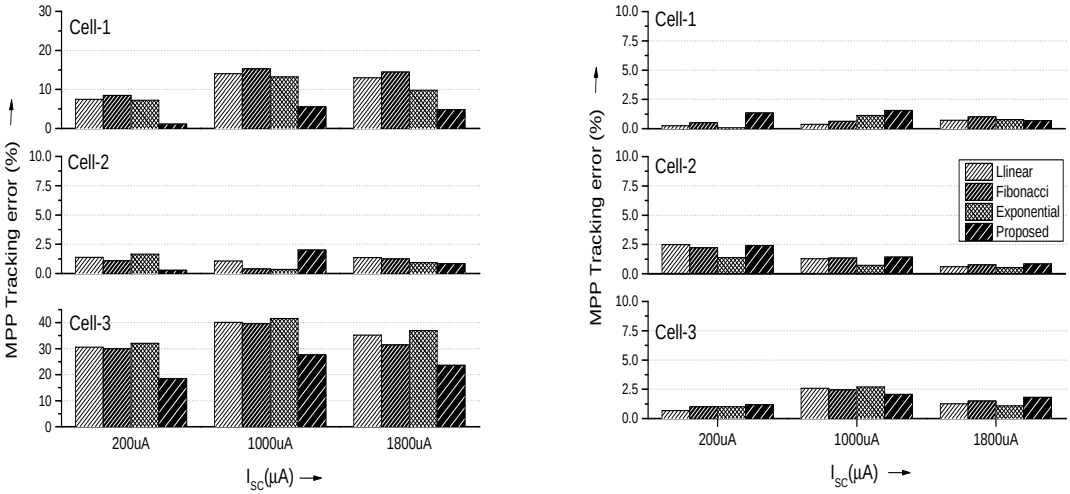
circuit operation, we first simulate circuit with a four stage linear charge pump topology ($N = 5$) at I_{SC} of 1000 μA. Resulting waveforms are shown in Fig. 4.9.

Initially during phase P_1, clock to the charge pump is disabled and hence the charge pump is seen as a open circuit from PV cell. Thus V_{SOLAR} reaches V_{oc} i.e 370 mV at particular radiation. Simultaneously, resistive divider samples 75% of V_{OC} on capacitor C_S, this value is MPP voltage which is 269 mV at given intensity. As P_2 starts functioning, V_{SOLAR} falls down from V_{oc} to V_{MPP} and finally settles down at 269 mV (V_{MPP} at 1000 μA). The clock frequency settles down to a MPP clock frequency of F_{MPP}. The tracking time, T_{MPP} is 200 μs. To observe the effectiveness of MPP operation, percentage error($\epsilon_{\%}$) in MPP tracking is quantified as:

$$\epsilon_{\%} = \frac{P_{MPP} - P_{Harvested}}{P_{MPP}} \tag{4.3}$$

The key results of proposed MPP are listed below.

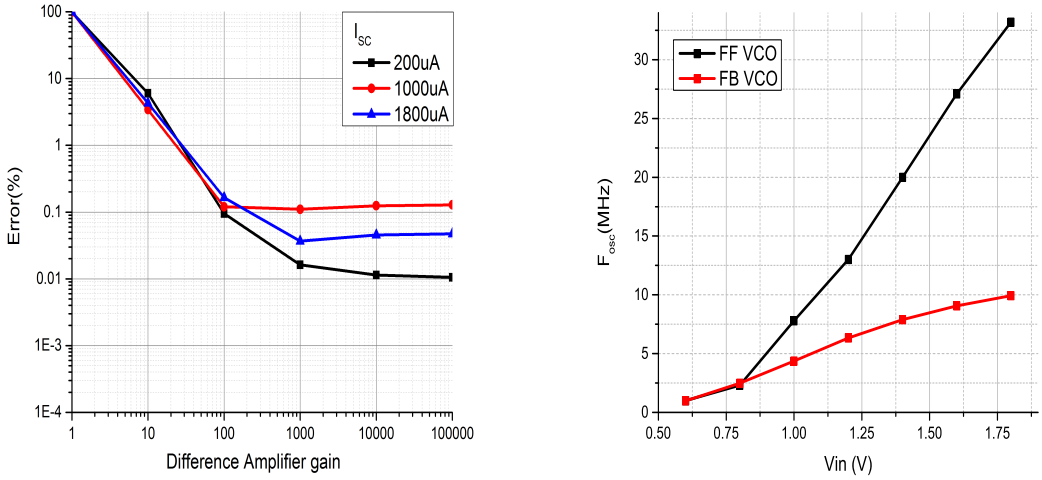
- The system is simulated for various converter topologies (Linear, Fibonacci, Exponential and Tree charge pump), with three diffrent PV cells (CELL-1, CELL-2 ,CELL-3) and error in MPP tracking is plotted for Feed Forward and proposed technique in Fig. 4.10. For Feed Forward



(a) Feed Froward MPPT tracking unit

(b) Proposed MPPT tracking unit

Figure 4.10: Tracking error across various PV cells and converter topologies



(a) Feed Froward MPPT tracking unit

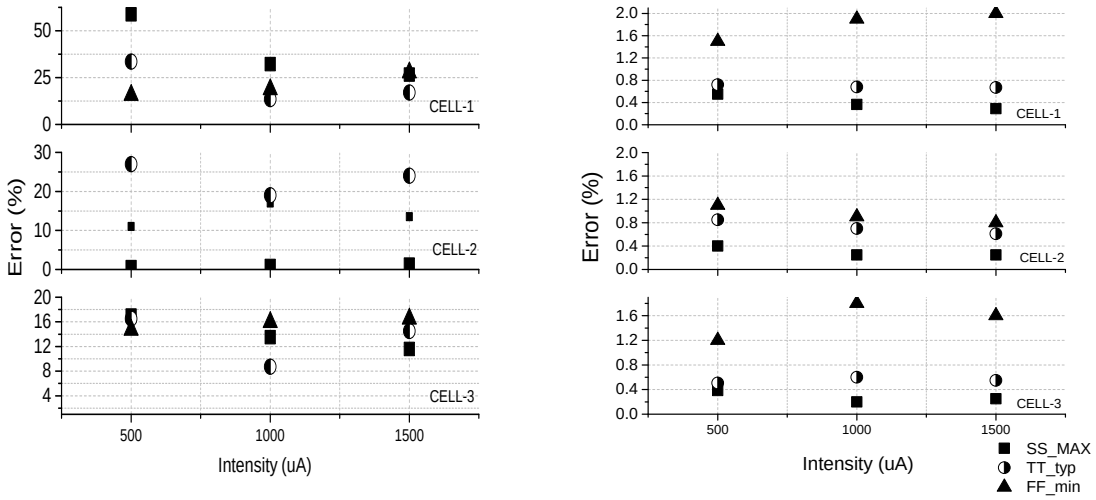
Figure 4.11: Details of OP-AMP VCO interface

MPP the VCO is designed for CELL-2 and hence MPP error for CELL-2 is within 1%. However this error increase significantly (10-40%) for CELL-1 and CELL-3.
On the other hand for Proposed MPPT, the error is within 2.5% for all PV cells and converter topologies. Hence the problem of feed forward MPPT's dependency on PV cell and converter topology can be solved through proposed feed back based approach.

- Since the approach involves an op-amp in feed back path, we have also verified the impact of op-amp gain on MPP accuracy, and corresponding tracking error is plotted in Fig. 4.11(a). It has been observed that increasing the gain reduces the MPP tracking error and beyond gain of 1000 (60dB) the error does change significantly. Since increasing the gain also increases power head of the amplifier. To minimize power and error the gain of amplifier is chosen as 1000.

- Layout of full system along with charge pump is shown in Fig. 4.18. Post layout simulations were carried out across extreme process corners (ss, tt, ff) and the tracking error plotted in Fig. 4.12. It is observed that the FF MPP operation is significantly sensitive to process variations. Even in CELL-2 (the cell for which MPP VCO is designed), the performance degrades across ss and ff corners. While for proposed case it lies within 2.5.% for all process corners for various PV cells. Thus proposed MPP technique is very effective in CMOS realization.

- We use a linear VCO as compared to that of Feed Forward(FF) MPP used in [34] for better loop controllability. The VCO characteristics are shown in Fig. 4.11(b). The operating frequencies required for our PV cell-converter interface are low. This leads to significant power reduction.



(a) Feed forward MPPT tracking unit

(b) Proposed MPPT tracking unit

Figure 4.12: Tracking error across various PV cells and process corners

Table 4.1: Operating frequency of generator

I_{SC}	Operating frequency of the clock generator (MHz)	
	Duty cycle approach	Proposed MPP technique
200 μA	6	0.77
1000μA	6	2.90
1800μA	6	4.86

4.2.3 Start up simulations

The start up simulations are shown in Fig. 4.13. The battery voltage V_{BAT} is initially zero (the battery is totally drained out). The driver supply voltage, V_{SUPPLY} is also zero.Hence the system is totally out of energy. The moment some very low solar voltage $(100 - 150mV)$ exist at PV cell output.The start up path is enabled by POR and the battery starts charging to the take off voltage that is 1.8V in our case. To reduce simulation time the battery size is kept at a small value (100nF) . With course of time take off is achieved at 1.8 V and the battery voltage is sufficient to power the driver and clock generation circuit . At this point battery is connected to supply of drivers and clock generator. Now the circuit operates in regeneration mode and finally the battery voltage as well as the clock amplitude regenerates to 3.3V .

4.2.4 Battery management circuit simulations

The battery management simulations for under voltage and over voltage protection are shown in Fig. 4.14(a) and 4.14 respectively . During UV protection the UV signal is low until $V_{TEMPCAP}$

Table 4.2: Performance details for harvester

Performance parameter	Value
Efficiency	55
Minimum power throughput $P_{Harvested,min}$	12μW
Maximum Power throughput($P_{Harvested,max}$)	690μW
Input voltage range	0.27-0.5 V
Output voltage	1V
MPPT tracking efficiency	98%

is sampled below 2.2V. At this point UV goes high to 2.2 V i.e the battery voltage (as everything is powered by battery). During UV protection the UV signal is high until $V_{TEMPCAP}$ is sampled above 3.4 V. At this point OV goes low to 0 V fro a initial voltage of V_{BAT} i.e the battery voltage . To keep simulation time low we have reduced the battery size i.e around 100nf. In real scenario these waveform can be scaled up in time considering a larger battery capacitance. The battery management circuit consumes around 400nA of current and hence is cheap in terms of power head.

4.3 Complete system architecture and layout in UMC 180nm CMOS

Complete system architecture is given in Fig. 4.15. System operation and condition for various voltage levels are shown in Fig. 4.16. The system was designed in UMC 180nm technology .Power consumption of assisting control blocks was 23.5μW.

The percentage overhead of this total power by each separate unit is shown in pie chart of Fig. 4.17 . System layout is shown in Fig. 4.18. Comparison of proposed harvester with recent novel works is shown in Table. 4.3. Tape out of system is done in UMC 180nm and results are fine across

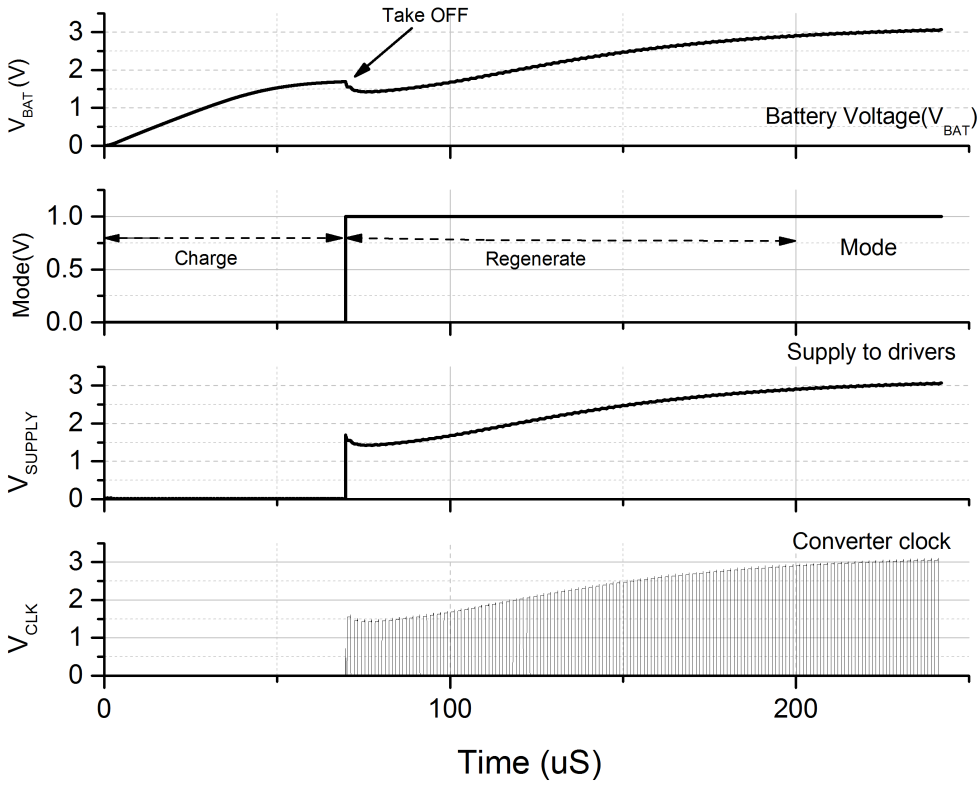
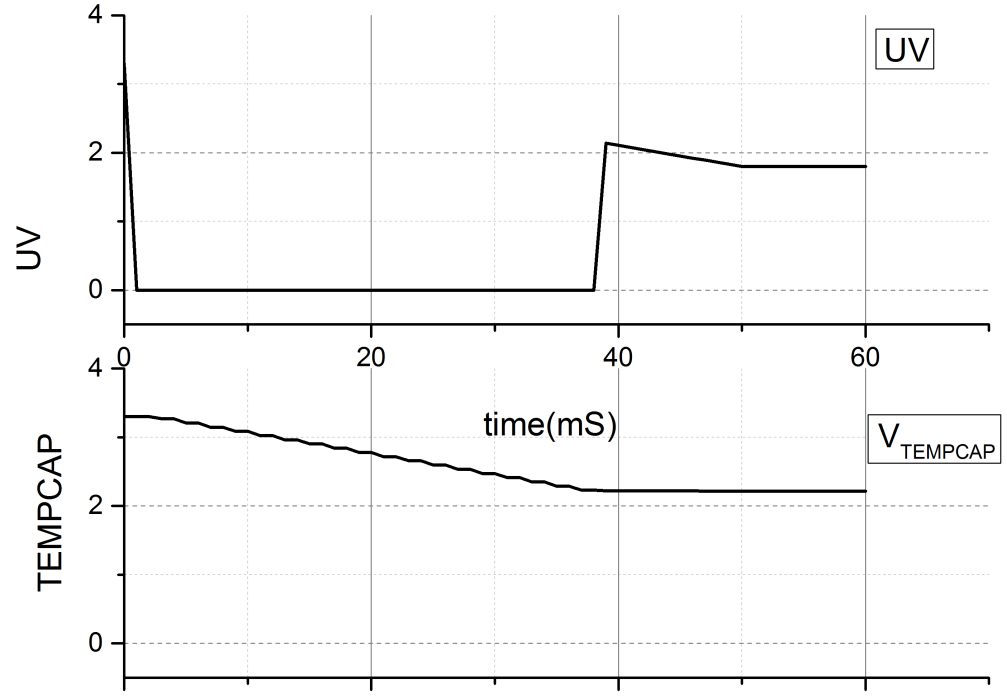


Figure 4.13: Operation of start up circuit

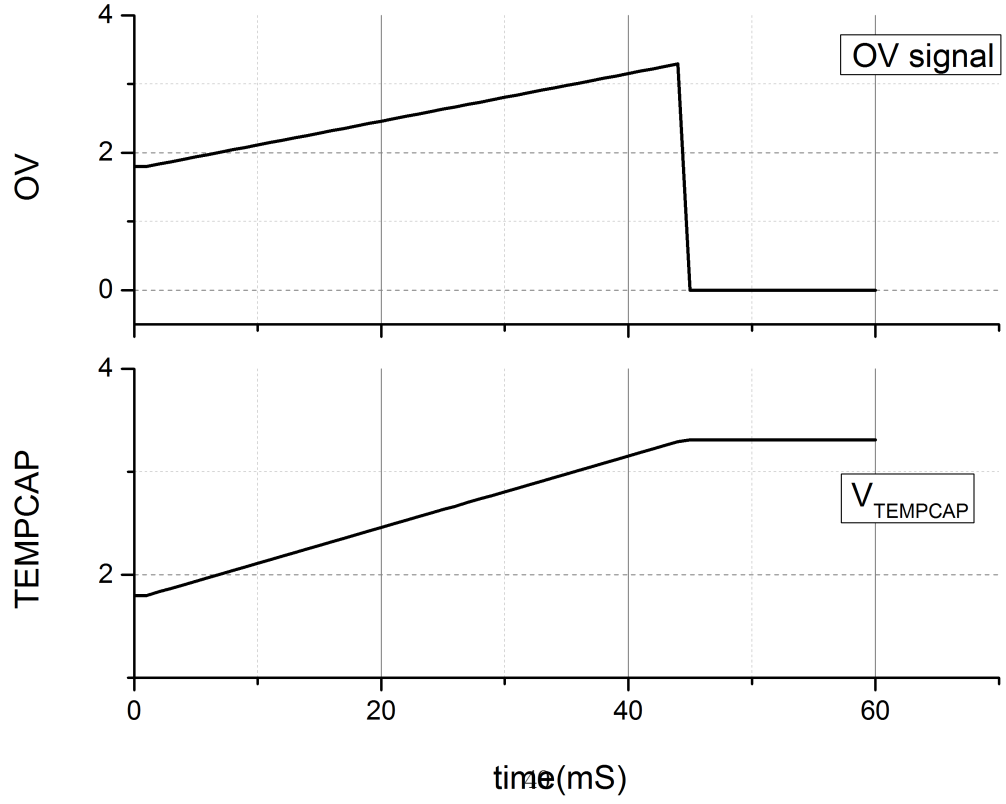
extreme process corners as shown in our simulations in previous sections.

4.4 Conclusions and Possible improvement

Proposed full system description and performance verification discussed in this chapter reveals that proposed system is not only adaptive to changes in illumination. But also involve condition aware energy harvesting such as battery management to enhance lifetime and circuits like cold start up to start up the circuit without any manual intervention. However many exiting problems are open with this system to work . The work can be characterized and extended to TEG and vibrational energy harvesting systems. A user enabled output voltage selection can be added which configures entire system to work for various battery voltages. That would be a nice step contributing to load independent harvesters. A detailed comparison of features of porposed system with some recent novel works is given in Table 4.3.



(a) Charging phase



(b) Regeneration phase

Figure 4.14: Charging and regeneration phase of start up circuit

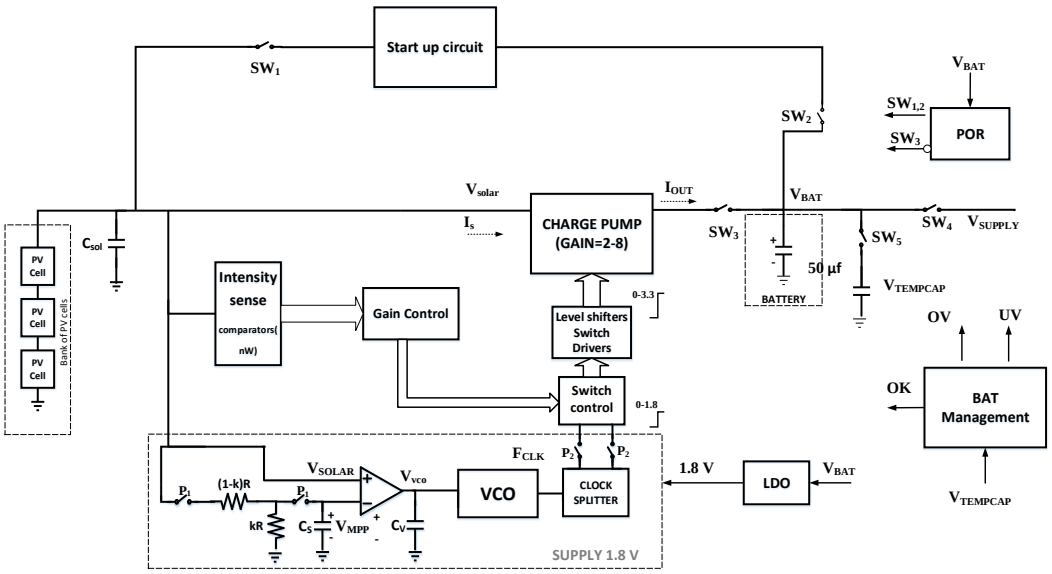


Figure 4.15: Architecture of 3.3V energy harvester system

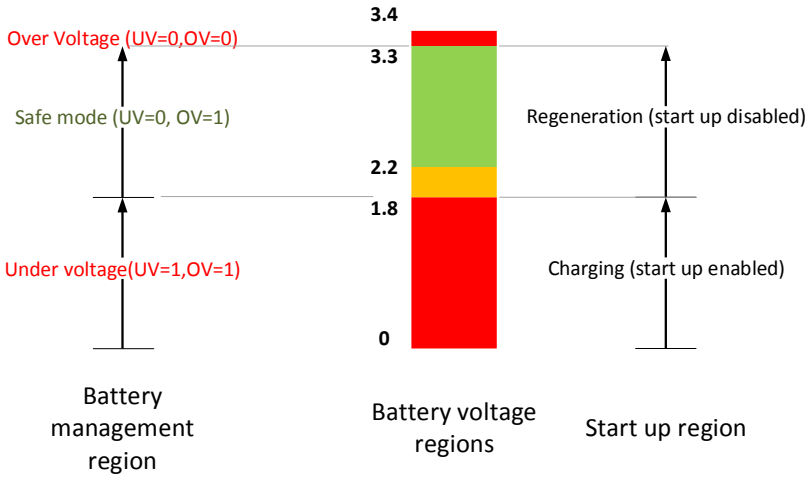


Figure 4.16: System operation under various battery conditions

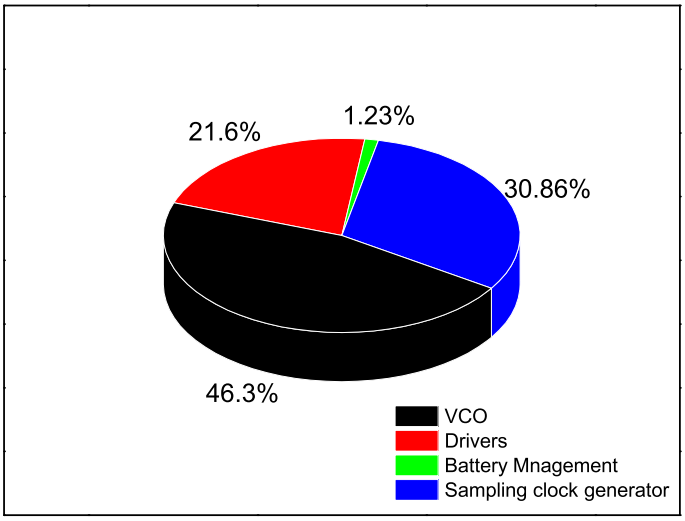


Figure 4.17: System operation under various battery conditions

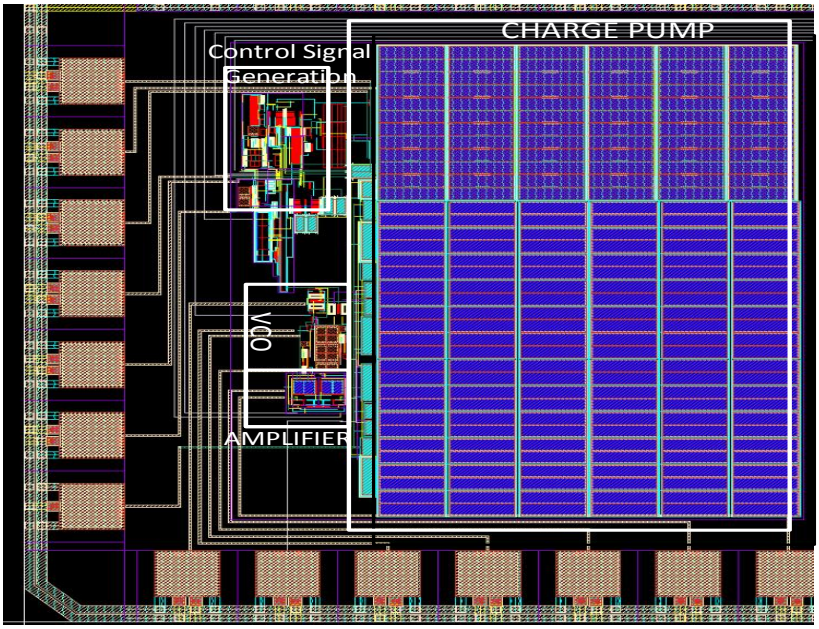


Figure 4.18: Layout of proposed system along with charge pump

Table 4.3: Comparison of proposed harvester with previous literatures

Feature	[21]	[22]	[25]	[23]	[24]	This work
Technology	180nm	AMS 350nm	350nm	130nm	350nm	180nm
Input voltage range	1-1.5	2.1-3.5	0.5-2	1-2.7	1.8	0.8-1.8V
Output voltage range	3-3.5	3.6-4.4	0-5	1.4	2	3.3V
Power throughput	0-29μW	100-775μW	5-1000μW	0-10μW	0-80μW	12-650μW
Battery Protection	No	No	No	No	No	Yes
Self sustaining & Fully in chip	Yes,Yes	No, Yes	Yes,No	Yes, Yes	No, Yes	Yes, Yes
Maximum system efficiency	88%	67%	70%	58%	86%	82%
Illumination aware	No	No	No	No	No	Yes

Chapter 5

Conclusions and Future work

This dissertation was focussed on a 3.3V PV harvester for sensor nodes and biomedical applications. This can be in a way considerd a contribution to wearability of devices due to achievement of conventional 3.3V output without a off chip passive component. However the fully on chip operation does not affect the efficiency and the interface is illumination aware able to scavenge for wide range of illumination making it more suitable over other on chip harvesters. We achieve a minimum efficiency of 48% in worst case. We have also discussed terms like PV cell independence and modelled it mathematically. We achieved a MPP tracking efficiency of at least 97.5% This was a contribution considering upcoming market ecosystem of harvesters where one could see many manufacturers of PV cells as well as harvesters thus enabling the user to be independent in selection of manufacturer of PV cells. Also this leads to lifetime of harvester against the ageing and surrounding conditions. Apart from converter and MPPT we discussed the lifetime and safe operation of battery as well. We were able to maintain the battery voltage in safe voltage ranges for long run operation. System was autonomous and The design challenges introduced with SC energy scavenger in the very first chapter were well met and a start up was added to start the system from a totally drained out condition. Such features are very important considering rural and remote locations where reach of technology and maintenance is still not upto the mark.

Future Work Although in this work we tried to push the ease of use and compactness as much as possible, there is scope in so many exciting problems to work with . In lower technology ranges the capacitance that can be integrated per unit area of silicon increases but other second order effects become even more severe than the existing technology this require more detailed modelling of SC DC DC converters in these technology nodes. Increasing research in PV cell energy harvesting is

now attracting reserchers towards on chip PV cells. Several such systems are proposed at abstract level in literature [41–45]. However, one needs to characterize the behaviour of CMOS photo diodes with refrence to energy harvesting in integrated CMOS environment . Generally the cmos diodes are characterized by post layout silicon results . One such effort was placed in [46]. This is not fesible considering a full system design including the harvester and sensor node. Apart from this, the form factor of CMOS photo-diode is even poorer than their discrete versions. Proper layout techniques needs to be used as done in [47]. Also technology roadmap has to come up for packaging and integration of such devices .Investigation can be done for utility of on chip photo-diode apart from conventional CMOS technologies. Success such on chip PV cell systems would be further a revolution in sensor nodes and IOT. Further the concept of platform independent fractional open circuit MPPT has to be explored for TEG and vibrational interfaces. This is a challenge because the transducers for TEG behave like a strong voltage sources and tuning their output voltage is a challenging task. Also its utility in hybrid energy harvesters has to be explored.

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