

# Low Power Analog Front End for ExG Acquisition with Automatic Gain Control and Analog Classification

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The Degree of Master of Technology

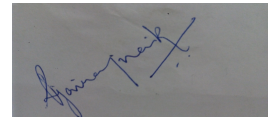


Department of Electrical Engineering

June 2015

## Declaration

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## Approval Sheet

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# Dedication

All hardworking souls

## Abstract

Cardiovascular diseases have been known to cause large number of deaths globally. For prevention and early detection of these diseases, continuous monitoring of ecg signals is required. With recent advances in IC technology, implantable ICs have seen the light of the day. Considering the implantable devices, power consumed by the system needs to be as less as possible without sacrificing the performance of the readout circuit. Due to the low frequency nature of the circuit,  $1/f$  noise dominates the noise profile. Moreover, the common mode interference from the power lines and the offset due to skin electrode interface needs to be removed. For effective signal acquisition under these circumstances, an analog front end with high CMRR, low noise and band pass characteristics is necessary. Moreover, to acquire different bio potential signals, the front end should have configurable gain and bandwidth characteristics. A programmable gain amplifier (PGA) is used to cater the need of variable gain. The gain of the PGA can be set using a automatic gain control circuit. A capacitively coupled signal acquisition system has been designed in UMC 0.18 $\mu$ m technology, it achieves an overall linearity of more than 10 bits with 0.47 $\mu$ W power consumption.

In conventional signal acquisition systems, a digital classifier is used post analog-digital converter(ADC) for identification of abnormal ecg signals to save power in the subsequent signal processing blocks. One of the important characteristics of an abnormal ecg signal can be seen in the form of abrupt changes in its amplitude. Taking advantage of this feature of the signal, a novel analog classification scheme has been implemented. The advantage of signal classification in the analog front end stage is twofold viz., a first order sigma delta ADC can be used for digitizing the abnormal signal instead of a second order sigma delta ADC, significantly reducing the power consumption of the overall system. Moreover, reusing the same automatic gain control circuit (AGC), previously used for setting the gain in PGA, can be used for this purpose. This further saves the power and area penalty of a separate circuit.

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# Chapter 1

## Introduction

According to the World Health Statistics 2012 report out of 57 million global deaths in the standard year 2008, 36 million died from non-communicable diseases (NCDs) of which 48% died from cardiovascular diseases (CVDs) [4]. This calls for a system which focuses not only on curing the illness (hospital- centric approach), but also on prevention and early detection of symptoms (patient-centric approach). Continuous ECG monitoring of biosignals become mandatory for such systems. All this, augmented with the radical advancement in CMOS and wireless communication technologies, has given impetus to concept of u-Health (ubiquitous healthcare) and use of wireless body area network (WBAN) based applications.

### 1.1 Biopotential Signal Characteristics

Biopotential signals are generated due to the electrical activity of cells that are components of nervous, muscular or glandular tissues. A non-zero current flows from the body to the input of the readout circuit. This current is carried by ions in the body and electrons in the wires connecting the electrodes to the readout circuits. A transducer interface, biopotential electrode, between the readout circuit and the body converts this electronic current into ionic current and vice versa. There appears a DC potential between the two electrodes, much larger than the differential input signal. Hence, the readout circuit should include a high pass filter to remove DC and prevent the saturation of subsequent circuits. Fig. 1.1 shows the amplitude and frequency ranges occupied by various biopotential signals. [1] Fig. 1.2 shows the transient response of electrocardiogram (ECG), electroencephalogram (EEG), electromyogram (EMG) and electrooculogram (EOG) respectively. All biopotential signals share some common characteristics essential for designing the readout circuits

namely [2]

- Small amplitudes (10  $\mu$ V to 10 mV) as can be seen in Fig. 1.2
- Low frequency range of signals (dc to several hundred hertz)
- Presence of biological interference (from skin, electrodes, motion, etc.)
- Noise from environmental sources (power line, radio frequency, electromagnetic, etc.).

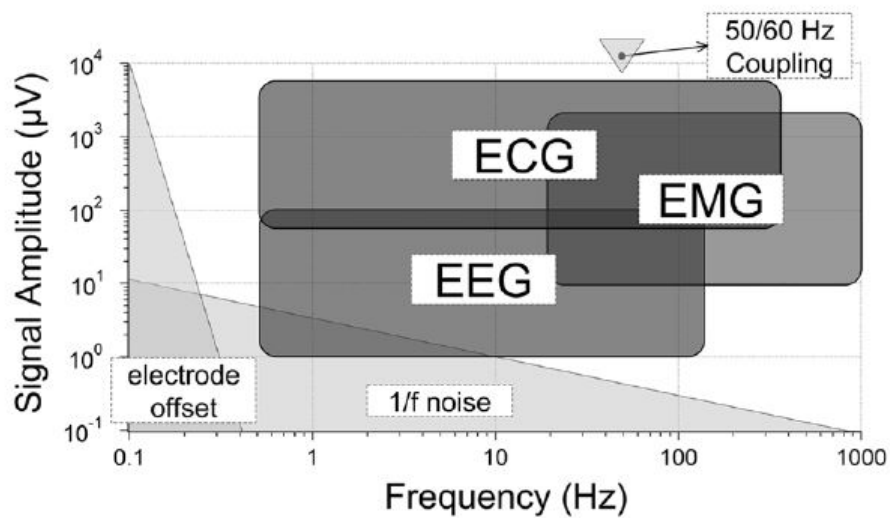


Figure 1.1: Frequency and amplitude ranges of various signals [1]

## 1.2 System Design Requirements

Following requirements need to be fulfilled by the readout circuit:

- High input impedance
- Amplify signals in the frequency band of interest
- High common mode rejection ratio
- Consume little silicon area and use few or no off-chip components to minimize size
- Block dc offsets present at the electrode-tissue interface to prevent saturation of the amplifier

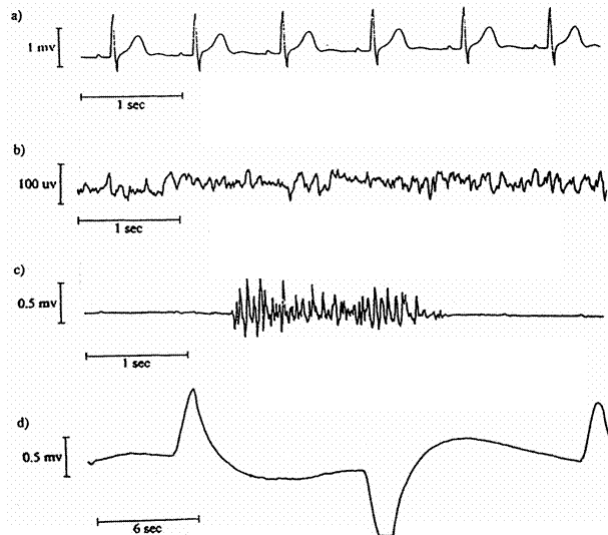


Figure 1.2: Transient response of various biopotential signals [2]

The system needs to have an input impedance many times higher than that of the electrode to efficiently extract the signals from the electrode. To reject the high and low frequency noise, the system needs to have a bandpass response. Also, to reject the common mode noise from the 50Hz power line, a system with high common mode rejection ratio is desired. For wearable and implantable systems, low area and power requirements are a must. The following chapters explain in detail the design methodology incorporated in designing the ASIC.

### 1.3 Noise Efficiency Factor

To compare various systems on the basis of the noise and power consumption, a figure of merit was introduced by [5]. The total equivalent input noise of an ideal bipolar transistor (only thermal noise and no base resistance) is given by

$$V_{in,rms} = \sqrt{\frac{BW * \pi * 4kT}{2gm}} = \sqrt{\frac{BW\pi * 4kTU_T}{2 * I_c}} \quad (1.1)$$

with BW being the frequency bandwidth (for a bipolar transistor this is the ft). The NEF of a system is then defined as

$$NEF = V_{rms,in} \sqrt{\frac{2I_{tot}}{BW\pi * 4kTU_T}} \quad (1.2)$$

where  $I_{tot}$  is the total drain current and  $V_{rms,in}$  is the total equivalent input noise. The NEF describes how many times the noise of a system with the same current drain and bandwidth is

higher compared to the ideal case, e.g., for a CMOS transistor with only white noise, the noise power is given by

$$V_{in,rms}^2 = \frac{4kT}{\frac{2g_m}{3}} BW \frac{\pi}{2} = \frac{3kT(V_{gs} - V_T)}{I_D} BW \frac{\pi}{2} \quad (1.3)$$

or, working on the boundary of strong inversion and the same bandwidth as the bipolar, the NEF is 2.43. This means that the noise of a CMOS design in strong inversion with the same current drain and bandwidth is approximately five times higher compared to a bipolar design. In weak inversion, transconductance is linearly proportional to bias current, so from 1.3 we can see that noise spectral density is inversely proportional to bias current. So, a trade off exists between power consumption and noise of the system. The goal towards designing better bio potential amplifier system should be to reduce the power without compromising with the performance of the system. [1, 6, 7]

## Chapter 2

# ECG Readout Front-End ASIC

There has been a spur in the number of research and publications related to self-powered acquisition systems for body sensor nodes (BSN). Incorporating energy harvesting mechanism can endow BSNs an indenite lifetime. An ultra - low power system rendering the functionality of acquiring, processing and transmitting is presented in . The BSN chip is powered by the energy harvested from human body heat through a thermoelectric generator (TEG). Another batteryless acquisition system powered by an adaptive RF scheme is reported in [8]. Reference [9] presents an excellent review on self-sustainable systems. Some related works make their system recongrurable also. Such a system with different types of monitoring is described in [10].

### 2.1 Readout front end ASIC

The read out analog front end block diagram is as shown in Fig. 2.1. The system consists of a lead detector circuit to power up the system only when both the leads are connected. To generate a band pass response, a high pass and low pass filter is added . The output of the two stage amplifier stage is given to the automatic gain control circuit and also to the ADC. The gain of the amplification stage is decided by the AGC depending on the input amplitude to the AGC. To get maximum signal to noise ratio at the output of the sigma delta ADC, an input amplitude of 200mVp-p is desired. The primary function of AGC is to set the gain such that the ADC input amplitude is around 200mVp-p. The analog classifier block detects the abnormal signal by monitoring the switching sequence of the AGC i.e. by monitoring the random fluctuations in the ECG signal.

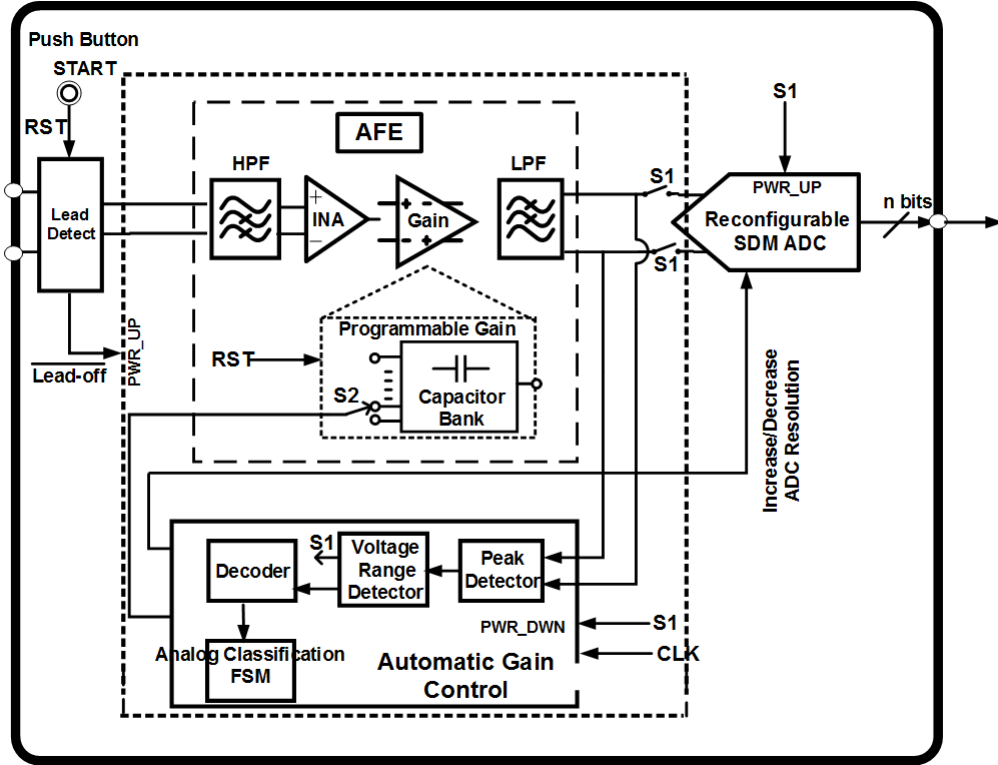


Figure 2.1: Block diagram of the whole biopotential readout circuit along with the ADC

## 2.2 System level description of the amplifier front end

As can be seen in the circuit, the amplification stage is implemented as a two stage capacitive coupled signal amplifier structure. The voltage gain of the closed loop amplifier can be varied by varying the feedback factor. Resistive feedback network leads to excess dc power consumption, hence capacitive feedback is used for closed loop gain control. In order to set the DC common mode, resistors have to be used as negative feedback parallel to the feedback capacitor. The value of this resistor also decides the HPF cut-off and hence, should be large. [3, 7]

The midband gain of the single stage OTA based capacitive feedback amplifier is given by

$$A_v = \frac{C_1}{C_2} \quad (2.1)$$

The gain variation with frequency is as shown in Fig. 2.3. The noise variation with frequency is as shown in Fig. 2.4. As the signals under consideration are low frequency signals, flicker noise is dominant in the system. However, the bandpass characteristics of the system reduces this noise component. In case of  $R2$  being implemented as a real resistor, the noise component of  $R2$  is given by



$$V_{nR}^2(f) = 4kTR \quad (2.2)$$

The corner frequency is approximated to be

$$f_{corner} = \sqrt{\frac{3C_L f_L f_H}{2C_1}} \quad (2.3)$$

To minimize noise contribution from  $R_2$ , the corner frequency should be less than  $f_H$ . This can be accomplished, if

$$\frac{C_L}{C_1} \ll \frac{2f_H}{3f_L} \quad (2.4)$$

As can be seen in Fig. 2.4, the OTA noise dominates in the bandpass region. And it is dependent on the input parasitic capacitance, creating a severe trade off between flicker noise component and total noise in the mid band region.

If the noise from  $R_2$  is made negligible, and  $C_1 \gg C_2, C_{in}$ , the output root mean square noise voltage is dominated by the OTA noise. Thus, the design of the OTA is very crucial for achieving the desired performance. [3]

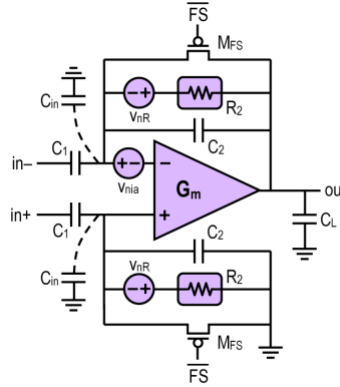


Figure 2.2: Example OTA based amplifier with capacitive feedback [3]

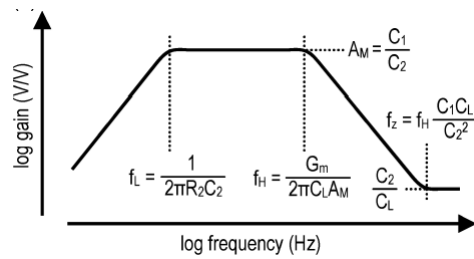


Figure 2.3: Frequency response of the amplifier [3]

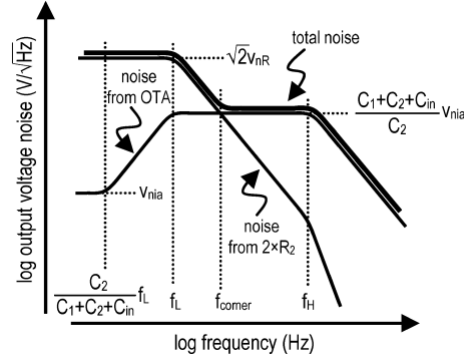


Figure 2.4: Output noise versus frequency [3]

The gain has been divided between the two stages based on the reason that the first stage needs to have low noise and higher gain, so that the subsequent stages have less impact on the noise performance of the system. A gain of 40dB was assigned to the first stage. The second stage has a gain which can be varied from 0-20dB by varying the capacitor ratio.

The large input capacitance (10 to 20 pF) also translates to equivalent input impedance that, in connection with the electrode impedance, form a frequency-dependent potential divider circuit at the input of the amplifier. If the input impedance is insufficiently high, the recorded signal will not only be attenuated, but it will also undergo amplitude and phase distortion. The effective common mode rejection ratio will also be degraded if the signal and reference electrode impedances are slightly mismatched. Hence, there is a need to increase the input impedance. In order to get the same gain with higher input impedance, the input capacitor as well as the feedback capacitor has to be reduced. However, there is limitation on the accuracy of lowest possible capacitance that can be fabricated. Therefore, a method is used to reduce the effective capacitance whilst using a fairly high value capacitor. To achieve this, a T-feedback network is used so that the same gain can be maintained with much smaller input capacitance [11]. From Fig. 2.5 the effective gain is given by  $M^*(N+2)$ .

In order to set the DC common mode, resistors have to be used as negative feedback parallel to the feedback capacitor. The value of this resistor also decides the HPF cut-off and hence, should be large. The high pass filter cut-off is in the range of 250 mHz to 1Hz, leading to resistor values of tens of Giga ohms. Looking at a complete on chip solution, it is not feasible to fabricate such high value resistors. Fortunately, this application does not need high accuracy in terms of high pass pole. Pseudo resistor operating as a linear resistor in the required region of operation are largely used to provide this high pass pole. The high pass cut-off is varied by varying the gate voltage of pseudo

resistors. Low pass cut-off is tuned by varying the load capacitor.

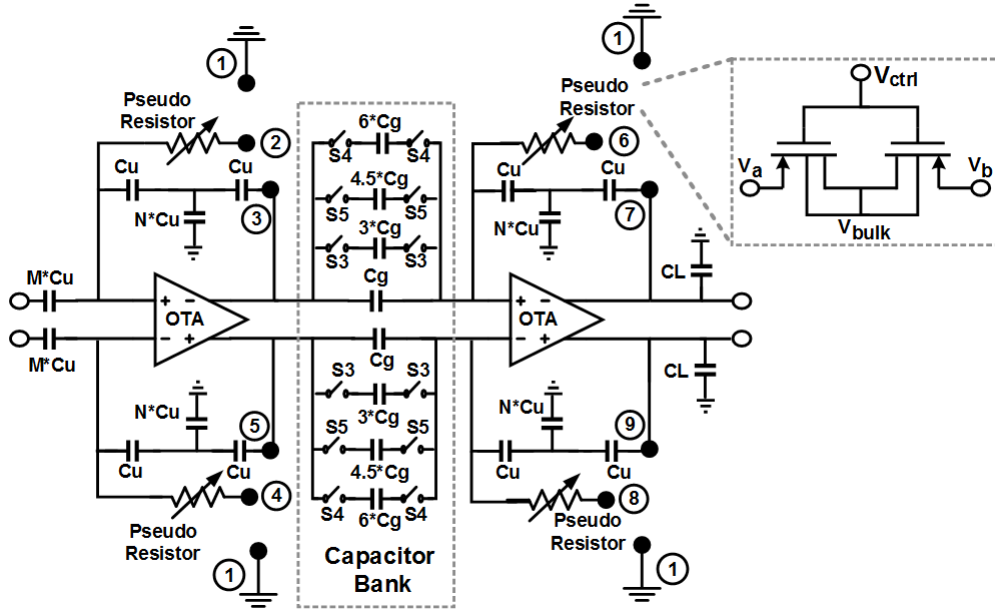


Figure 2.5: Two stage capacitive coupled amplifier

The challenges for designing a biopotential readout front-end circuit can be summarized as follows: Due to the low frequency behavior of the signals, in-band noise of the readout is dominated by  $1/f$  noise. Moreover, the common-mode interference from the mains to the human body disturbs the biopotential signals [10], and there is the problem of electrode offset generated at the skin-electrode interface [11]. Therefore, in order to achieve signal extraction under these circumstances a readout front-end is needed with high CMRR, low-noise, and band-pass filter characteristics. Moreover, amplitude and bandwidth characteristics of biopotential signals vary for different biopotential signals, and different applications of these signals. Therefore, the front-end should have configurable gain and filter characteristics.

## 2.3 Pseudo-resistor

It is very difficult to generate large time constants with limited area constraints of on-chip circuit elements. The position of the high pass pole is not critical for the current application. It is enough if the pole lies between DC and lowest input frequency, which is around 1Hz for the current application [6].

Pseudo-resistors are used to emulate terra-ohm resistances to generate very low high pass cutoff frequencies in low area. We have used PMOS transistors in series, operating in deep depletion

region. It supports larger swings with lower distortion as compared to MOS-bipolar pseudo-resistors as reported by [6]. The resistance of the pseudo-resistor can be controlled by varying the gate voltage. The gate control voltage controls the charge density in the depletion region which in turn controls minority carrier diffusion current. This varied the resistance of the pseudo-resistor [6, 7].

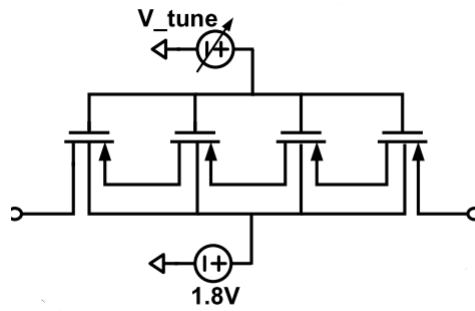


Figure 2.6: Pseudo resistor with resistance tuning

## Chapter 3

# The Instrumentation Amplifier

The purpose of a biopotential amplifier is to amplify the low amplitude biopotential signals amidst noise and large dc electrode offsets. The various challenges in designing a biopotential amplifier can be summarized as follows:

- High CMRR to reject common mode signals from 60 Hz AC lines.
- High pass and low pass filter characteristics to reject noise from various sources in the system.
- The amplifier should itself not add any significant noise to the signal passing through it.
- Ultra low power consumption/dissipation for efficient usage and long term power autonomy.
- Gain and bandwidth should be reconfigurable to accommodate different biopotential signals using the same hardware.

### 3.1 Instrumentation Amplifier Architectures

The instrumentation amplifier (IA) is the first stage of the analog front end. This stage is the dominating factor in deciding the noise of the whole system. The noise added by this stage is amplified by all the subsequent gain blocks. Fundamental requirements of bio potential sensing amplifiers are high linearity, baseline drift rejection, high CMRR, high PSRR and low noise efficiency factor (NEF). The design effort focuses on reducing the power of the circuit without compromising with other performance factors like the noise of the system.

Few well known IA architectures are:

- Three op-amp architecture

- Current balanced instrumentation amplifier
- Chopper modulated amplifiers

The CMRR of three opamp architecture is highly dependent on the matching of resistors which needs to be trimmed for precision. Moreover, the opamp should have a low output impedance stage to drive the resistors, thereby increasing the power dissipation of the opamp. In current balanced instrumentation amplifiers, the input stage is a transconductance amplifier converting the input voltage to current. This current is exactly mapped and passed through a trans resistance stage, and the resultant voltage is buffered to the output. The output voltage will be dependent on the input voltage according to the equation,

$$(V_{out+} - V_{out-}) = \frac{R_{(out)}}{R_{(in)}}(V_{(in+)} - V_{(in-)}) \quad (3.1)$$

Hence, this topology eliminates the need for matched transistors and high power opamps thereby overcoming the drawbacks of the previous architecture. However, the 1/f noise and process variations in the mosfets limit the low power and high CMRR capability of the circuit respectively.

Chopper modulated amplifiers can be used to reduce the 1/f noise and increase the CMRR. One of the main disadvantages of chopper coupled amplifier is the inherent DC coupling because of which the DC electrode offset between the two electrodes is amplified. High pass filters are used to remove the DC offset [1]. Theory behind chopper modulation is explained in next topic.

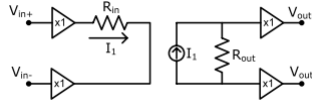


Figure 3.1: Current balanced instrumentation amplifier

### 3.1.1 Chopper Modulation

The basic principle of chopper modulation is used to remove low frequency noise, the main source of noise affecting the low frequency biopotential signals. In chopper modulated amplifiers, the input signals is modulated to a higher frequency with a square wave modulation signal. This modulated signal is amplified by the amplifier along with low frequency noise, at the input the input of the amplifier. The amplified signal is de-modulated again using the same square wave signal at the output of the amplifier. Thus, the amplified input signal is demodulated to lower frequency keeping noise at the higher frequency . The noise at this higher frequency can be filtered out using a low pass

filter. The chopper amplifier also increases the CMRR because the input modulator is transparent to the common mode signals. The common mode signals are amplified differentially by the amplifier. This differential output signal is modulated to a higher frequency by the output modulator which can be easily filtered out using a low pass filter, thereby removing the common mode noise. This is similar to removal of low frequency noise [12–14].

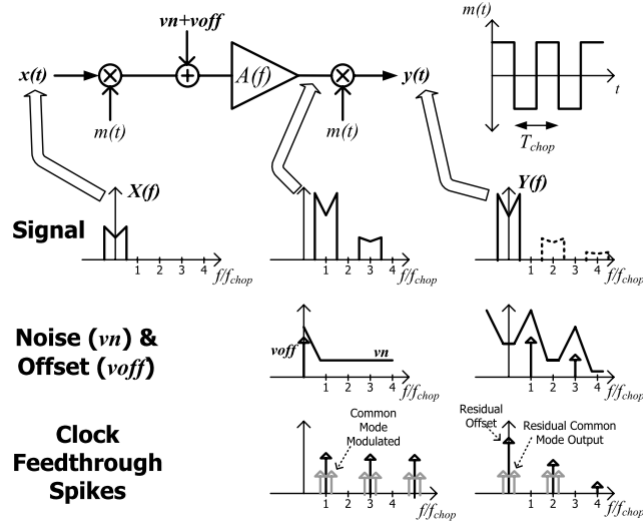


Figure 3.2: Concept of chopper modulation

### 3.2 Capacitive Coupled two stage Amplifier

The most obvious advantage of the two stage capacitive coupled amplifier is the low power consumption by the overall circuit. This two stage amplifier gives all four functionality expected from the analog front end, viz. bandpass filtering, gain tuning and bandwidth tuning. We have used recycled folded cascode architecture for the operational transconductance amplifier (OTA). This OTA gives the better performance than folded cascode OTA while consuming same amount of power. This can be attributed to the current reuse technique in the OTA. In normal folded cascode the two current source transistors function only to carry the current of both folding branch and the input transistors. In recycled folded cascode the current flowing through these transistors is recycled back so that they contribute to the overall transconductance ( $G_m$ ) of the circuit [15–18]. Transconductance of input transistors plays an important role in minimizing input referred noise. However in low power design, it is not plausible to boost the transconductance by increasing the current. Recycling folded cascode technique is used to double the transconductance for the same current consumption. The bottom

two transistors are sized in the ratio  $K:1$ . The overall transconductance then becomes  $(K-1)$  times the  $G_m$  of input transistors. This corresponds to a higher gain and bandwidth when compared to a normal folded cascode. To minimize flicker noise of the OTA, PMOS input pair is used. NMOS input pair with large gate area can be used, but large input capacitance degrades the overall bandwidth. Also, the low slew rate property combined with other characteristics of transistors operating in weak inversion region, viz., high current efficiency, high output voltage range have favoured the use of weak inversion transistor operation [7]. Moreover, the extremely low current aids in keeping the device dimensions as less as possible. Gain boosting architecture is used to increase the output impedance and hence, gain of the amplifier. This further improves the linearity of the system essential for the application in hand. The common mode feedback circuit consists of a resistive averaging circuit followed by an error amplifier to effectively balance the output common mode by varying the current of the pmos transistors. The error amplifier is a simple differential amplifier with transistors operating in subthreshold region.

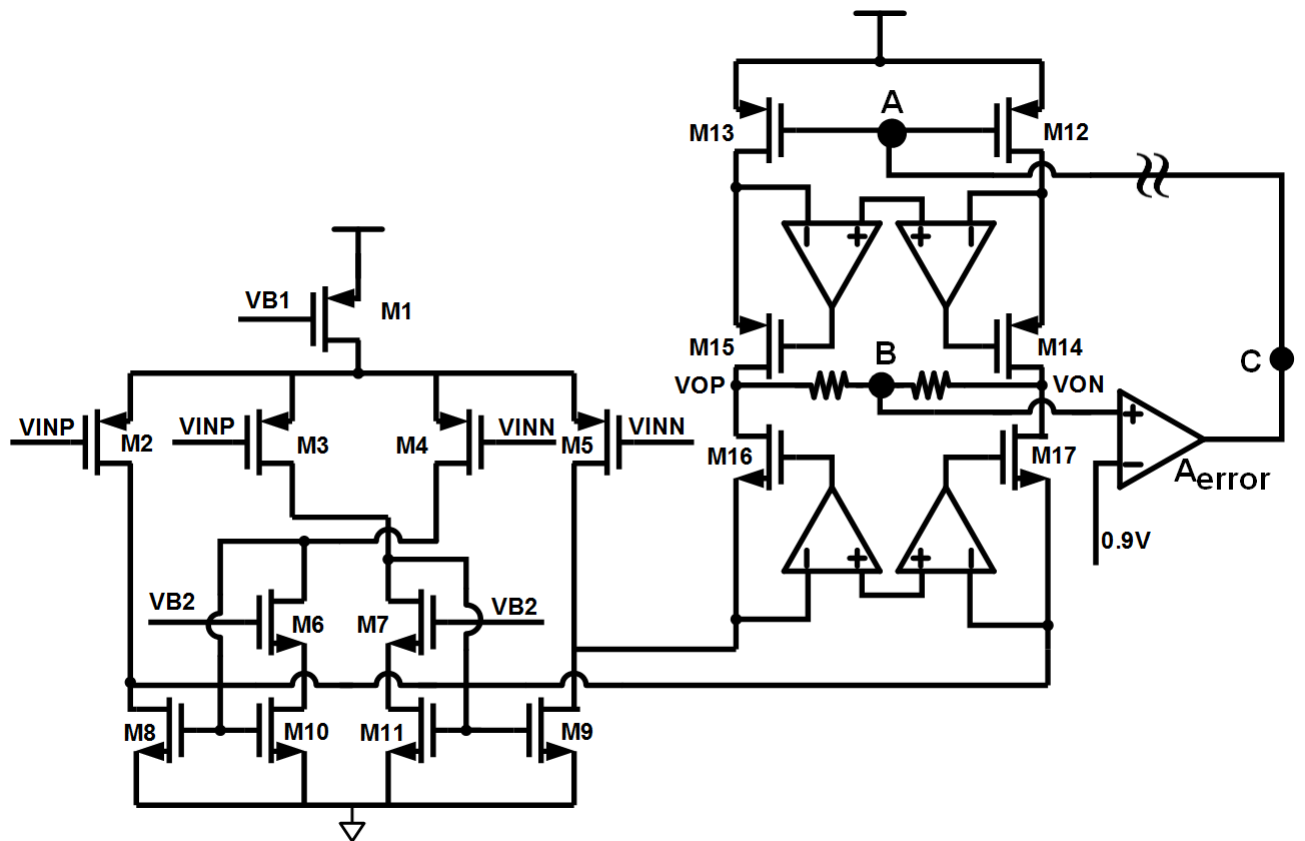


Figure 3.3: Recyclic folded cascode OTA with gain boosting

The transistor dimensions are given in 3.1.



Table 3.1: OTA transistor dimensions from Fig. 3.3

Transistor	Length( $\mu\text{m}$ )	Width( $\mu\text{m}$ )
M1	0.25	1.5x5
M2	0.25	1.5x1.65
M3	0.25	1.5x1.65
M4	0.25	1.5x1.65
M5	0.25	1.5x1.65
M6	1	1.5x4.21
M7	1	1.5x4.21
M8	1	1.5x5.7
M9	1	1.5x5.7
M10	1	1.5x2.28
M11	1	1.5x2.28
M12	1	1.5x8.39
M13	1	1.5x8.39
M14	1	1.5x8.32
M15	1	1.5x8.32
M16	1	1.5x6.43
M17	1	1.5x6.43

Table 3.2: NMOS Gain boosting amplifier Transistor Sizes from Fig. 3.5

Transistor	Length( $\mu\text{m}$ )	Width( $\mu\text{m}$ )
M1	10	2.18
M2	1	15.44
M3	1	15.44
M4	1	12.85
M5	1	12.85
M6	1	0.24
M7	1	0.24
M8	0.27	4.59
M9	0.27	4.59
M10	1	1.06
M11	1	1.06
M12	10	0.45
M13	10	0.45

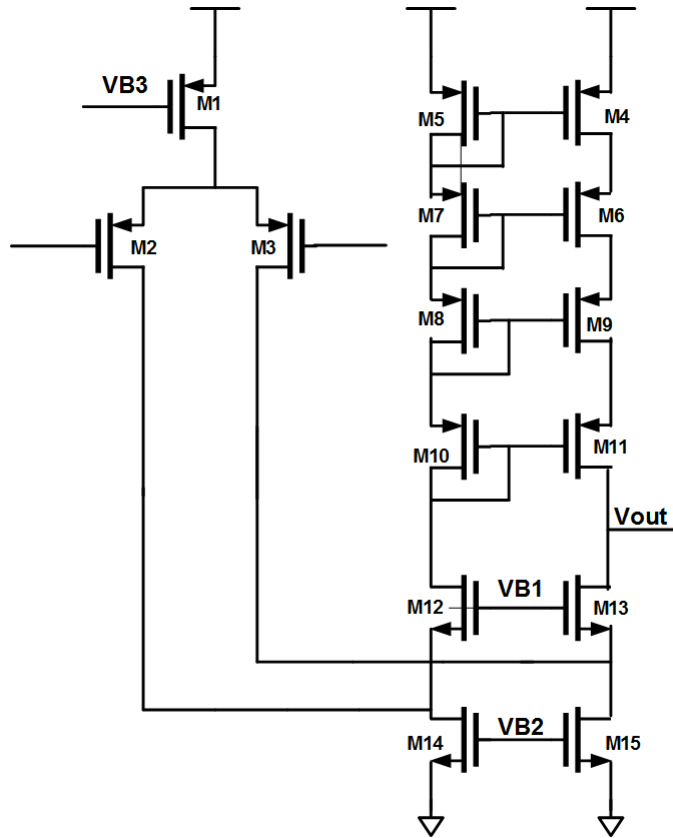


Figure 3.4: PMOS folded cascode OTA

### 3.3 Summary

In this chapter we focused on different types of instrumentation amplifiers with their respective pros and cons. Various challenges encountered while designing the biopotential amplifier was discussed. The low power two stage amplifier architecture was discussed in detail along with the recyclic folded cascode OTA architecture. The amplifier can be further modified for high linearity and low noise performance by increasing the current. Thus, power - noise performance trade off was identified and suggested for modification in future.

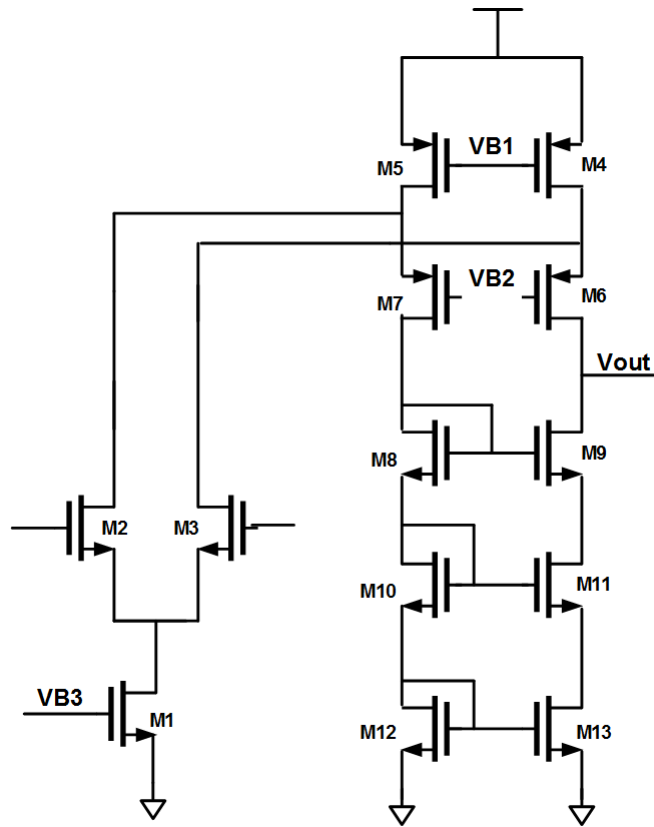


Figure 3.5: NMOS folded cascode OTA

Table 3.3: PMOS Gain boosting amplifier Transistor Sizes from Fig. 3.4

Transistor	Length(um)	Width(um)
M1	1	12
M2	0.5	10.9
M3	0.5	10.9
M4	1	0.68
M5	1	0.68
M6	0.97	0.67
M7	0.97	0.67
M8	1	0.68
M9	1	0.68
M10	1	6.49
M11	1	6.49
M12	13.85	0.96
M13	13.85	0.96
M14	9.72	0.83
M15	9.72	0.83

## Chapter 4

# Automatic Gain Control

For maximum signal to noise ratio(SNR), an amplitude of 200mV<sub>p-p</sub> is desired at the input of the sigma delta analog to digital converter(ADC). Power hungry and large area occupying digital signal processors (DSPs) were previously being used for this purpose. To meet the low power specifications and functionality of automatic gain variation, a custom digital circuit is introduced in this chapter. Various building blocks have been discussed in the sections below. Also, a novel analog classifier scheme has been discussed. This classifier distinguishes normal ECG from abnormal ecg signal and reduces the power consumed for processing in the subsequent blocks.

### 4.1 Peak Detector

Fig. 4.2 shows the peak detector circuit with sense amplifiers [19]. The peak detector circuit consists of a low power single ended folded cascode operational transconductance amplifier (OTA) with its transistors operating in weak inversion region. A voltage range between 0.93V and 1.05V is optimum for getting maximum SNR from the sigma-delta ADC. The threshold voltages of the inverters are set such that they detect these two voltage levels. Fig. 4.2 also shows the different input logic levels and the corresponding decision taken by subsequent blocks.

Also, in the case of an ECG the time difference between two R peaks is around 1 second. Hence, the peak detector is designed such that its total discharge time is higher than the time duration between two R peaks. Here the discharge time is kept greater than 1s to prevent the digital control logic from varying the gain during low amplitude peaks (P,Q,T) of the ECG signal [23]. In the proposed circuit, the peak detectors output drops by only 22.5mV in half a second. A voltage range between 0.93V and 1.05V is determined to be the optimum input level for the ADC.

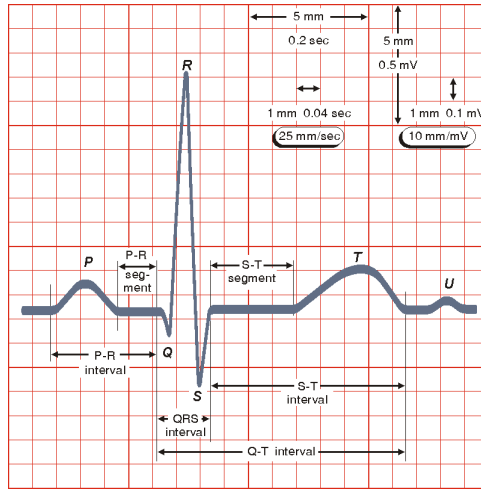


Figure 4.1: ECG signal characteristics

Therefore, the inverters of the voltage level detector are sized such that the top inverter in Fig. 4.2 outputs a logical 1 only when its input is lesser than 1.05V, while the other outputs a logical 1 only if its input is lesser or equal to 0.93V. Therefore, the output of the level detector can be represented digitally as 00 10 or 11 if its input is greater than, within or lesser than the desired level respectively. Finally, the subsequent digital logic is programmed such that it decreases (increases) the gain if the output of the level detector is 00 ( 11 ). It is designed so as to generate control signals, viz. S3, S4 and S5, which select the appropriate number of capacitors from the capacitor bank in the AFE (see Fig. 2.5). As soon as the level detectors output equals 10 a control signal S1(see Fig. 2.1) is generated which activates the path between AFE and ADC, turns the ADC on, and turns off the AGC.

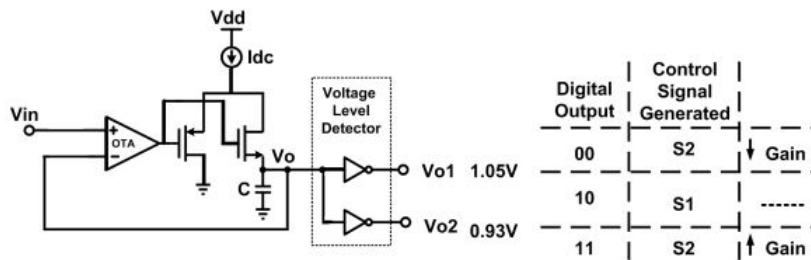


Figure 4.2: Peak detector with sense amplifiers. Here,  $C=30\text{pF}$  and  $I_{dc}=92\text{pA}$

Table 4.1: Output codes of AGC Block with their corresponding Normalized Gain values

Output Codes(S2)			Normalized Gain
G3	G2	G1	
0	0	0	1
0	0	1	3
0	1	0	4
1	0	0	5
0	1	1	6
1	0	1	7
1	1	0	8
1	1	1	10

## 4.2 Digital State Machine for Automatic Gain Control

The output of the peak detector is given to a custom digital logic, which increments or decrements the previous gain setting code depending on the input it receives as shown in Fig.2.1. The output of this block is connected to a decoder which decodes the input BCD code to the relevant binary code for setting the switches as shown in Table 4.1. A simple digital logic has also been designed which checks the level detector sense amplifier outputs for 10 code and fixes the current gain value without further switching. Hence, switching happens only at certain intervals periodically, thus saving power and turns ON the ADC only when the proper amplitude is reached at the input (which is, 200mV<sub>p-p</sub>).

## 4.3 AGC as Analog Classifier

In conventional signal acquisition systems, a digital classifier is used post analog-digital converter(ADC) for identification of abnormal ecg signals to save power in the subsequent signal processing blocks. One of the important characteristics of an abnormal ecg signal can be seen in the form of abrupt changes in its amplitude. Taking advantage of this feature of the signal, a novel analog classification scheme has been designed. The advantage of signal classification in the analog front end stage is twofold viz., a first order sigma delta ADC can be used for digitizing the abnormal signal instead of a second order sigma delta ADC, significantly reducing the power consumption of the overall system. Moreover, reusing the same automatic gain control circuit (AGC), previously used for setting the gain in PGA, can be used for this purpose. This further saves the power and area penalty of a separate circuit.

The AGC consists of a peak detector, followed by two inverters as sense amplifiers and a custom digital circuit for setting the gain switches. The digital circuit is a Mealy machine getting two bit

input from the sense amplifiers. Based on these inputs and the previous state, the next gain setting will be decided. This state machine increments the gain in ascending order with unit gain steps. The output of peak detector discharges with time to accommodate next peak. This discharge time is set to be around 1 second, the approximate duration between two R peaks in an ECG. During normal ECG operation, the gain is incremented in unit steps from the initial minimum value. The gain value is fixed once the peak detector output settles within  $100mV_{peak}$  amplitude. If an abnormal peak arrives after the gain value is fixed, the gain would follow increment-decrement sequence before settling to a single value. The number of these increment-decrement sequences will be counted by a counter, thereby generating a trigger signal once the required number is reached. This number is set to be greater than 2 to account for any misinterpretation of normal signal.

As the input amplitude is very less, even for an abnormal signal, some gain is required to get a proper signal to noise ratio at the ADC input. Also, the gain shouldn't be too high to saturate the subsequent blocks. Hence, the gain for such signals is set to the middle value of the maximum gain setting. While processing normal ECG signals, the output codes of this block increment the gain in unit steps as shown in Table 4.1 .

While processing abnormal signals with varying amplitudes, the gain steps vary without following the above mentioned sequence. This variation is captured by one more state machine which takes the output codes and peak detector bits as input and increments a counter whenever the correct sequence is missed. When the counter output becomes 2, indicating an abnormal signal, the predefined mid-gain is fixed.

### 4.3.1 Algorithm of state machine for analog classification

Output of automatic gain control circuit is compared with its previous value. The previous value is obtained by storing the output in a register.

If the current value is greater than or equal to previous value, the same sequence continues; else, the counter is incremented by 1. The cycle continues until the counter value becomes 2. If the output of counter is greater than or equal to 2, then the gain is set to 5, else the output of the AGC sets the gain of the front end.

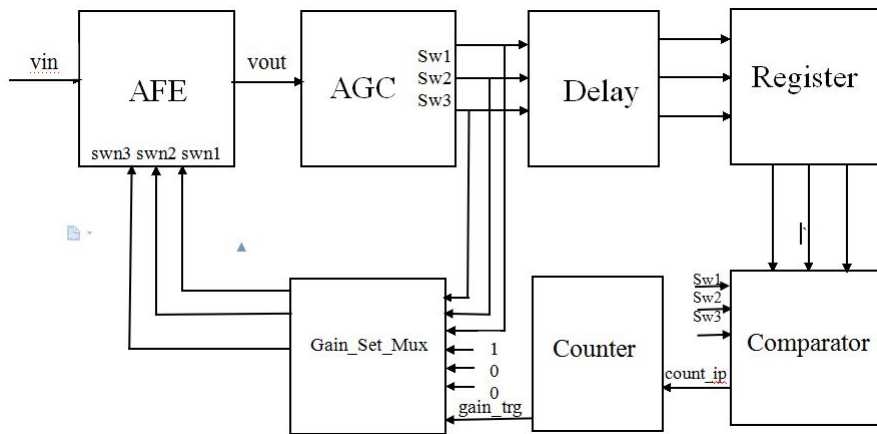


Figure 4.3: Block diagram of AGC used as an analog classifier



## Chapter 5

# Conclusion and future work

### 5.1 Simulation results of analog front end

This section presents simulation results of the analog front end, except that of the ADC. The AC response plots of the two stage amplifier stage with bandwidth tunability is plotted in Fig. 5.1. The maximum gain of the afe is 60dB and the high pas cutoff can be varied from 100mHz to 10Hz by varying the pseudo resistor gate voltage from 0.7V to 1.4V. Fig. 5.3 and Fig. 5.2 show the dft plots of signals with two sets of amplitudes. Spurious free dynamic range reduces slightly when the input amplitude is high because of the inherent non-linearity of the amplifier output. The last three plots show the overall functionality of the whole system.

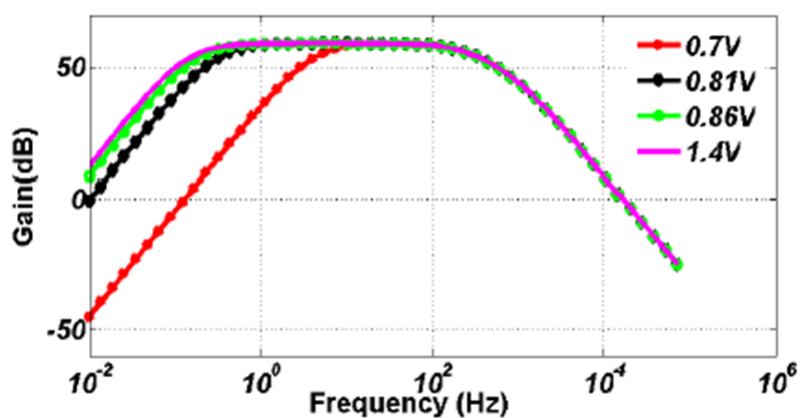


Figure 5.1: Tunable Bandwidth of ECG

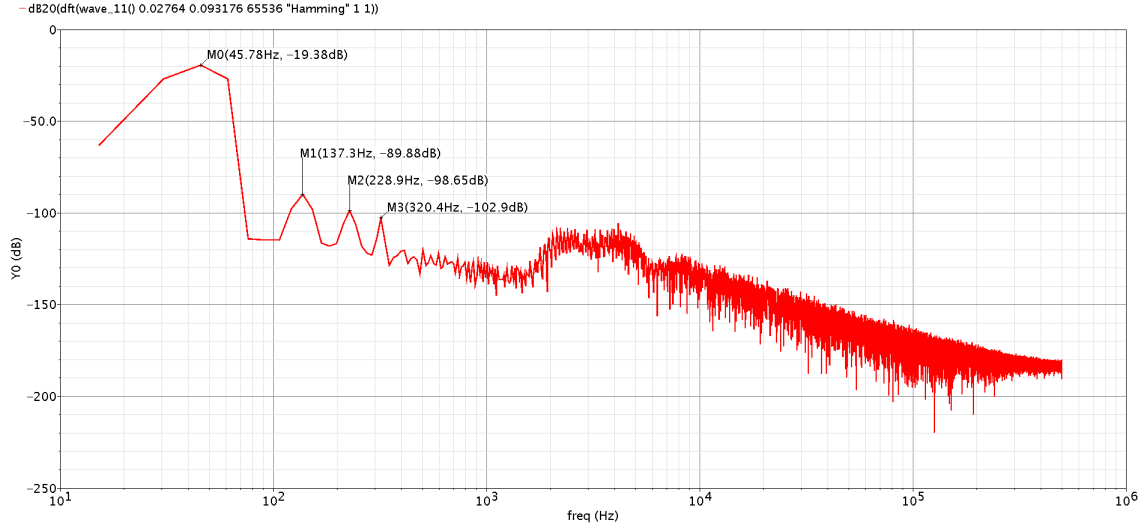


Figure 5.2: FFT plot of AFE output with input of  $1mV$  amplitude

Table 5.1: Comparison Table

Parameter	Value				
	This work	[20]	[21]	[22]	[23]
Technology (m)	0.18	0.18	0.35	0.35	0.18
Voltage Supply (V)	1.8	1.3-1.8	2.5	1	1
Power Consumption (W)	0.47	0.884	0.62	0.9	0.8
CMRR (dB)	110	90	70	71.2	60
DC Gain (dB)	40-60	20-43.2	40.7	45.6-60	34
Bandwidth (Hz)	0.25-250	1-130	5m-200	4.5m-290	0.2-5.8k
NEF	4.4	$4.9\mu V_{rms}$	1.96	3.26	2.79

## 5.2 Future Work

Comparison of this work with previous publication has been shown in Table 5.1

Current work can be continued to reduce the power further without compromising with the noise numbers. A new architecture of amplifier and the whole system would be beneficial in this direction. Further, the system can be generalised to accept and process all kinds of biopotential signals for classification. For this, research needs to be done on the characteristics of all the signals instead of mere amplitude and frequency characteristics. That would lead to identification of unique features distinguishing one signal from the other.

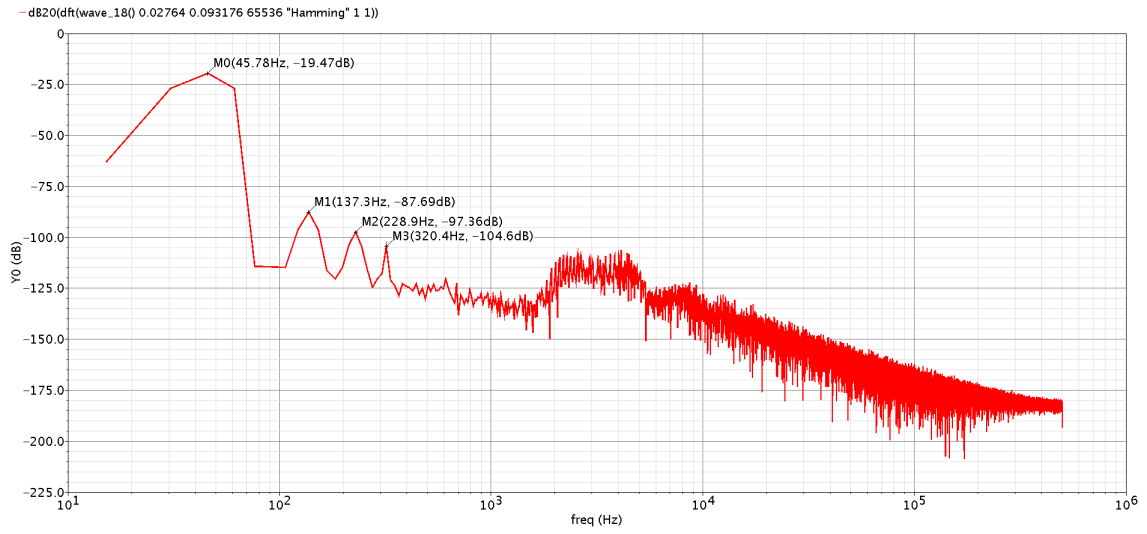


Figure 5.3: FFT plot of AFE output with input of 100uV amplitude

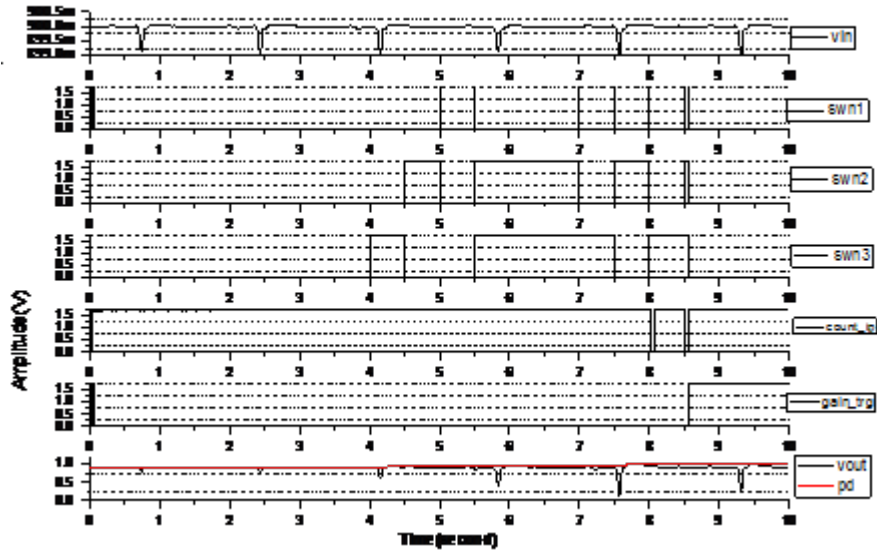


Figure 5.4: Outputs at various stages of AGC with abnormal ECG input

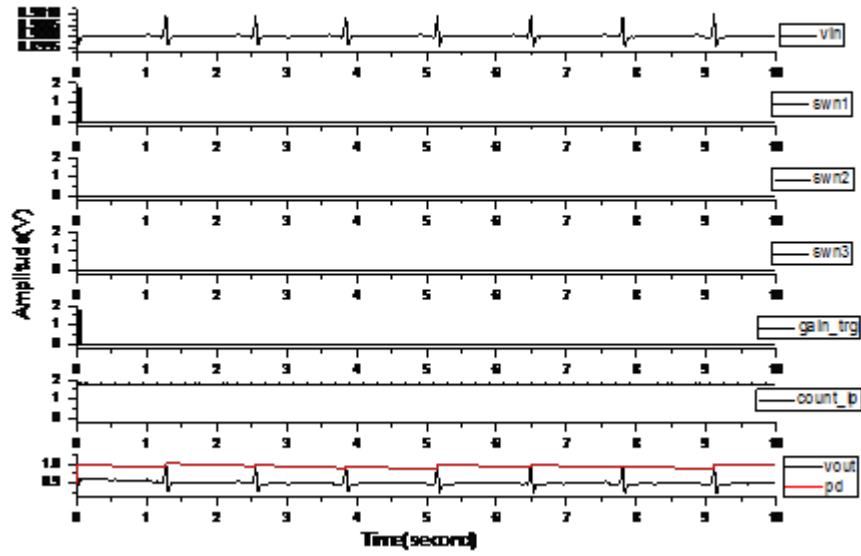


Figure 5.5: Outputs at various stages of AGC with 1mV ECG input

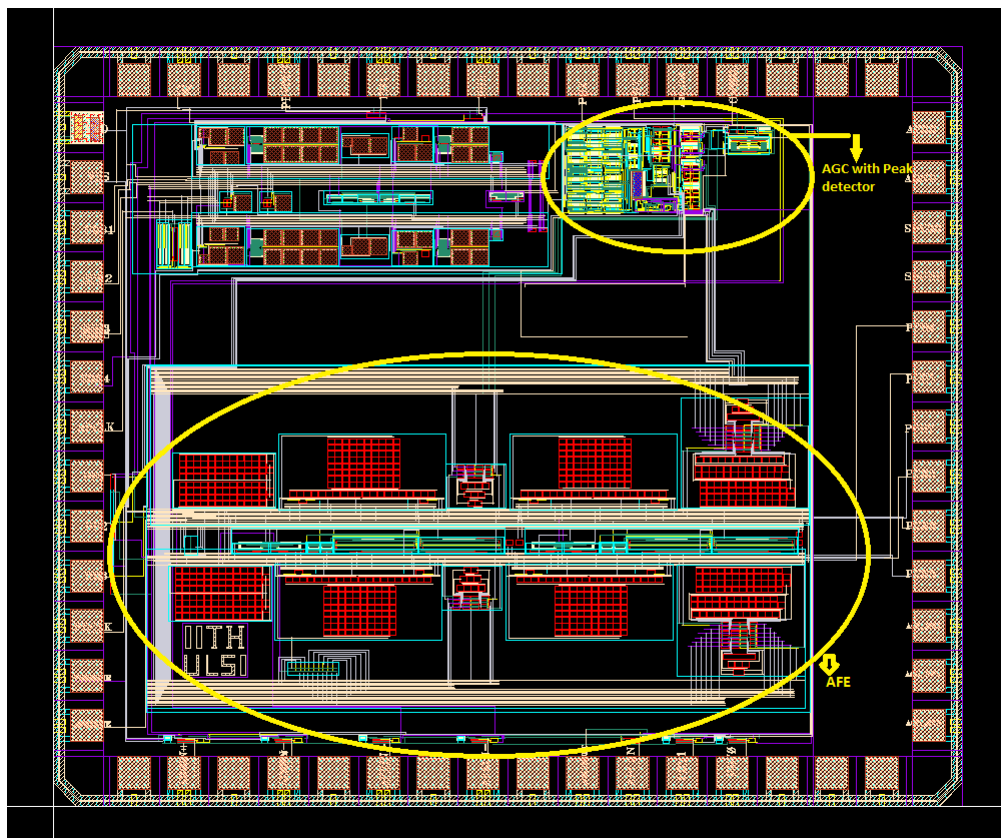


Figure 5.6: Layout of biopotential front end with ADC

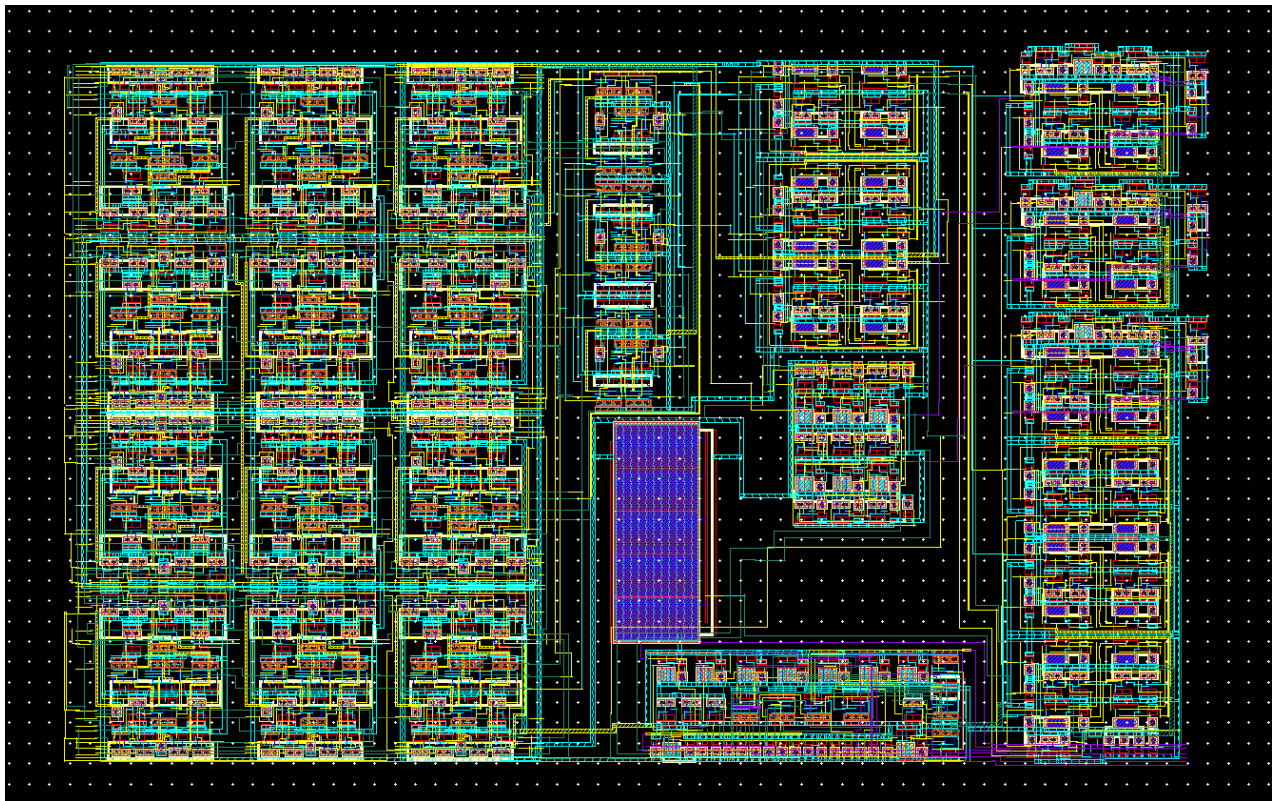


Figure 5.7: Layout of Custom automatic gain control circuit

# References

- [1] R. F. Yazicioglu, C. van Hoof, and R. Puers. Biopotential Readout Circuits for Portable Acquisition Systems. 1st edition. Springer Netherlands, 2009.
- [2] N. Thakor. Biopotentials and Electrophysiology Measurement. CRC Press, 1999.
- [3] R. Harrison. The Design of Integrated Circuits to Observe Brain Activity. *Proceedings of the IEEE* 96, (2008) 1203–1216.
- [4] W. H. Organization. World Health Statistics 2012. WHO Press, World Health Organization, 20 Avenue Appia, 1211 Geneva 27, Switzerland, 2012.
- [5] M. Steyaert and W. Sansen. A micropower low-noise monolithic instrumentation amplifier for medical purposes. *Solid-State Circuits, IEEE Journal of* 22, (1987) 1163–1168.
- [6] V. Chaturvedi. Low Power and Low Area Techniques For Neural Recording Application. Ph.D. thesis, Indian Institute of Science 2013.
- [7] R. Harrison and C. Charles. A low-power low-noise CMOS amplifier for neural recording applications. *Solid-State Circuits, IEEE Journal of* 38, (2003) 958–965.
- [8] P. Cong, N. Chaimanonart, W. Ko, and D. Young. A Wireless and Batteryless 10-Bit Implantable Blood Pressure Sensing Microsystem With Adaptive RF Powering for Real-Time Laboratory Mice Monitoring. *Solid-State Circuits, IEEE Journal of* 44, (2009) 3631–3644.
- [9] A. P. Chandrakasan, N. Verma, and D. C. Daly. Ultralow-Power Electronics for Biomedical Applications. *Annual Review of Biomedical Engineering* 10, (2008) 247–274. PMID: 18647116.
- [10] H. Kim, S. Kim, N. Van Helleputte, A. Artes, M. Konijnenburg, J. Huisken, C. Van Hoof, and R. Yazicioglu. A Configurable and Low-Power Mixed Signal SoC for Portable ECG Monitoring Applications. *Biomedical Circuits and Systems, IEEE Transactions on* 8, (2014) 257–267.

- [11] K. Ng and Y. P. Xu. A Compact, Low Input Capacitance Neural Recording Amplifier. *Biomedical Circuits and Systems, IEEE Transactions on* 7, (2013) 610–620.
- [12] A. Said. Design of a Chopper Amplifier for Use in Biomedical Signal Acquisition. Engineering, Southern Illinois University Edwardsville, 2010.
- [13] D. Han, Y. Zheng, and M. Je. A 0.18  $\mu\text{m}$  front end for ECG/EEG/neural sensor interface. In Radio-Frequency Integration Technology (RFIT), 2012 IEEE International Symposium on. 2012 107–109.
- [14] T. Denison, K. Consoer, A. Kelly, A. Hachenburg, and W. Santa. A 2.2  $\mu\text{W}$  94nV/Hz, Chopper-Stabilized Instrumentation Amplifier for EEG Detection in Chronic Implants. In Solid-State Circuits Conference, 2007. ISSCC 2007. Digest of Technical Papers. IEEE International. 2007 162–594.
- [15] R. Assaad and J. Silva-Martinez. The Recycling Folded Cascode: A General Enhancement of the Folded Cascode Amplifier. *Solid-State Circuits, IEEE Journal of* 44, (2009) 2535–2542.
- [16] P. Patra, S. Kumaravel, and B. Venkatramani. An enhanced fully differential Recyclic Folded Cascode OTA. In Systems, Signals and Devices (SSD), 2012 9th International Multi-Conference on. 2012 1–5.
- [17] P. Patra, P. Jha, and A. Dutta. An enhanced recycling folded cascade OTA with a positive feedback. In Microelectronics and Electronics (PrimeAsia), 2013 IEEE Asia Pacific Conference on Postgraduate Research in. 2013 153–157.
- [18] Y. Li, K. Han, X. Tan, N. Yan, and H. Min. Transconductance enhancement method for operational transconductance amplifiers. *Electronics Letters* 46, (2010) 1321–1323.
- [19] Y.-C. Su, S.-Y. Lee, and A.-P. Lin. A 0.6-V 1.8  $\mu\text{W}$  automatic gain control circuit for digital hearing aid. In Circuits and Systems, 2008. APCCAS 2008. IEEE Asia Pacific Conference on. 2008 113–116.
- [20] L. Yan, P. Harpe, M. Osawa, Y. Harada, K. Tamiya, C. Van Hoof, and R. Yazicioglu. 24.4 A 680nA fully integrated implantable ECG-acquisition IC with analog feature extraction. In Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014 IEEE International. 2014 418–419.

- [21] T.-Y. Wang, M.-R. Lai, C. Twigg, and S.-Y. Peng. A Fully Reconfigurable Low-Noise Biopotential Sensing Amplifier With 1.96 Noise Efficiency Factor. *Biomedical Circuits and Systems, IEEE Transactions on* 8, (2014) 411–422.
- [22] X. Zou, X. Xu, L. Yao, and Y. Lian. A 1-V 450-nW Fully Integrated Programmable Biomedical Sensor Interface Chip. *Solid-State Circuits, IEEE Journal of* 44, (2009) 1067–1077.
- [23] L. Liu, X. Zou, W. Goh, R. Ramamoorthy, G. Dawe, and M. Je. 800 nW 43 nVHz neural recording amplifier with enhanced noise efficiency factor. *Electronics Letters* 48, (2012) 479–480.