

Sub 1V Charge Pump based Micro Scale Energy Harvesting for Low Power Application

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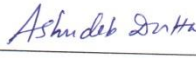
This thesis entitled "Sub 1V Charge Pump Based Micro Scale Energy Harvesting for Low Power Application" by Akash Kumar Gupta is approved for the degree of Master of Technology from IIT Hyderabad.



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Abstract

Harvesting energy from our environment is a promising solution to provide power to wireless sensor network, wearable devices and biomedical implantation. Now a days, usage of battery power system has disappeared because of replacement issues, installation costs every periodic year and the possibility of health hazard in the case of biomedical implants. Considering these issues, energy harvesting proves to be the most feasible and convenient option in the case of wearable devices and biomedical implantation. Hence, we have focused on indoor single solar cell energy harvesting to power ultra-low power load. The tree topology DC-DC converter is used for power management circuit with optimized efficiency. High efficiency is achieved by using ZVT-MOSCAP. The power management circuit includes DC-DC converter and feed forward maximum power point tracking algorithm to transfer maximum power from the single solar cell. The system has ultra-low power battery protection and input condition sensor circuit to extend the life of the battery by protecting from overcharging and over discharging. Also, cold startup circuit is used to run the system when battery voltage drains out to zero. The objective of this system to make complete energy harvester unit is to drive wide range of ultra-low power applications. We have driven the ZigBee receiver to validate our system and the system works effectively.

Nomenclature

WSN	Wireless Sensor Network
PMC	Power Management Circuit
PV Cell	Photo Voltaic Cell
SC	Short Circuit
OC	Open Circuit
MPPT	Maximum Power Point tracking
SCCP	Switched Capacitor Charge pump
VCO	Voltage Controlled Oscillator
BM	Battery Management
LDO	Low Dropout Regulator
CP	Charge pump
MIMCAP	Metal Insulator Metal Capacitor
ZVT-MOS	Zero Threshold MOS Capacitor
ICS	Input Condition Sensor
EMI	Electromagnetic Interference
DC	Direct Current

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Chapter 1

Introduction

1.1 Motivation

Our immediate surroundings have abundance of energy sources. Energy Harvesting is a physical process by which energy is collected from our surroundings and converted into electrical energy. Some examples of such energy sources include solar, thermal gradient, vibration, electromagnetic wave, and wind. Harvesting energy from these sources is very attractive and feasible to power the low power electronic devices, particularly wearable and embedded wireless sensor network as well as biomedical devices where battery replacement is impractical [1].

Nowadays advances in computing, communication and integration have resulted in the emergence of a new era of ultra-low power application. An example of such a system is the wearable and implantable biomedical device [1]. These systems require to work from several months to years without battery replacement because battery replacement is infeasible. In case of biomedical implants like pacemaker the, battery should be replaced in every eight years hence, surgery needs to be done each time. This can lead to life threatening issues if hazardous chemicals of depleted battery spread during surgery [2]. For large number of micro sensors that spatially spread across our surroundings, it is impossible to replace battery in every year or in decades because of the expense and non- feasibility. Focusing on these challenges in our mind, we implemented self-power energy harvester unit that helps to run the system without any issues for longer time. However, the voltage generated by these energy harvester (Table 1.1) is in the range of a few mV to a couple of hundreds mV.

1.1.1 Review of various ambient sources [3]

Table 1.1 Energy Harvesting Estimates

Energy Source	Harvested Power
Vibration/Motion	
Human	4 $\mu\text{W}/\text{cm}^2$
Industry	100 $\mu\text{W}/\text{cm}^2$
Temperature Difference	
Human	25 $\mu\text{W}/\text{cm}^2$
Industry	1–10 mW/cm^2
Light	
Indoor	10 $\mu\text{W}/\text{cm}^2$
Outdoor	10 mW/cm^2
RF	
GSM	0.1 $\mu\text{W}/\text{cm}^2$
Wi-Fi	0.001 $\mu\text{W}/\text{cm}^2$

This voltage has to up convert with the help of power converter to supply for electronics devices. This power converter circuit, implemented with CMOS devices have higher threshold voltage (350mV-500mV) in UMC 180nm technology which is still higher than the voltage generated by the energy harvester. Therefore the key challenge is to implement CMOS based power converter, startup circuit as well as controller unit at this voltage level.

1.1.2 Application of Energy Harvesting & Their Power Level [4]

Table 1.2 Selected battery-operated systems

Application	Power	Energy source buffer
Pacemaker and cardioverter defibrillator	<10 μW	10-year lifetime battery
Hearing aid	100–2000 μW	1-week lifetime rechargeable battery
Analog cochlear processor	200 μW	1-week lifetime rechargeable battery
Neural recording	1–10 mW	Inductive power
Body-area monitoring	140 μW	Battery

1.2 Challenges in Energy Harvesting: Single Solar Perspective

For indoor application, power extraction from single solar cell is in the range of a few μW to mW. Scavenging optimum power from this transducer is a big challenge because we need to design the system with a harvester having low dissipation power. Harvesting power should always be greater than the power consumption by harvester circuit. A typical energy harvesting system has three blocks: transducer, power management circuit (PMC) and storage buffer. PMC circuits are used to rectify the output voltage of transducer and if necessary, to regulate the output voltage at desired level and store in a battery or super capacitor [5]. The core part of PMC is a DC-DC converter and the prerequisite for PMC is to maximize the net energy harvested by -

- Transferring maximum power from source to storage buffer
- Minimum power dissipation across converter as well as the clock generation circuit and drivers

The meeting of the two requirements needs a trade-off in PMC design for small scale EH. To transfer the maximum power, the load impedance should match the source impedance, and the source impedance changes as operating conditions changes [6]. The match between the source and load are accomplished using maximum power point tracking (MPPT), which dynamically adjusts the load impedance (or the load voltage for photovoltaic cells) and specifically, the input impedance of the DC/DC converter. To minimize the power dissipation of a PMC, one needs to select an MPPT algorithm judiciously by considering the type of transducer, the amount of energy available, and its application. For example, employment of a sophisticated MPPT algorithm harvests more energy from the energy source, but the PMC dissipates more power to execute the MPPT algorithm. Another rather unique problem of PMCs for EH application is the cold startup circuit [5]. A PMC is typically powered by the storage device of an EH system, as the storage voltage is regulated. When the storage is drained completely, the PMC fails to start. Two solutions are feasible; one is to provide a dedicated backup battery for cold startup circuit, and the other one, to use the source power to start. Both approaches have pros and cons. But the second one is the better option for wearable and biomedical application of light weight and of smaller size [2]. A PMC for EH should be able to harvest energy from a low input voltage and should have low standby power dissipation, and desirably a battery protection circuit.

The above issue is the generic problem of energy harvester. The problems respective to single solar cell is the designing of PMC, battery protection and cold startup circuit. So we have to

maintain high efficiency as well as lower power dissipation across these blocks. Single solar cell perspective's another constraint is area, that is, implementing PMC, startup and other interface circuit with minimum area as well as on the chip. Implementing on chip PMC with higher efficiency and minimum loss is a big challenge for single solar cell because it has very low voltage level.

1.3 Solar Cell Modeling: Single Solar (I-V) Characteristics Respective to Illumination

1.3.1 Solar Cell Ideal Model

The solar cells are semiconductor with a p-n junction fabricated in a thin wafer or layer of semiconductors. When exposed to light, a photo current proportional to the solar radiation is generated if the photon energy is greater than the band gap. In the dark, the I-V characteristics of a solar cell have an exponential characteristic similar to that of a diode [6].

The ideal equivalent circuit of a solar cell is a current source in parallel with a single-diode. The configuration of the simulated ideal solar cell with single-diode is shown in Figure 1.1.

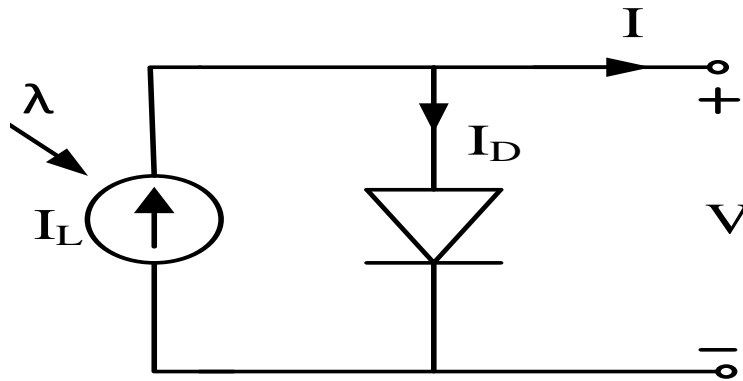


Figure 1.1 Ideal solar cell with single-diode

In Figure 1.1, λ is the solar radiance, I_L is the photo generated current, I_D is the diode current, I is the output current, and V is the terminal voltage. The I-V characteristics of the ideal solar cell with single diode are given by

$$I = I_L - I_D \tag{1}$$

I = output current (ampere)

I_L = photo generated current (ampere)

I_D = diode current (ampere)

$$I = I_L - I_o \left(e^{qV/\eta KT} - 1 \right) \quad (2)$$

Where I_o is the diode reverse bias saturation current, q is the electron charge, m is the diode ideality factor, k is the Boltzmann's constant, and T is the cell temperature. A solar cell can at least be characterized by the short circuit current I_{SC} , the open circuit voltage V_{OC} , and the diode ideality factor m . For the same irradiance and p-n junction temperature conditions, the short circuit current I_{SC} , it is the greatest value of the current generated by the cell. The short circuit current I_{SC} is given by:

$$I_{SC} = I_L = I \quad (3)$$

For the same irradiance and p-n junction temperature conditions, the open circuit voltage V_{OC} is the greatest value of the voltage at the cell terminals [7]. The open circuit voltage V_{OC} is given by:

$$V_{OC} = \frac{KT}{q} \ln \left(1 + \frac{I_{SC}}{I_o} \right), \text{ For } I = 0 \quad (4)$$

The output power is given by:

$$P = V \left[I_{SC} - I_o \left(e^{qV/\eta KT} - 1 \right) \right] \quad (5)$$

1.3.2 Solar cell with Series and Shunt Resistance [7]

The diode represents the P-N junction. (R_{SH}) represents the shunt resistor that models the leakage current at the junction; its value is usually high. (R_S) Represents the silicon ohmic contacts, the higher the (R_S) value is, the lower slope of the (I-V) curve is at the constant voltage region. Conversely, the lower the (R_{SH}) value is, the higher the slope of the (I-V) curve is at the constant current region.

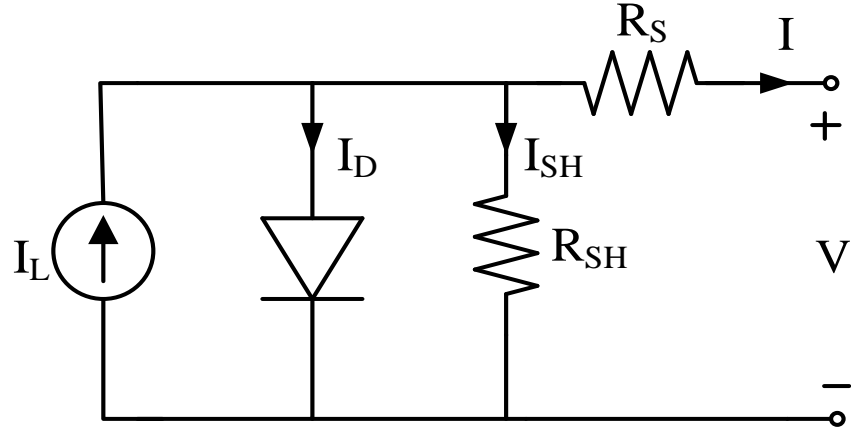


Figure 1.2 Solar cell with single-diode and series resistance.

$$I = I_L - I_D - I_{SH} \quad (6)$$

I_{SH} = shunt current (ampere)

The current through these elements is governed by the voltage across them

$$V_j = V + IR_S \quad (7)$$

V_j = voltage across both diode and resistor R_{SH} (volt)

V = voltage across the output terminals (volt)

I = output current (ampere)

R_S = series resistance (Ω)

$$I_{SH} = \frac{V_j}{R_{SH}} \quad (8)$$

R_{SH} = shunt resistance (Ω)

$$I = I_L - I_o \left(e^{qV/\eta KT} - 1 \right) - \frac{V + IR_S}{R_{SH}} \quad (9)$$

In case of unloaded solar cell, $I=0$, $V=V_{OC}$,

$$I_L = I_o \left(e^{qV_{OC}/\eta KT} - 1 \right) - \frac{V}{R_{SH}} \quad (10)$$

By substituting equation 10 in 9, and by ignoring R_S and R_{SH} , since R_S is very small and R_{SH} is very large, one could get:

$$I = I_o \left[\left(e^{qV_{oc}/\eta KT} \right) - \left(e^{qV/\eta KT} \right) \right] \quad (11)$$

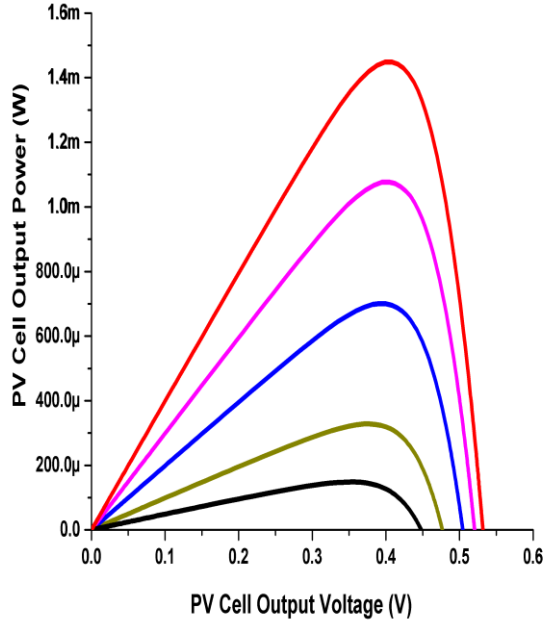


Figure 1.3 Output power vs. PV terminal voltage

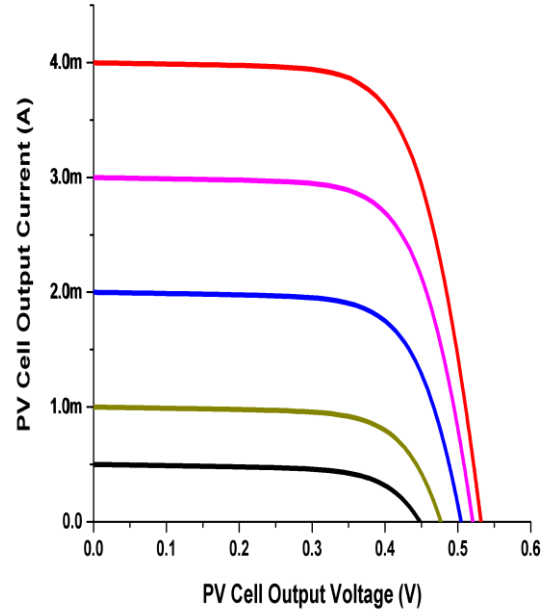


Figure 1.4 I-V characteristic of a PV module

The simulation is performed to plot IV and PV plot of single solar cell. The curves shown in Fig. 1.3 & Fig.1.4 correspond to different illumination. Different illumination level generates different I_L , so we choose I_L value from 0.5-4mA.

1.3.3 Effects of Physical Size [7]

The values of I_0 , R_S , and R_{SH} are dependent upon the physical size of the solar cell. In comparing otherwise identical cells, a cell with twice the surface area of another will, in principle, have double the I_0 because it has twice the junction area across which current can leak. It will also have half the R_S and R_{SH} because it has twice the cross-sectional area through which current can flow. For this reason, the characteristic equation is frequently written in terms of current density, or current produced per unit cell area:

$$J = J_L - J_o \left(e^{qV/\eta KT} - 1 \right) - \frac{V + Jr_S}{r_{SH}} \quad (14)$$

Where,

J = current density (ampere/cm²)

J_L = photo generated current density (ampere/cm²)

J_0 = reverse saturation current density (ampere/cm²)

r_s = specific series resistance (Ω -cm²)

r_{sh} = specific shunt resistance (Ω -cm²)

1.4 Review of the Single Solar Cell Energy System

The core block of energy harvesting unit is PMC. The first charge pump based power converter is Dickson charge pump that had a linear topology [6] recently N stage linear charge pump have been extensively studied [7] and optimized in terms of efficiency and losses (switching and conduction). The performance of linear charge pump will degrade when used in terms of ultra-low voltage energy transducer [8]. In order to improve the power conversion efficiency cross coupled charge pump that failed when input voltage is lower than threshold voltage of MOS. The author of [8] addresses these problems and implements Tree charge pump that has maximum efficiency around 72% (MIMCAP) and implements the system with MPP to achieve efficiency of 39.8% (MOSCAP).

In second literature review [9] author addresses about 120mV input dual mode charge pump topology. But this voltage is not enough to charge 1 volt of battery. At 120 mV input voltage system output will reach at 770mV. Maximum efficiency achieved is 38.8%.

Third one [10] , proposed how to improve output power of SCCP which include bottom plate capacitor. Maximum efficiency achieved is 67%, but at high input voltage (753.8mV).

None of the authors addresses the issue of the protection circuit for battery and cold startup circuit. So furthering from this stage we improve the present system given in [11] with battery protection input condition sensor and cold startup circuit.

Chapter 2

Efficient DC-DC Power Converter with Feed Forward MPPT

2.1 System Block Overview

This system has on chip charge pump based DC-DC power converter, feed forward voltage controlled oscillator (VCO) [14] to harvest maximum power from the energy harvester unit, Battery protection circuit to protect battery from over charging as well as excess discharging in case of over load or lower input power, Input condition sensor to sense input power level, digital controller block to enable or disable battery protection circuit, input condition sensor circuit and startup circuit. Startup circuit is used to charge the battery from zero voltage level to make the system functioning. The block level of proposed energy harvesting unit is shown in Fig.2.1.

It can be shown that input energy passes through different states [15] starting from energy conversion from surroundings through solar cell, energy transfer by DC-DC converter, energy storage by battery or super capacitor, energy transfer to load, and energy consumption by controller block (BM, DC, VCO etc.). Micro scale solar energy harvesting means extracting energy from very tiny solar cell of 1cm^2 size. Harvesting energy from light, it is converted into electrical energy with help of very tiny solar cell size of 1cm^2 . It produces very low power in the case of indoor lights, in the range of a few micro watts. It has voltage range from 0.0 volt to 0.5 volt [16]. To drive the load operated at 1 volt, we need the converter which transfer energy and boost the voltage. To transfer maximum power from the solar cell we need the maximum power tracking circuit and that is done by the feed forward voltage controlled oscillator. To store energy we need the battery or super capacitor so that, in the absence of input power, battery can drive the load for some time. Now, we have to protect the battery from over discharging and over charging hence, we need the battery protection circuit to extend the life time of the battery. In the

absence of input power, controller circuits will consume power from the battery itself and the battery will discharge.

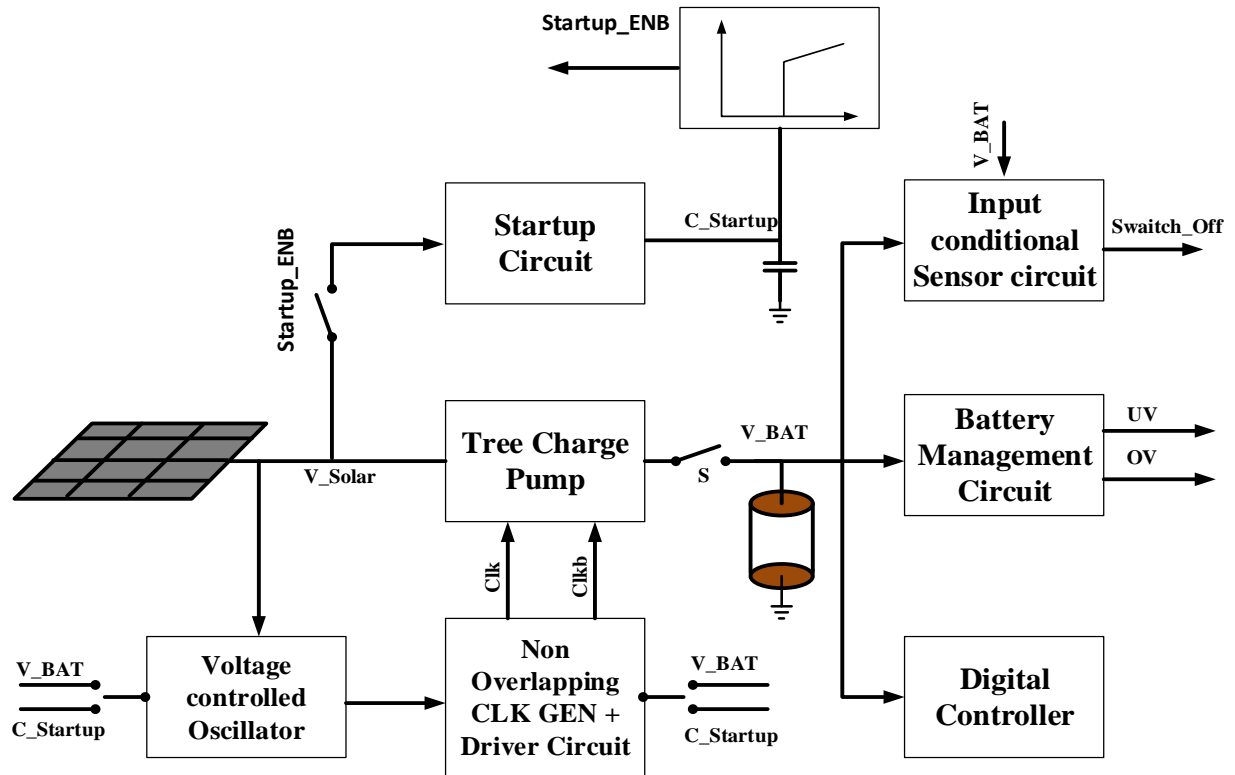


Figure 2.1 Proposed Energy harvesting Architecture

For the continuous monitoring of the input power we have implemented the input conditional sensor circuit. For operating all the controller blocks like battery protection circuit, input condition sensor need digital controller that handle enabling and disabling process. In the end, the most challenging block, the startup circuit that triggers when the battery voltage goes below under voltage cutoff or totally drains out.

2.2 DC-DC Power Converter

There are three different kinds of converter available. First one is low dropout regulator (LDO), buck boost converter and switched capacitor charge pump (SCCP) [15]. The advantages of a low dropout voltage regulator over the other DC to DC regulators include the absence of switching noise (as no switching takes place) [17]. This is used for step down purpose. LDO has high efficiency because it has very less drop out voltage. DC-DC Buck boost converter is used for step down and step up respectively. It has very high efficiency because of high quality factor inductor. The main drawback of using these converters is the bulky off-chip inductor [2]. This

introduces huge electromagnetic interference (EMI) noise as well as occupies large area that is not suitable for low cost integration due to the die area constraints [14]. SCCP has combination of MOS switches and capacitors. SCCP has very low cost and less area integration. It requires two phase clock generation circuit. We are focusing on SCCP because our motivation is to implement low cost, less area and on chip solution. Whether to choose step up or step down converter, it does depend on transduce output and buffer voltage level.

2.3 Switched Capacitor Charge Pump

Charge pumps have different design metrics such as power conversion efficiency, output ramp up time, and output ripples. The most important metric is the charge sharing capability (the ability of the charge pump to do a complete charge sharing), which is characterized by the knee frequency (the frequency at which the output current of the charge pump reaches $(1/\sqrt{2})$ of the maximum possible current value) of the architecture used [18]. The first published converter is the Dickson charge pump [8], which exhibits linear characteristics. Linear topologies performance degrades in terms of charge sharing for low input voltage values which is the case for micro-scale harvesters. Several topologies are proposed recently and the most effective architecture proposed is the tree topology [10]. It increases the capability of the charge sharing by decreasing the worst charging time constant, and correspondingly, increases the knee frequency. Fig. 2.2 shows a two stages tree charge pump that is used in the proposed design in this work. The number of stages is determined by the input voltage and the output voltage levels. Here, the output voltage is four times the input voltage according to Eq. (2.1). The charge pump output current depends on the flying capacitance values C_F (C_1 , C_2 and C_3), frequency of PHI, PHIB and the difference between the input voltage and the output voltage [10]. The flying capacitance is chosen to be 500 pF in order to decrease the operating frequency range where N is the number of charge pump stages used, here two stages is used to reach an output voltage of 1 V.

Considering complete charge sharing happened at given clock frequency, so the output current equation I_{OUT} .

$$V_{buffer} = (N + 1)V_{Source} \quad (2.1)$$

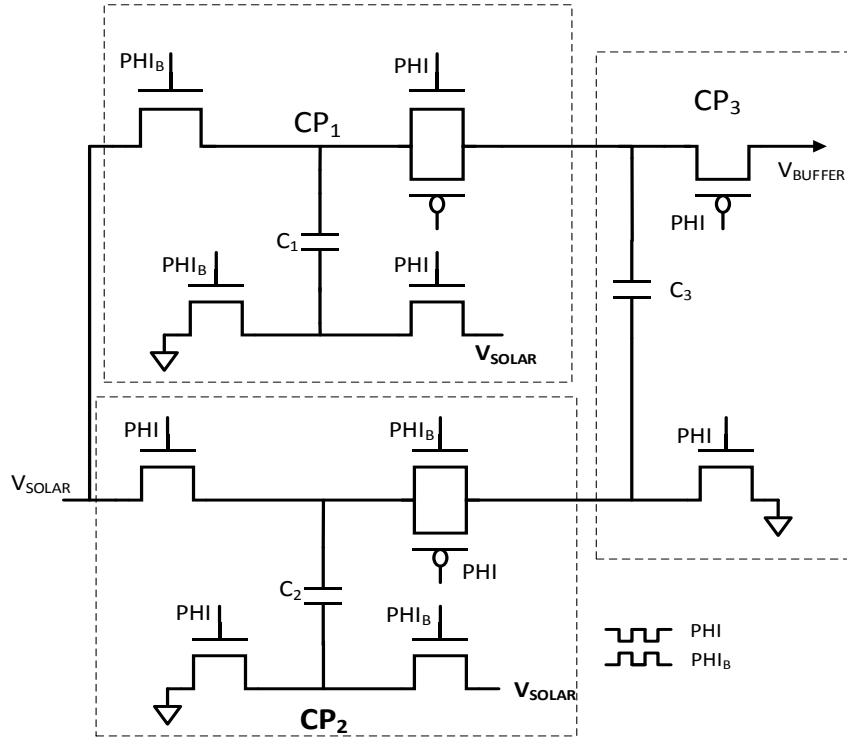


Figure 2.2 Tree CP Topology

$$I_{OUT} = f_{CLK} Q_{avg} \quad (2.2)$$

$$I_{OUT} = \frac{1}{N} f_{CLK} C [(N + 1)V_{source} - V_{buffer}] \quad (2.3)$$

$$I_{IN} = (N + 1)I_{OUT} + I_{CP,LOSS} \quad (2.4)$$

$$I_{IN} = \frac{N + 1}{N} f_{CLK} C ((N + 1)V_{source} - V_{buffer}) + f_{CLK} \beta \quad (2.5)$$

Where N is the ideal voltage step-up ratio, C is the flying capacitance used in each stage, and f_{CLK} is the switching frequency. V_{source} and V_{buffer} are the power converter's input and output voltages, respectively. β represents the power converter losses.

The equivalent input impedance R_{IN} of the power converter can be derived as-

$$R_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{1}{f_{CLK} \left[\left((N + 1) - \frac{V_{buffer}}{V_{source}} \right) \frac{(N + 1)C}{N} + \frac{\beta}{V_{source}} \right]} \quad (2.6)$$

The input impedance of the charge pump is inversely proportional to the operating frequency. It should be noted also that this impedance is matched to the solar cell, so each input light intensity has a corresponding matched impedance value for maximum power [14]. This impedance value

has a corresponding frequency value, so the goal of the control unit is to search for the optimum frequency value that delivers maximum solar cell power at a given input light power.

Comparison wise this tree CP topology has similar characteristics to linear CP except knee frequency. In case of tree CP, knee frequency is high because of less R_{ON} resistance at high stages. So it can be concluded that tree topology is better charge pump for broad range of frequency.

So we have implemented tree CP topologies as DC-DC converter for energy harvesting unit.

Now we implement CP with different flying capacitor. Different flying capacitors are MIMCAP, MOSCAP and ZERO- V_T -MOSCAP. We found that for compact device area, MIMCAP is not a feasible solution rather it gives better efficiency because of high quality factor.

If we compare MIMCAP with MOSCAP for the same area, effective capacitance is increased by (X8) (Table 2.1) in case of MOSCAP. MOSCAP is also not a proper solution because output voltage of transducer is less than the threshold voltage of MOS in 180nm technology. So if you see in C-V curve in Fig.2.3 [19], below threshold voltage MOSCAP will not give effective capacitance. So the first two flying capacitors we used as ZERO- V_T -MOSCAP. This simulation is done for the same size ($W=64, L=16$) of MOS and ZVT-MOS capacitor Vs voltage. It is concluded that ZVT is giving effective capacitance ($C=8.43pF$) below threshold voltage of MOS. In [14] tree topology has 39.6% efficiency by using MOSCAP. We introduced ZVT MOSCAP in first stage and achieve 67% maximum converter efficiency shown in fig.2.4.

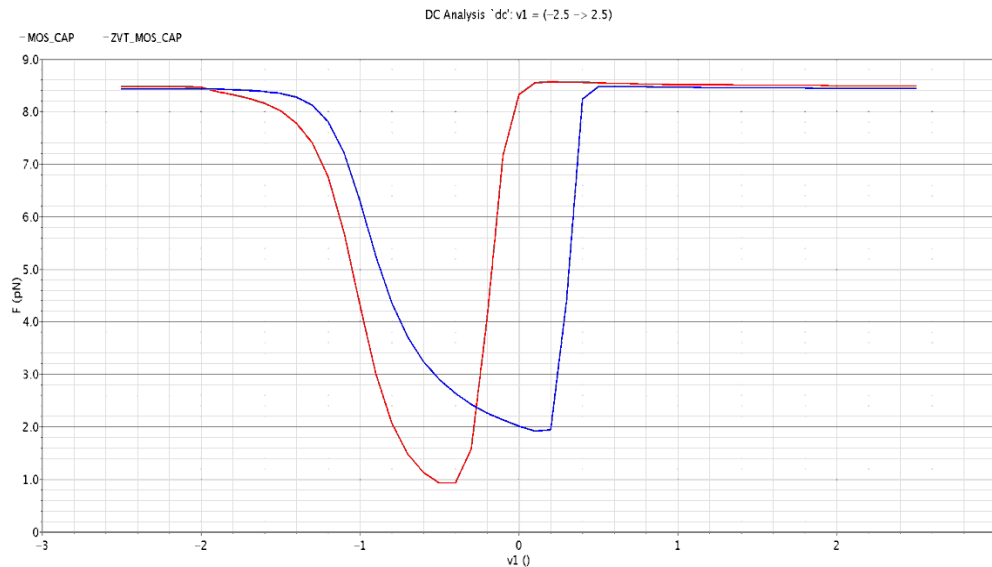


Figure2.3 CV plot of MOS and ZVT-MOS CAP

Table 2.1 Area comparison of different capacitor with capacitance value

Area Comparison	W(μm)	L(μm)	Capacitor Size(pF)
MIMCAP	64	16	~1
MOSCAP	64	16	~8

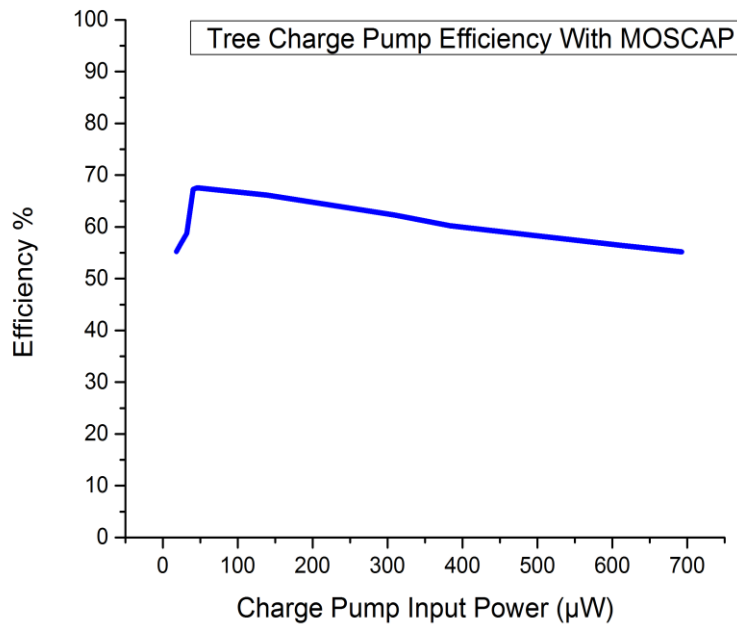


Figure 2.4 Charge pump efficiency vs. input power

For efficiency, plot simulation is performed with two ZVT MOS and one MOS cap. We achieved maximum efficiency of 67% with this concept without changing the size. Also, more than 50% efficiency has been achieved for wide range of input power.

2.4 Major Power Losses in CMOS Charge Pumps

As shown in Fig.2.2, since the voltage drop across each turned-on power switch is equal to the drain-to source voltage V_{DS} (150 mV or less) rather than a threshold voltage V_{TH} in a Dickson charge pump, the design is determined to be more efficient [9]. Today, almost all on-chip charge pump designs are based on the V_{DS} drop across power switch.

In general, the efficiency of a charge pump is defined as,

$$\eta \% = \frac{P_{OUT}}{P_{IN} + P_{LOSS}} \times 100 \quad (2.7)$$

Where P_{OUT} represents the output loading power, and P_{LOSS} represents the total internal power loss caused by the charge pump itself, including switching loss, conduction loss etc. Obviously, when P_{LOSS} is minimized, the efficiency is optimized to the maximum.

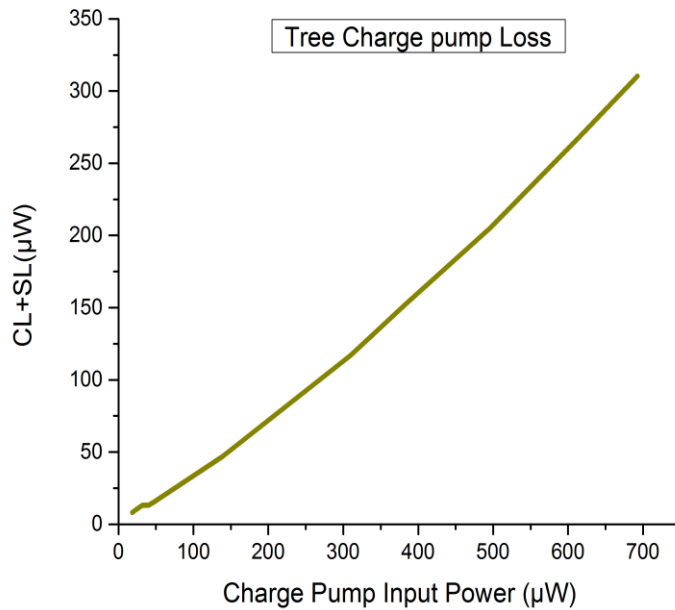


Figure 2.5 Charge pump losses vs. input power

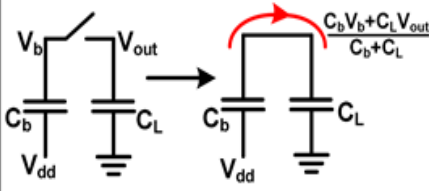
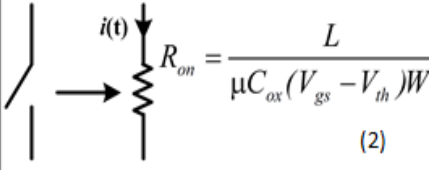
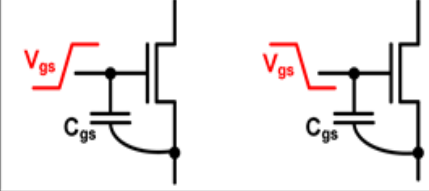
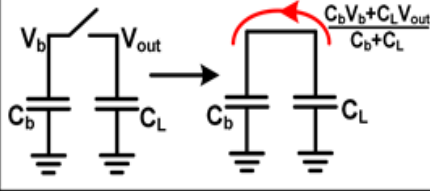
The power loss of the power stage normally dominates P_{LOSS} . Based on power loss generation mechanisms, the power loss in a power stage mainly consists of redistribution loss, conduction loss, switching loss and reversion loss. We first summarize the losses [20] in Table 2.2 and discuss them one-by-one in due course.

As listed in Table 2.2, the redistribution loss is caused by charge transference between the capacitors in a charge pump. Charge sharing happens because of Voltage difference between two flying capacitors cause “redistribution losses”.

In CMOS implementations, power switches are usually implemented by MOSFET transistors. When a switch is turned on, the turn-on resistance of the transistor causes the “conduction loss”

in the power stage. From the conduction loss equation in Table 2.2, the loss can be reduced by increasing the aspect ratio of the transistor, W/L . However, this directly leads to the increase on another power loss – “switching loss”. It is well known that a MOSFET transistor is a voltage controlled device, meaning that the transistor’s ON/OFF states as a switch are determined by a control voltage V_{GS} . The voltage changes on V_{GS} are accomplished by charging and discharging the gate capacitor of the transistor, which is proportional to the product of transistor’s width and length, WXL . From this perspective, to reduce the switching loss, the size of the transistor is preferred to be small. Obviously, there exists an optimal point for the width of the transistor, W , where the sum of conduction loss and switching loss reaches the minimum. Finally, a reversion loss occurs when shorting a higher voltage node to a lower one, forming a reversion current from the original power flow. In this scenario, charge is transferred from the higher voltage circuit node to the lower one.

Table 2.2 POWER LOSSES IN CMOS CHARGE PUMPS [20]

Mechanism	Power Loss
	<p>Redistribution Loss</p> $\frac{1}{2} f_s C_b (V_b - V_{dd})^2 + \frac{1}{2} f_s C_L V_{out}^2 - \frac{1}{2} f_s \frac{(C_b V_b + C_L V_{out})^2}{C_b + C_L} \quad (1)$
	<p>Conduction Loss</p> $R_{on} f_s \int_0^{DT} i^2(t) dt \quad (3)$ $R_{on} = \frac{L}{\mu C_{ox} (V_{gs} - V_{th}) W} \quad (2)$
	<p>Switching Loss</p> $\propto \frac{1}{2} f_s C_{gs} V_{gs}^2 = \frac{1}{2} f_s C_{ox} W L V_{gs}^2 \quad (4)$
	<p>Reversion Loss</p> $\frac{1}{2} f_s \frac{C_b C_L (V_{out} - V_b)^2}{C_b + C_L} \quad (5)$

2.6 MPPT

The maximum power point tracking algorithm originates from empirical data analysis. According to experimental results on transducer, there is a linear relationship between V_{MPP} and V_{OC} . This is approximately 0.75x of V_{OC} . Based on this relationship; energy transducer momentarily disconnects from load and sampled the V_{OC} value and store in capacitor. Then compare with voltage connected to the load. This method is suitable for micro-scale energy harvesting systems because it involves simple open-loop control and does not require any intensive computations like hill climbing algorithms [20]. The drawback of this approach is that the energy transducer is periodically disconnected from the load, which causes temporary power loss to the load. Further, there is a hardware cost like switches and control generation circuitry involved in time multiplexing between normal operation and the open circuit mode of operation. To address these disadvantages, an improved design was presented in [21], where an additional energy transducer is used in the system as a pilot cell. The open circuit voltage of the pilot cell is used in place of the open circuit voltage of the main energy transducer. This eliminates the necessity for doing any open circuit voltage sensing on the main energy transducer. However, with this approach, the pilot cell should be carefully chosen to ensure that its feature is close to that of the main energy transducer. More importantly, this approach is hard to implement for system-level MPP tracking, since the system MPP voltage is no longer linearly dependent on the open circuit voltage, when the impact of a power converter is considered [15].

For our project we are using the architecture proposed in [14]. The approach is based on investigating the system design equations and finding a compact relationship between PV cell terminal voltage and the target operating frequency required for maximum power transfer. This technique is based on the negative feedback automatic tracking [15]. The main advantage of this design is that there is no need for extra tracking circuitry. So we need very less power to operate this circuit, as it is suitable for micro scale energy harvesting. We can see from above equation how the relationship happening in between equating input current of CP and output current of solar cell-

$$I_{IN} = \frac{N+1}{N} f_{CLK} C \left((N+1)V_{source} - V_{buffer} \right) + f_{CLK} \beta \quad (2.8)$$

$$I = I_o \left[\left(e^{qV_{oc}/\eta KT} \right) - \left(e^{qV/\eta KT} \right) \right] \quad (2.9)$$

$$f_{CLK} = \frac{I_o \left[\left(e^{qV_{oc}/\eta KT} \right) - \left(e^{qV/\eta KT} \right) \right]}{\frac{N+1}{N} C \left((N+1)V - V_{buffer} \right) + \beta} \quad (2.10)$$

From the equation, it can be concluded that CP switching frequency depends on charge pump input voltage (same solar cell output voltage). We can see from equation of the input impedance of the charge pump that when frequency increase impedance will decrease so the input voltage of the charge pump will also decrease. Hence, it can be concluded that there is a point on each curve that corresponds to the maximum power out of the solar cell. Designed VCO is given in Fig.2.6 and the output of VCO with input voltage variation shown in Fig.7.

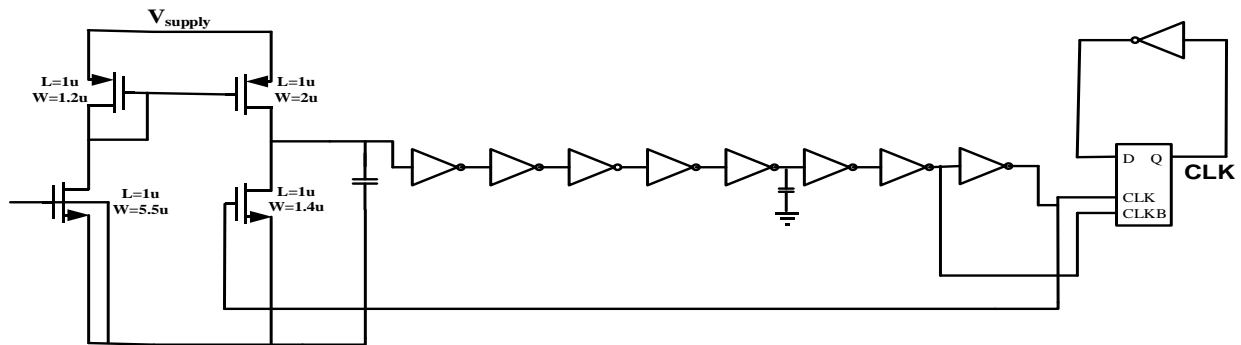


Figure 2.6 Feed forward Voltage Controlled Oscillator

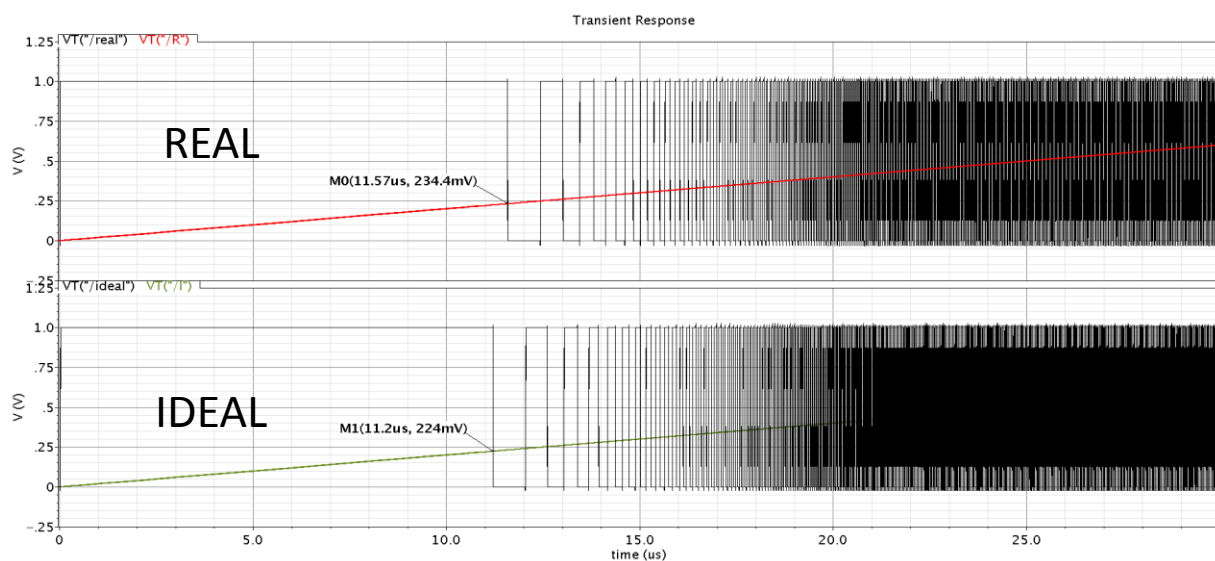


Figure 2.7 Frequency variation vs. voltage of VCO

2.6 Basic System

Fig.2.8 shows the block diagram of basic micro scale energy harvesting system. This system contains automatic MPPT tracking unit driver circuit to drive power converter switches. Previously, we have shown the efficiency plot of the converter with the external clock supply voltage. Now our controller circuit (VCO + DRIVER) takes power from Battery itself to supply to two phase of clock with tracking maximum power.

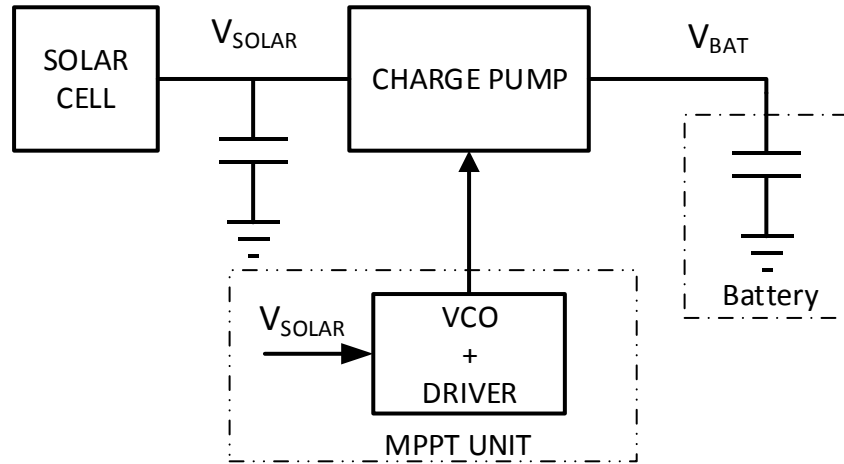


Figure 2.8 Basic Architecture of Energy Harvester

Table 2.3 End to end efficiency comparison of energy harvester with different flying

System with different kind of flying cap	P_{in}	P_{out}	Max. efficiency
MIMCAP	324.5 μ W	196.76 μ W	60.63%
ZVT MOS	323 μ W	176 μ W	55%
MOSCAP	326 μ W	143.5 μ W	44%

We checked system with different flying capacitor for power converter. Comparison Table 2.3 Shown that the maximum efficiency is achieved by MIMCAP. But we have already discussed that for small form factor we choose MOSCAP. Conventional MOSCAP doesn't give effective capacitance because solar transducer used in indoor cases gives voltage less than threshold voltage of MOSCAP. From Table 2.3, we conclude that ZVT is the better solution for SCCP for input voltage less than threshold voltage. So we simulated this system for different illuminations and achieved maximum end to end efficiency 51.8%. Fig.2.9 & Fig.2.10 shows the end to end

efficiency vs. input power for basic block and power loss across VCO and driver circuit respectively.

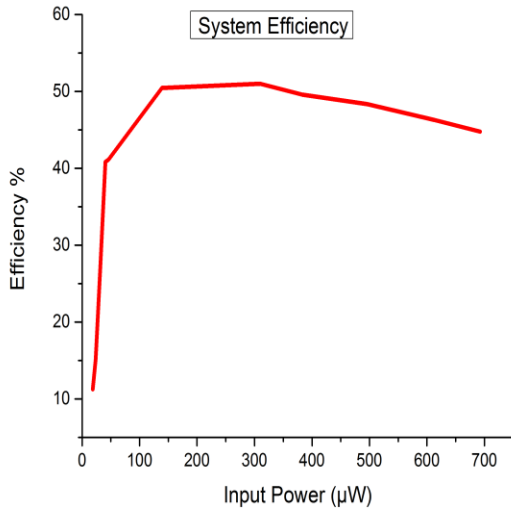


Figure 2.9 End to end Efficiency vs input power

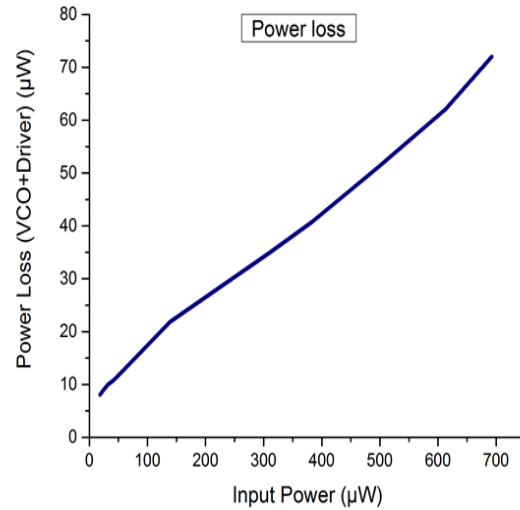


Figure 2.10 Controller loss vs. input power

2.7 Storage Buffer

Energy sources, as seen in Table 1.1, are very rare and inconsistent over time. A system would stop working in the night if relying only on the output of a solar cell. For this reason storing harvested energy is very important. Subsequently, terms as high power or peak power are intended to power values of $> 10\text{mW}$, on the other hand, small power is everything below 1mW [22]. There are several types of storage elements such as batteries or capacitors, however, the crucial characteristic for this project is that they must be able to be charged and discharged several times, since this is most likely how they are going to be used. The main physical difference between capacitors and batteries is how the energy is stored: in the capacitor the energy is stored on the plates thanks to an electric field; in the battery instead the energy is stored in chemical format and then converted into electrical energy [23]. This justifies that battery performances decays after charging cycles due to chemical deterioration, instead capacitor can be charged more than a million of times without significant deterioration. Capacitors discharge and re-charge very quickly, in this way they can provide a lot of power but only for a short time. So capacitors have a lot of power capability but small energy capacity. On the other hand, batteries are slow devices, providing less power but for longer periods, they are not able to stand high peaks of power demand, but they work efficiently in constant load conditions. Supercapacitors are an evolution of

capacitors with higher energy, but still not able to reach energy level in batteries. The important parameter is to take into account when considering super-capacitor is the leakage current, proportional to capacity, temperature and voltage. Initial leakage is quite high, but declines over time. Since this current is usually high, it can rapidly discharge a capacitor.

After analyzing all the parameters, it is clear that Li-Ions are not suitable for EH due to their low level of life cycles, in fact an EH system could be charged and discharged several times per day.

Chapter 3

ULP monitoring circuit with cold startup

3.1 Battery Protection Circuit

3.1.1 Battery under voltage (UV) protection

To prevent rechargeable batteries from being severely discharged and damaged, and to prevent the complete depletion of charge from a capacitive storage element, the chip has set UV threshold (UVT) with the help of external resistor. The UVT point has been set to 0.8V (programmable) externally with the help of the resistor divider. This is performed by V_{REF} and two sample signals corresponding to the battery voltage [3]. In the case of UV, both sample voltages are less than the V_{REF} voltage. In this case, the UV signal will turn low and the system will turn in to the startup mode.

$$V_{LS} = \frac{R_3 V_{BAT}}{R_1 + R_2 + R_3} \quad (3.1)$$

$$V_{US} = \frac{(R_2 + R_3) V_{BAT}}{R_1 + R_2 + R_3} \quad (3.2)$$

$$V_{REF} > V_{LS}, V_{US} \quad (3.3)$$

3.1.2 Battery Over Voltage (OV) Protection

To prevent rechargeable batteries from being exposed to excessive charging voltages and to prevent it from over charging, a capacitive storage element at the overvoltage (OV) threshold level must be set to protect battery.

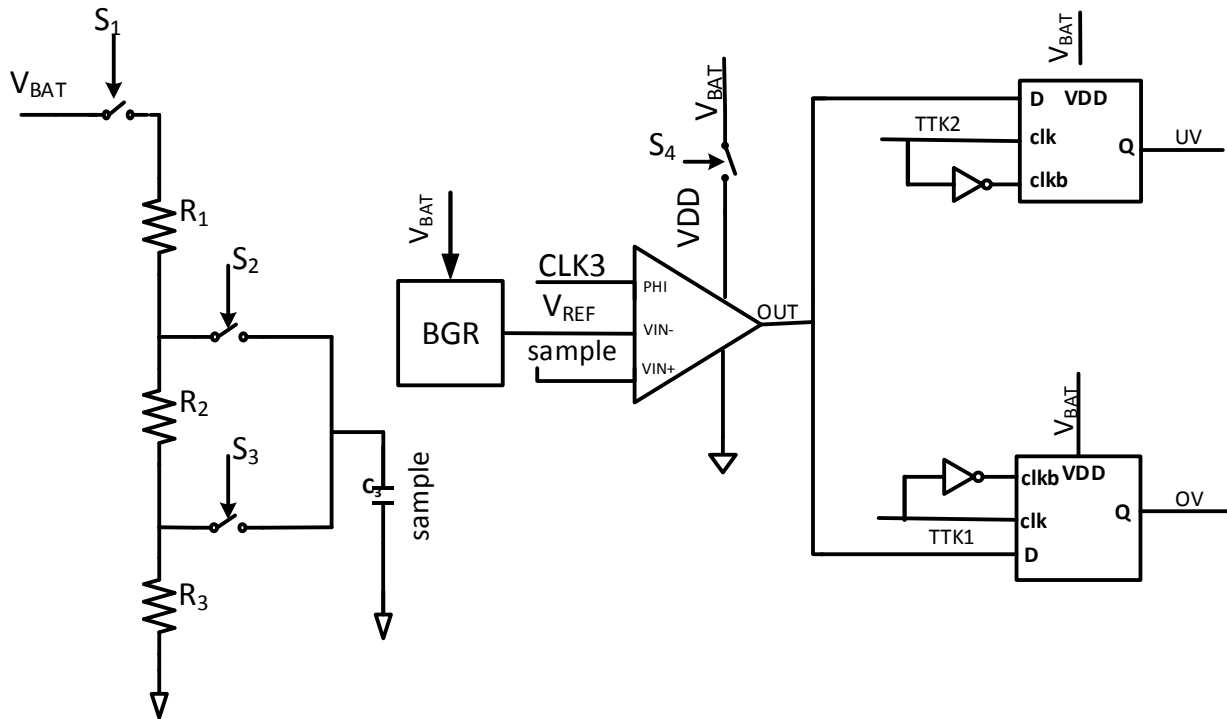


Figure 3.1 Battery protection Schematic Circuit

The chip has set OVT point with the help of external resistor. In the case of OV both sample (LS, US) values are higher than the V_{REF} .

$$V_{REF} < V_{LS}, V_{US} \quad (3.4)$$

In this case OV signal will go high, and stop the converter to charge the battery further.

3.1.2 Battery Voltage in Operating Range

When the Battery Voltage remains in the operating range, it denotes that it is higher than the UVT point and less than the OVT point,

$$V_{LS} < V_{REF} < V_{US} \quad (3.5)$$

In this case the battery can drive the load properly.

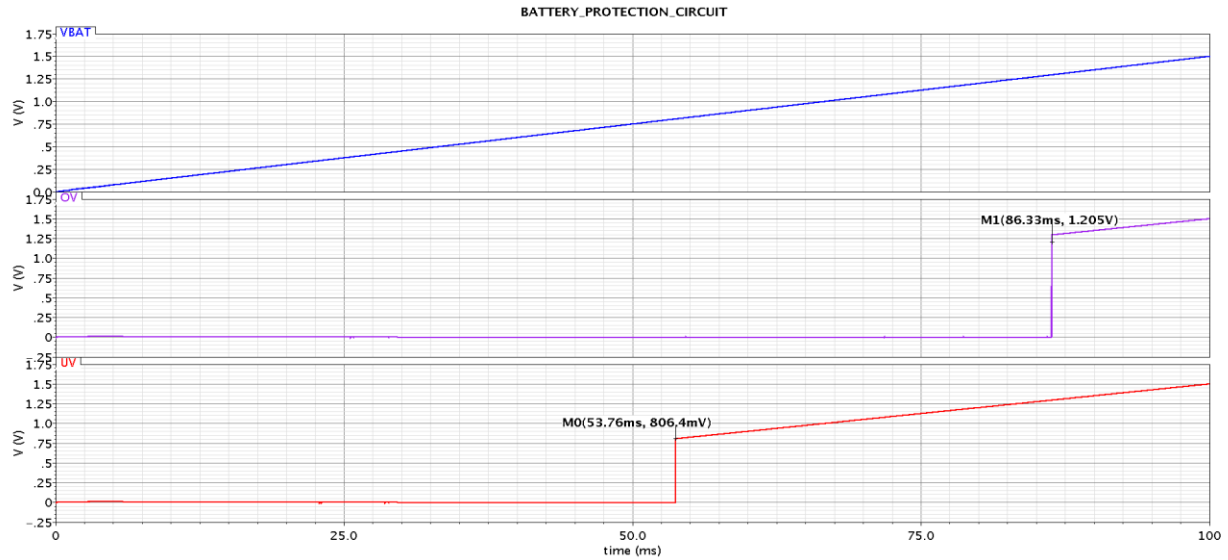


Figure 3.2 Battery Protection output w.r.t. battery condition

3.2 Input Conditional Sensor

To obtain an estimate of the net power, the MPPT block generating the clock is powered using a battery ($C=50\mu\text{F}$) of 1 volt. Also, the output of the power converter is connected to the same battery. An increase in the voltage across the capacitor implies positive net power and a decrease implies a negative net power [23]. To check whether the net power is positive or negative we proposed input sensing circuit.

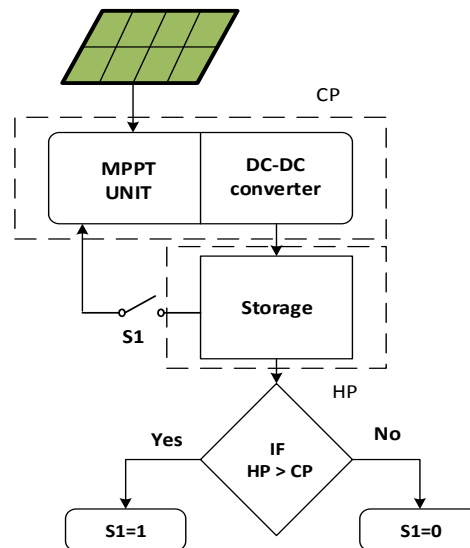


Figure 3.3 State diagram of input condition sensor

The sensing circuit consists of two capacitors C1 and C2 and a comparator. The activation signal to the sensing circuit is provided by low frequency clock. When the sensing circuit gets activated the battery voltage is sampled across the capacitors C1 and C2. Then the MPPT block producing clock is powered using the capacitor C1 and the output current is also fed to the capacitor C1.

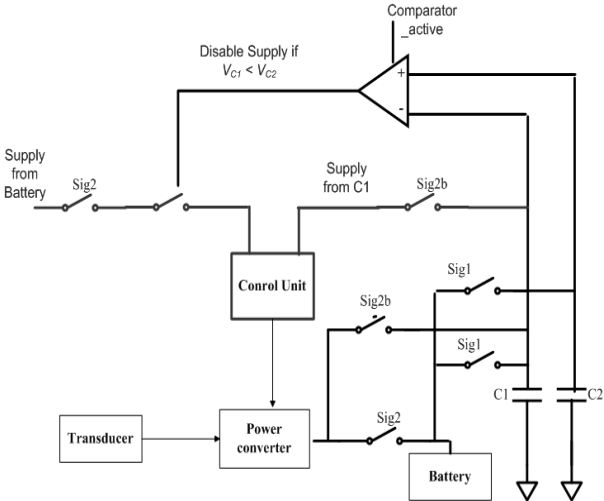


Figure 3.4 Implementation of the Input condition sensor

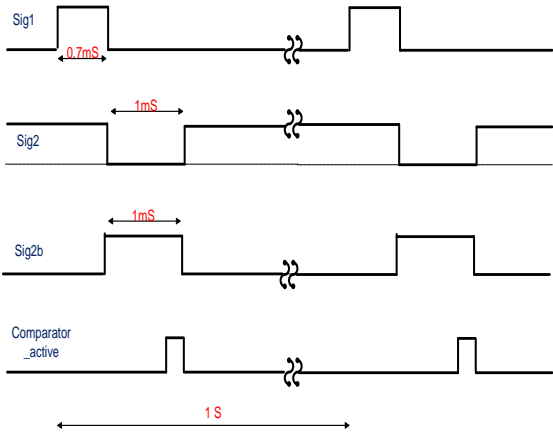


Figure 3.5 Control signal for input condition sensor

After a certain period of time, the voltage at capacitor C1 is compared with that of the reference capacitor C2. There are two possibilities, if voltage across C1 is less than C2 it indicates that the power consumed to generate the clock for the power converter is more than the power delivered to the battery. And the second, if voltage across C1 is greater than C2 it means system is efficient to harvest the energy at this power level. In the first case it switches off the power converter block to save battery power.

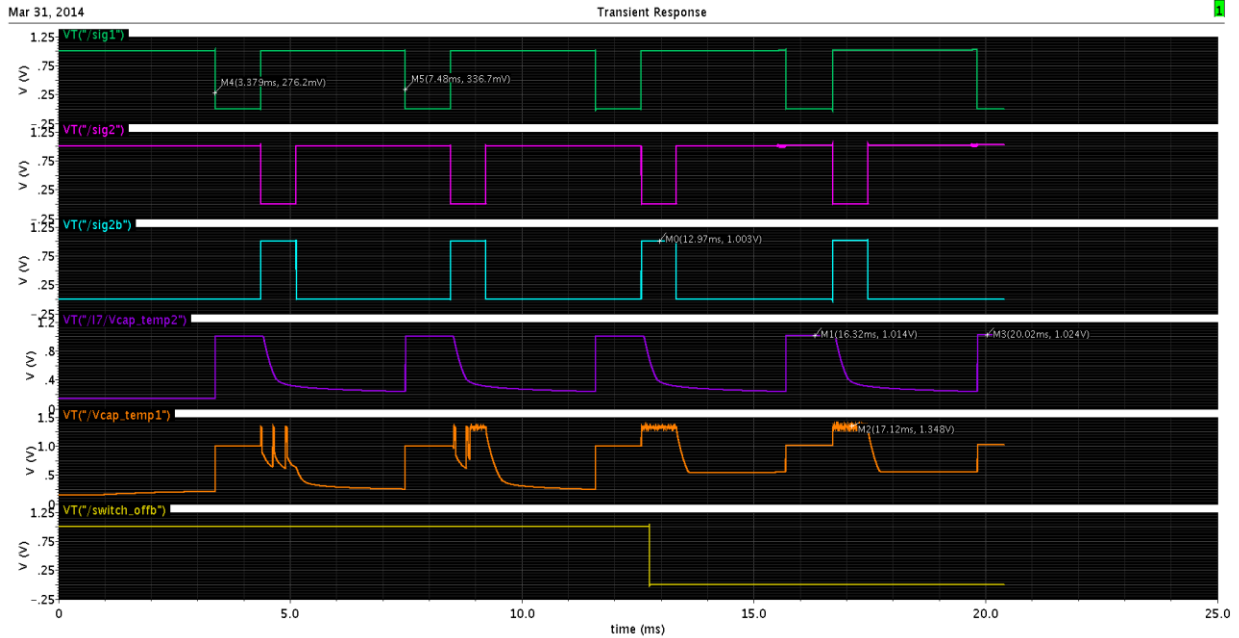


Figure 3.6 Simulation result of input condition sensor

Here two 500pF capacitors are used. A very low frequency clock is used to generate signal sig1. When sig1 goes low, both capacitors are connected in parallel with the battery. The signal sig1 is held low for 700us so that the two 500pF capacitors reach up to the battery voltage. After sig1 another signal sig2 is pulled low. When sig2 goes low, the power supply to the power converter system is provided by one of the 500pF (C1) capacitor. Also, the power delivered by the power converter is fed into this 500pF (C1) capacitor. After a period of 1ms sig2 is pulled high so that the power converter gets its power from the battery and also delivers the power to the battery. After the sig2 period, comp_active pulse is generated to compare the voltages across the two capacitors. Fig.3.6 shows the results of input condition sensor, we can observe that after 13ms (startup time of digital controller to generate comp_active signal) sensor given decision that input power is effective to run the system.

3.3 Startup Circuit

In this section, we propose the 317mV input voltage startup circuit that will charge up to 1volt. The startup circuit is used in two conditions: first, when the battery voltage goes below UVT and second, when the battery voltage drains out to zero. When the battery voltage drains out to zero, all the interface blocks will disable and only the startup circuit will work with the help of solar output power. The solar output voltage lies in the range of 0-0.5V. The block level diagram is shown in

Fig.3.7. This circuit consists of ring oscillator, voltage doubler and driver circuit. Basic operation of startup circuit explained –

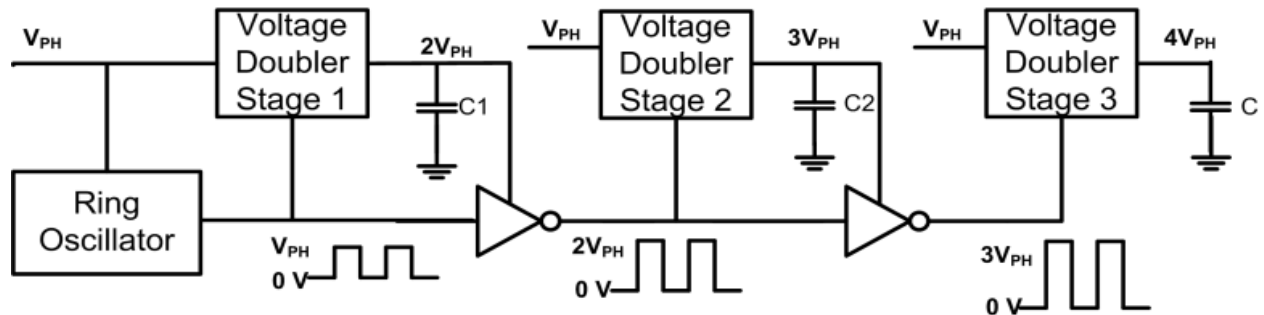


Figure 3.7 Startup circuit

Ring oscillator will generate a clock of V_{SOLAR} amplitude. This clock will be connected to the first stage of the voltage doubler through the driver circuit. At the output of the first stage, voltage will double and it is made constant with the help of the clock and the switch. In the second stage $2 \times V_{SOLAR}$ amplitude clock is generated and is applied to the voltage doubler that will give $3 \times V_{SOLAR}$ output. Continuing and following the same sequence, we will get $4 \times V_{SOLAR}$ in the end of the fourth stage.

In the case of battery drain out, startup circuit will charge C_{START} capacitor up to 1V.

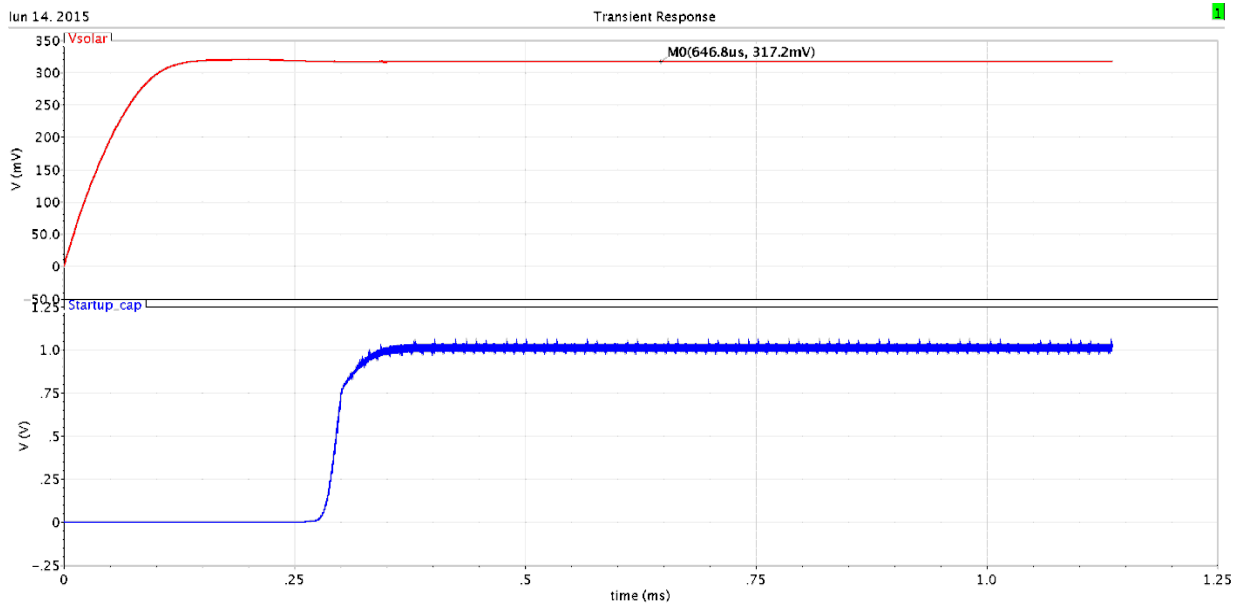


Figure 3.8 Simulation of startup circuit with minimum voltage level

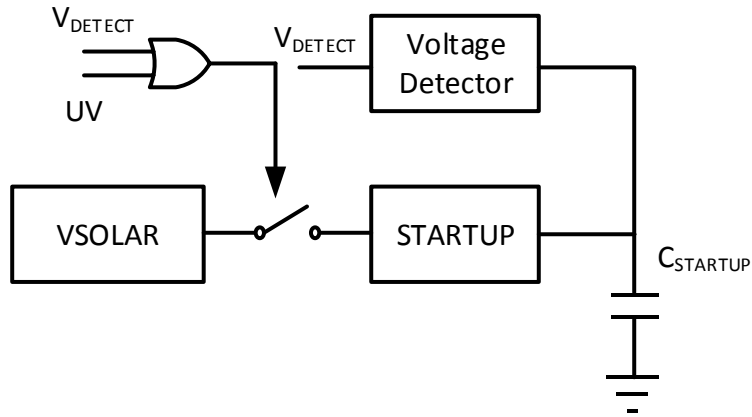


Figure 3.9 Startup circuit with voltage detector

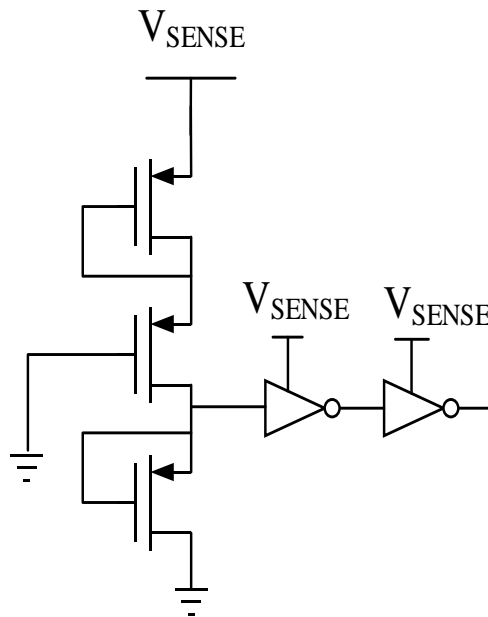


Figure 3.10 Voltage detector circuit

Fig.3.9 shows how the startup and the main converter interact with each other. When the battery voltage is below UVT point, UV will indicate low and the voltage detector will also go low until $C_{STARTUP}$ reach to 1V. The switch is active low and when the OR operation gives low, it enables and the solar cell will connect with startup circuit. Alongside, the main converter will not work hence the battery voltage will be held at the same value. When the $C_{STARTUP}$ reaches to 1V, voltage detector will give high and the switch will disable. At the same time, the $C_{STARTUP}$ start gives power supply to VCO and the driver to charge the battery through the main converter. There will be some finite iteration between startup and the main converter before the battery voltage reaches UVT point, then the UV will give high and the system will go in the main converter mode.

3.4 Voltage Detector

The modes from the startup circuit to the main step up DC-DC converter changes by detecting $C_{STARTUP}$. To change the mode, author [24] proposes nW reference less CMOS voltage detector circuit. To further decrease the power consumption, the proposed scheme eliminates the comparator and the single input signal is applied (V_{SENSE}). It can detect the voltage level of the (V_{SENSE}) and provide the trigger signal to the switches. In this scheme author derives an equation to set trigger point of voltage detector circuit. The equation is given below to find trigger point-

$$V_{Trigger} = \frac{2mKT}{q} \ln\left(\frac{W_1}{W_2} \times \frac{L_2}{L_1}\right) \quad (3.6)$$

where K is the Boltzmann constant, m is the subthreshold swing coefficient ($m > 1$). kT/q is the thermal voltage and is approximately 26 mV at room temperature ($T=300K$).

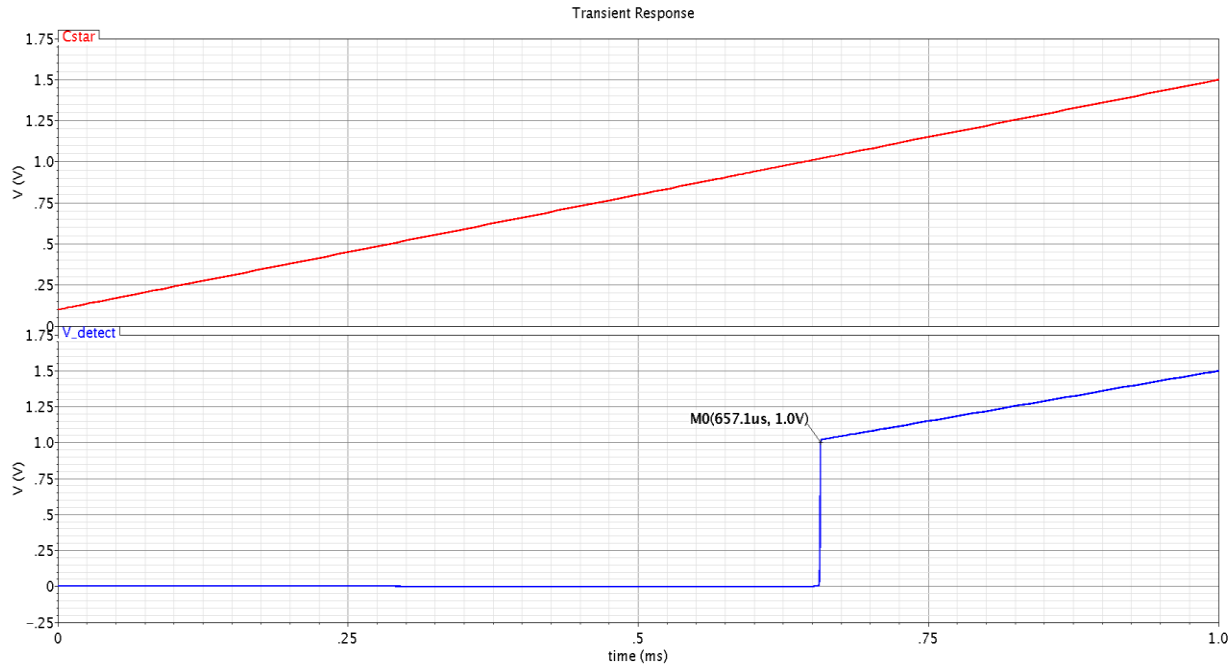


Figure 3.11 Output result of voltage detector with $C_{STARTUP}$ voltage

The simulation results of the proposed voltage detector are shown in Fig.3.11. In our design, the channel width and channel length are designed as follows: $W_2=0.24\mu$, $L_2=30\mu$, $W_1=250\mu$ and $L_1=0.24\mu$. As can be seen from Fig. 3.11 $V_{Trigger}$ point sharply changes at 1V (size corresponds to detect 1V). When the $C_{STARTUP}$ start charges from 0V and reaches 1V, the detector circuit goes high and the mode will change from startup to main converter mode.

Chapter 4

Simulation Results and Validation of Energy Harvester

4.1 System Simulation

The energy harvester system is designed with tree charge pump which has the gain of 4 and the maximum efficiency achieved is 67%. The feed forward MPP tracking algorithm is used to track the maximum power of the solar cell with the continuous monitoring of the battery and the input power level. This system also includes a startup circuit, so when the battery voltage drains out to zero the startup circuit will enable. The top level architecture shown in Fig.4.1 includes resistor divider for battery management and sample capacitor for input condition sensor, respectively.

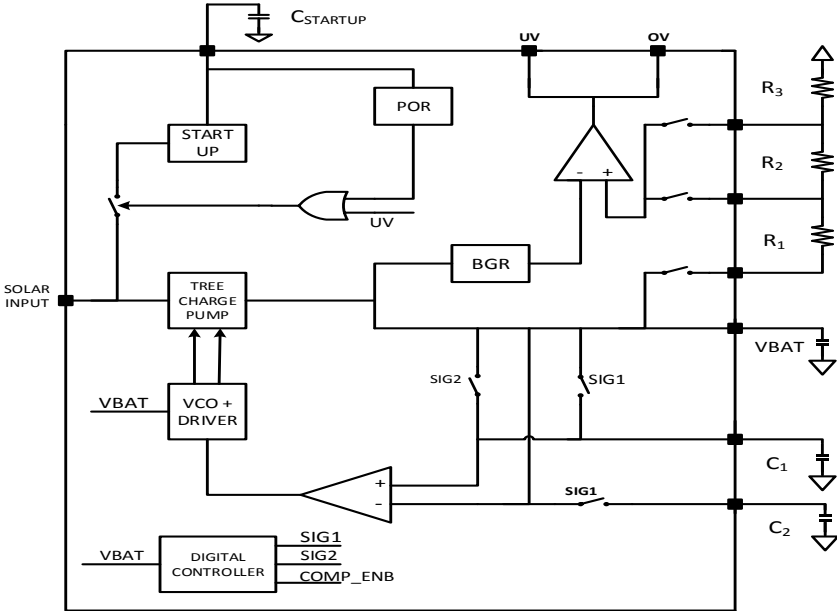


Figure 4.1 Top level Architecture of Energy Harvesting

The simulation is performed considering 0.9V UVT point and 1.1 OVT point. According to the threshold point we choose resistor value to generate samples for the battery management circuit. The program to choose the value of the resistor is given towards the end of the thesis.

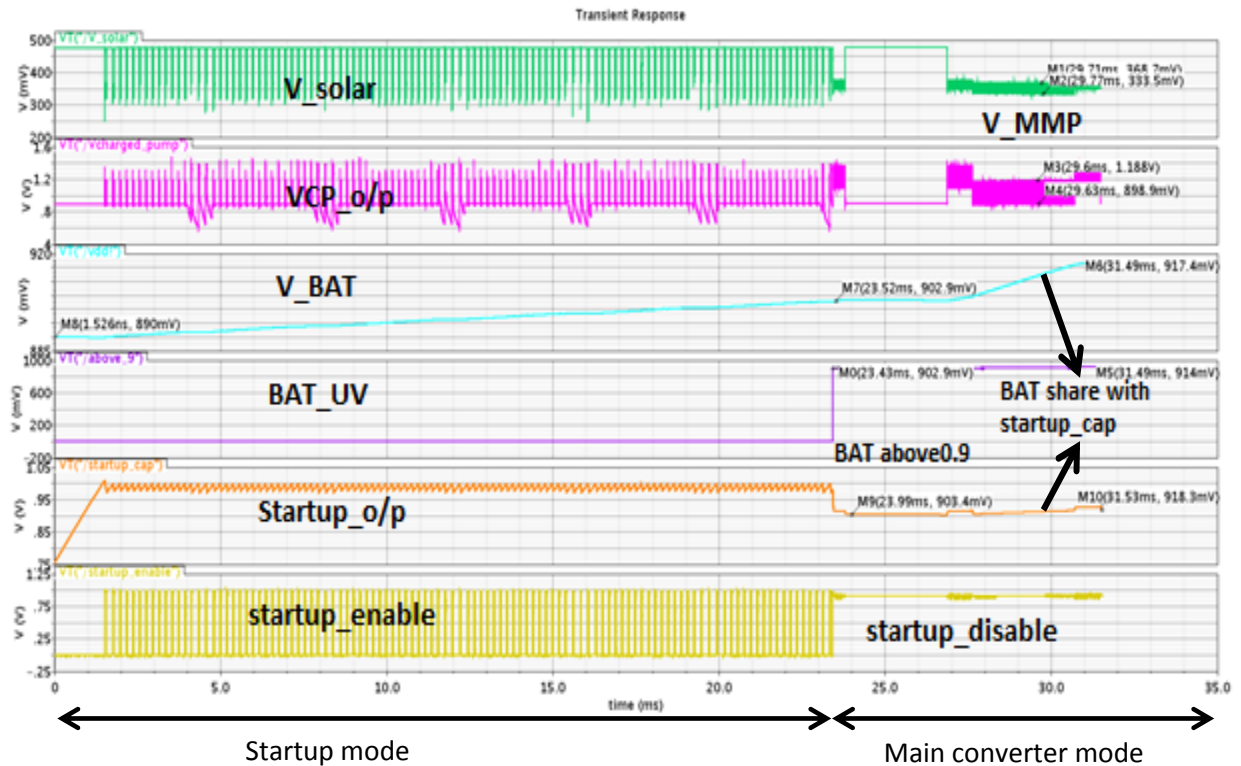


Figure 4.2 Battery protection and cold startup operation

To perform the simulation we have initialized the VBAT to 0.89mV. The system will start running and the BM will give the decision that the system is below UVT point, hence, the system will change its mode to startup mode. We can observe that the $C_{STARTUP}$ (startup_cap) starts charging to one volt. After reaching 1V, it will give supply to VCO and the driver to drive the main converter. It can be seen from the wave-form, the VBAT starts to boost and slowly reaches to 0.9V. At the same time, UV (above_9) signal goes high and it changes its mode to main converter mode. We can see that in the main converter mode, the battery charging is fast, as compared to the startup mode because of high efficiency. When the battery voltage goes above UVT point, the battery and $C_{STARTUP}$ gets connected. So whenever the battery discharges and goes below UVT point, $C_{STARTUP}$ takes less time to reach 1V. Fig.4.3 shows that when battery voltage drains out to zero, the mode will change to startup mode. To test the system we initialize the battery ($C=1\mu F$) voltage to zero and run the simulation.

It is clear from the waveform that in some finite iteration battery voltage charges and it will reach 1V.

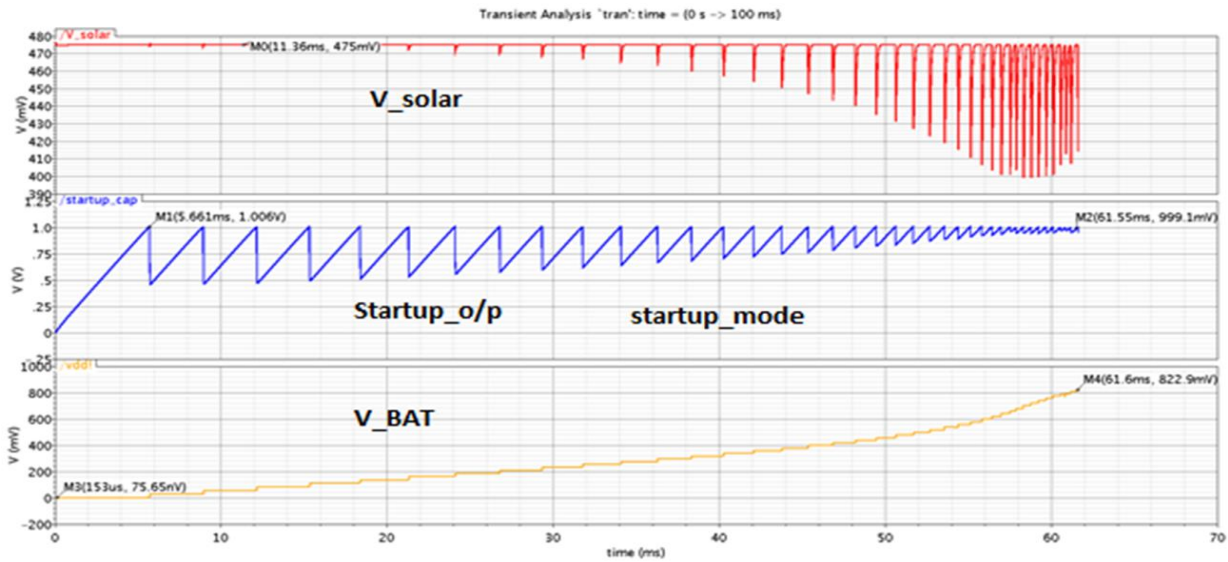


Figure 4.3 Cold Startup circuit operation with zero VBAT voltage

4.2 Cold startup Circuit

When we performed the post layout simulation of the startup circuit we got results with a small variation in the frequency. It is clear from fig.4.4 that in both cases, $C_{STARTUP}$ reaches to 1 volt with some delay.

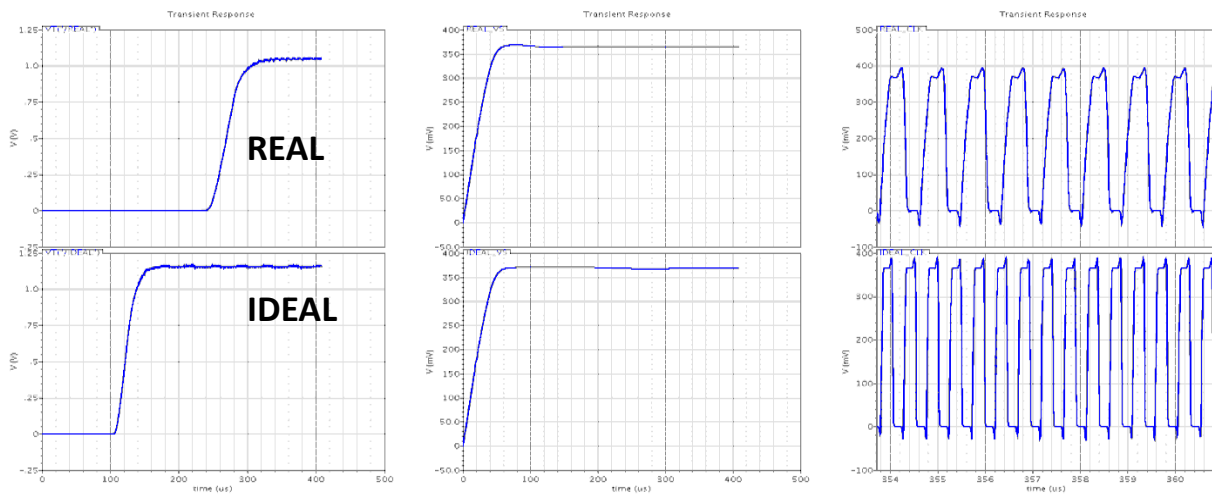


Figure 4.4 Schematic simulation vs. post layout

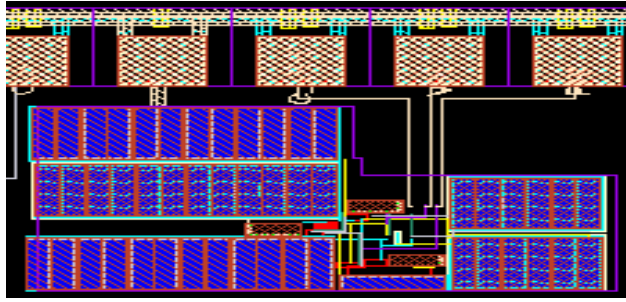


Figure 4.5 Layout image of startup circuit

Table 4.1 Startup specification

Minimum Voltage	317 mV (all process corner)
Minimum Power	847 nW
Maximum Efficiency :	42.2 %
Maximum Area	425 μ m*250 μ m

The minimum voltage required for the startup to charge up to 1 volt is 317mV. Table 4.1 shows the startup specification.

4.3 DC-DC converter (Tree CP) with VCO and driver

Fig 4.6 shows that the system can drive wide range of load with maximum efficiency of 51.2% and the maximum power consumption by VCO and the driver is 72 μ W. The whole system is designed with the minimum area of 0.489mm². This is advantageous for wearable and biomedical application. The layout image shown in Fig.4.7.

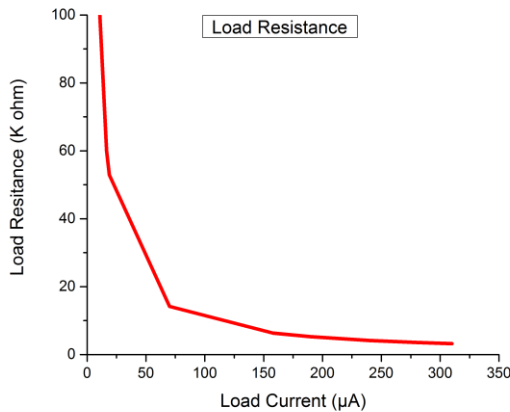


Figure 4.6 Load vs. output current

Table 4.2 Energy Harvesting specification

Minimum Input Voltage	267mV
Minimum Input Power	24 μ W
Maximum Efficiency	51.2%
Maximum Area	720 μ m * 680 μ m

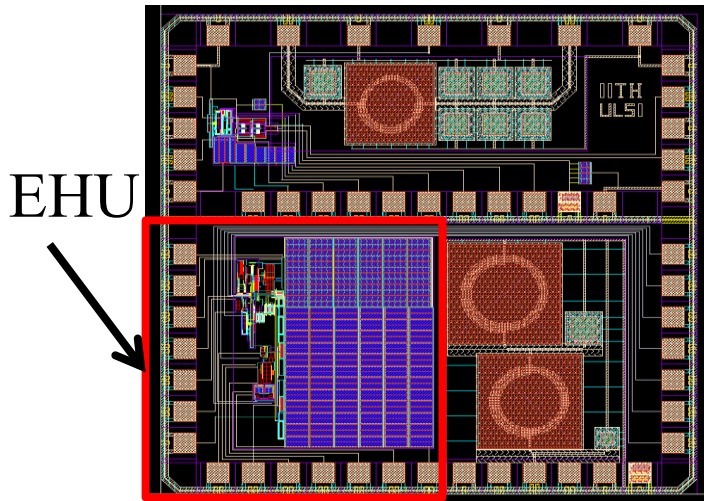


Figure 4.7 Layout image of energy harvesting unit

4.4 System Validation

To validate our system, we have to apply this energy harvester to make the device self-powered. We chose ZigBee receiver with specification of $700\mu\text{A}$, 0.8V power supply with maximum power of $560\mu\text{W}$. But our single energy harvester system can drive maximum $350\mu\text{W}$ to maintain efficiency above 50%. To achieve $560\mu\text{W}$ power, we connected two harvester systems in parallel with two identical solar cells and a single battery. To drive ZigBee, we need the constant supply voltage of 0.8V hence we connected LDO to the battery that can give 0.8V with $0.4\text{V } V_{\text{REF}}$ and 0.28V bias voltage. Fig.4.8 shows the block diagram of energy harvester system with driving load.

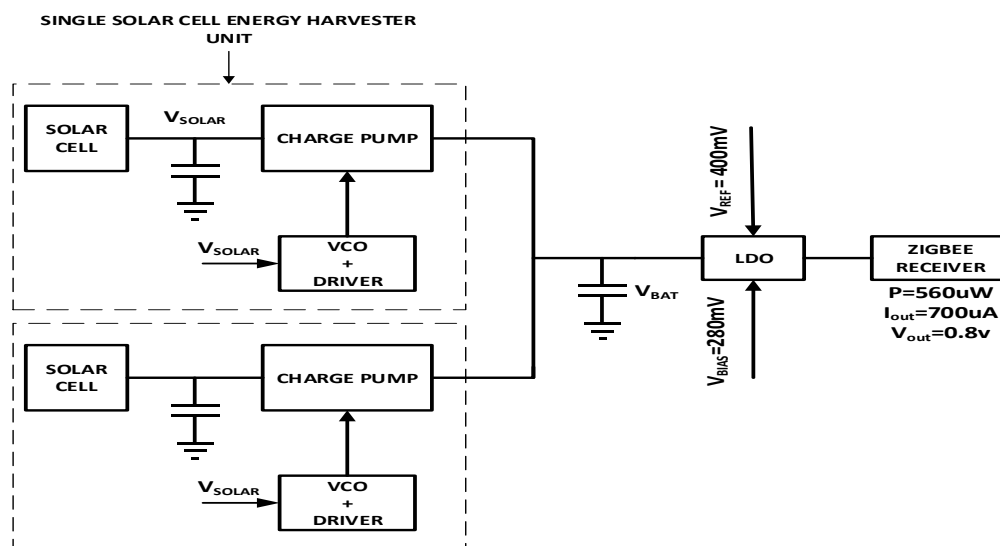


Figure 4.8 Application of energy harvesting

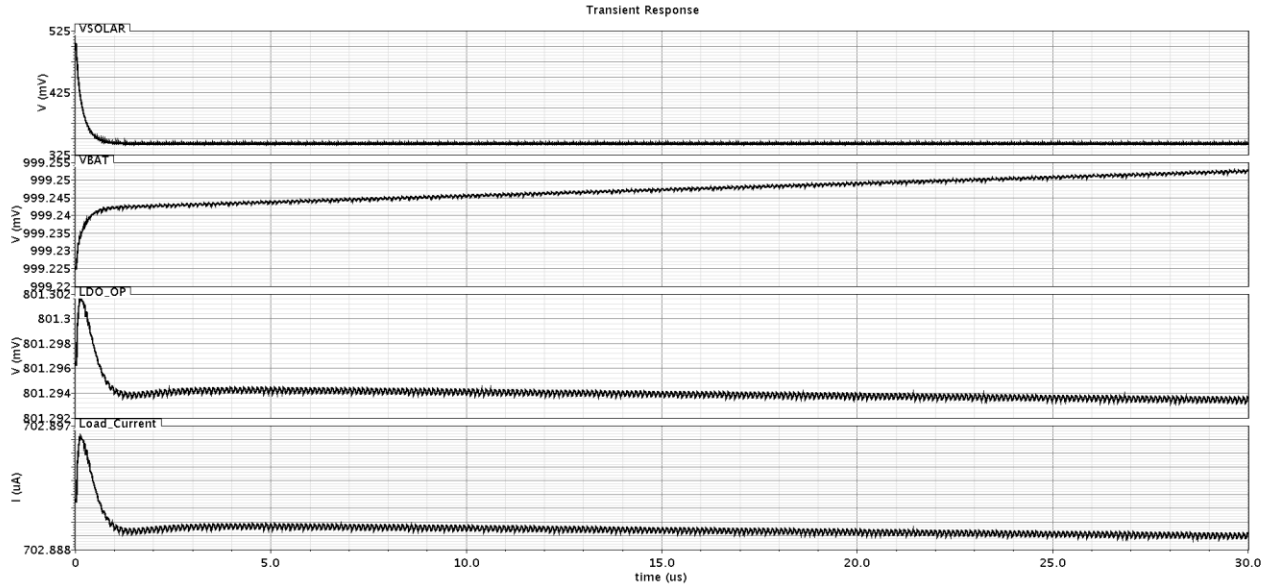


Figure 4.9 Simulation result of energy harvesting with LDO to drive 1.1K Ω

Fig 4.9 shows the result of two energy harvesters with 1V of battery voltage and LDO to drive the load of 0.8V. At LDO output we connected 1.1K of resistive load to check the output current. From Fig 4.9 it is clear that the output current is $\sim 700\mu\text{A}$ with increasing battery voltage. It means we are getting more power from the solar cell as compared to the power consumption by the load and the controller circuit.

It is evident from the fig.4.10 that the PLL lock in $30\mu\text{s}$ and the quadrature output is coming perfectly. Hence, it is proven that ZigBee receiver with energy harvester is working efficiently.

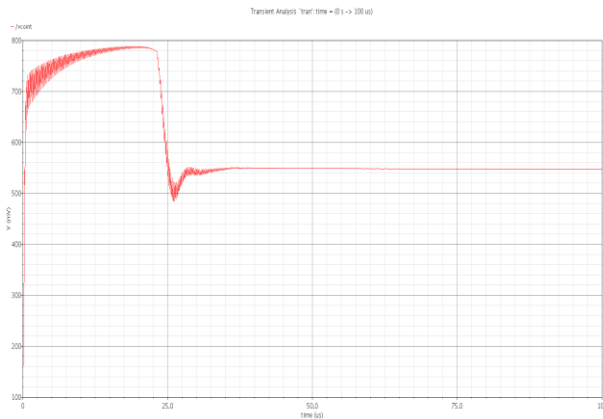


Figure 4.7 VCO locking to 2.4GHZ

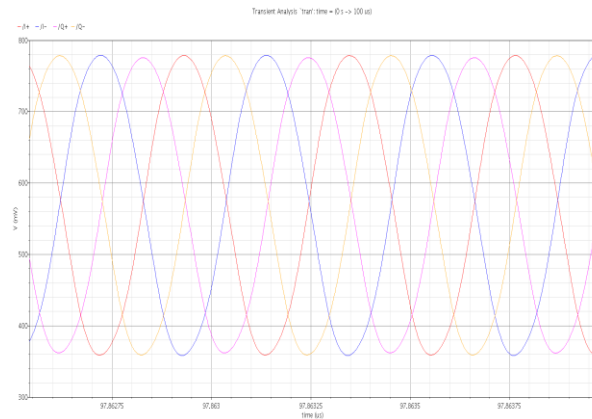


Figure 4.8 ZigBee RX quadrature output

Chapter 5

Conclusions and Future work

5.1 Conclusion

In this Master's Thesis, the work was focused on developing an Energy Harvesting system for indoor usage, capable of efficiently transferring the energy generated by the single solar cell to the storage element. The main issue with this kind of source are very low output power and inconsistency of power level. Furthermore this thesis successfully reached the established goals and completed the sequential tasks:

- To research and study the different DC-DC power converter for 1V battery case.
- Studied and Modified the Tree CP topology to achieve maximum efficiency at very low voltage.
- Studied and simulated with different flying capacitors (MIMCAP, MOSCAP, ZVT MOSCAP) of CP. Also, we concluded that the combination of ZVT and MOSCAP gives better efficiency with very small form factor and achieved maximum converter efficiency of 67% after parasitic extraction.
- To research and study the different MPPT methodology and we chose very low power effective MPPT so that it can work for indoor solar energy harvesting.
- Post layout Simulation of Tree CP with feed forward MPPT and achieved maximum efficiency of 51.8%.
- Proposed battery protection circuit for under voltage discharge and over voltage charging and input condition sensor to sense input power level.

- Designed startup circuit with minimum input voltage of 317mV and power of 847nW to charge $C_{STARTUP}$ capacitor up to 1V.
- All the blocks are brought together and simulation is performed to validate PMC with battery protection, input condition sensor and cold startup circuit and it is working successfully.
- The energy harvesting unit taped out successfully in UMC 180nm technology with PMC, battery protection circuit, input condition sensor and cold startup circuit.
- Finally, to validate the system with load we connected to parallel energy harvesting unit followed by LDO to drive ZigBee R_X with specification of 0.8V supply and power requirement of $560\mu W$. We concluded that the energy harvesting system is driving effectively to ZigBee R_X without any loss.

5.2 Future Work

- Testing the chip in real environment
- Input protection circuit to protect devices from high input voltage/current
- Power reduction of sub-blocks module
- Integration of photo diode with energy harvesting unit to target particular application and to make the device compact
- Design of startup circuit to target very low input voltage
- Integration of startup circuit with all modules

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Code

```
clc;

R1=1e3;
R3=1e3;
R2=1e3;

for n=1:1000

    for m=1:1000

        for p=1:100

            if(0.278*R1<0.512*(R2+R3) && 0.278*(R1+R2)<0.512*(R3) && 0.298*R1<0.512*(R2+R3) &&
            0.298*(R1+R2)>0.512*(R3) && 0.678*R1<0.512*(R2+R3) && 0.678*(R1+R2)>0.512*(R3) &&
            0.698*R1>0.512*(R2+R3) && 0.698*(R1+R2)>0.512*(R3))
                R1
                R2
                R3
            else
                R2=R2+1;

            end
            break;
        end

        R1=R1+1;
        R2=1e3;

    end
    R1=1e3; R2=1e3;
    R3=R3+10;

end
```