Anodic Silicon Dioxide as a Mask Material for the Fabrication of Microstructures in Surfactant Added TMAH

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Approval Sheet

This thesis entitled "**Anodic Silicon Dioxide as a Mask Material for the Fabrication of Microstructures in Surfactant Added TMAH**" by **Ramachandrappa Muttannavar** is approved for the degree of Master of Science from IIT Hyderabad.

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Abstract

In the microelectromechanical system (MEMS) fabrication, silicon dioxide (SiO_2) thin films are most widely used for different applications such as etch mask, structural and sacrificial layers. One of the widespread applications is etch mask in alkaline etchants. In the synthesis of silicon dioxide thin films anodic oxidation method offers several advantages over the conventional deposition techniques such as room temperature deposition, low cost, simple experiment setup, etc. The present work aims to explore anodic SiO_2 thin films as etch mask material in surfactant added tetramethylammonium hydroxide (TMAH) solution for the fabrication of MEMS structures with sharp convex corners. Anodic oxidation of silicon is employed to grow oxide thin films at wafer-scale at room temperature. Thickness uniformity and refractive index are measured using ellipsometry. Etch rate of the oxide is investigated in 0.1% v/v of surfactant (Triton X-100) added 25 wt% TMAH at three different temperatures. Furthermore, the etch rate, etched surface morphology and undercutting at convex corner of {100} silicon wafer are investigated. Optical microscope is employed to inspect the etched surface morphology of {100} silicon and also to check the quality of the etched oxide surface. Undercutting and etch depth are measured using a 3D measuring laser microscope.

Contents

Page No

Declaration ---------- 2

Approval sheet ---------- 3

Acknowledgements ---------- 4

Abstract ---------- 5

1. **Introduction** ---------- 7
2. **Experimental details** ---------- 8
3. **Results and Discussion** ---------- 10
   - 3.1. Growth characteristics ---------- 10
   - 3.2. Ellipsometry characteristics ---------- 10
   - 3.3. Etch rate study ---------- 11
     - 3.3.1. Anodic oxide etch rate ---------- 11
     - 3.3.2. Etch rate of Si{100} ---------- 12
   - 3.4. Investigation of etched surface morphology---- 13
     - 3.4.1. Anodic silicon dioxide ---------- 13
     - 3.4.2. Si{100}surface ---------- 14
   - 3.5. Undercutting at convex corner ---------- 16
   - 3.6. Fabrication of MEMS structures ---------- 17
4. **Conclusions** ---------- 19
5. **References** ---------- 21

Lists of figures

Figure 1: Schematic of anodic oxidation of silicon experiment set-up.

Figure 2: Constant temperature bath for anisotropic etching of silicon.

Figure 3: Cell voltage *vs* oxidation time for the oxide deposited in 2.7 vol% water added electrolyte at 8 mA/cm^2.

Figure 4: A comparison of film thicknesses measured at five different spots for the oxide deposited in 2.7 vol% water-added electrolyte at 8 mA/cm^2, 300 V.

Figure 5: Etch rate of anodic silicon dioxide in 0.1 vol% surfactant added 25 wt% TMAH at different temperatures.

Figure 6: Etch rate of Si {100} in 0.1 vol% surfactant added 25 wt% TMAH at different temperatures.

Figure 7: Optical micrographs of anodic oxide Surface after two hours etching at different temperatures (a) 60 ˚C (b) 68 ˚C (c) 76 ˚C.

Figure 8: Surface roughness of Si {100} in 0.1% v/v surfactant added 25 wt% TMAH at different temperatures.

Figure 9: Optical micrographs of silicon {100} surface after two hours etching at different temperatures (a) 60 ˚C (b) 68 ˚C (c) 78 ˚C.

Figure 10: Undercutting of convex corner along silicon <110> direction in 0.1 % v/v surfactant added 25 wt% TMAH at different temperatures, etching time: 2 hours.

Figure 11: Optical micrographs of <110> direction oriented cantilever after etching of two hours in 0.1 vol.% surfactant added TMAH solution at different temperatures (a) at 60 ^{o}C (b) at 68 ^{o}C (C) 76 ^{o}C.

Figure 12: Sample preparation procedure.

Figure 13: Various shapes microstructures fabricated in 0.1 vol% surfactant added 25 wt% TMAH at 76 ˚C, etching time: 2 hrs.

1. Introduction

Silicon dioxide (SiO_2) thin films are most extensively used insulating films in the manufacturing of silicon-based semiconductor devices, integrated circuit (ICs) for different applications such as gate component in metal oxide semiconductor (MOS) transistors, masking layer against diffusion and implantation of dopants in the silicon [1, 2], isolation of devices [3], etc. In the microelectromechanical systems (MEMS) fabrication silicon dioxide (SiO_2) thin films are most widely used for different applications such as etch mask, structural and sacrificial layers. One of the widespread applications is etch mask in alkaline etchants. Silicon dioxide thin film is preferred over other dielectric films due to its ease of synthesis, excellent insulating properties and high quality Si-SiO_2 interface. Thermal oxidation technique is known to provide high quality SiO_2 film and hence widely employed [4]. However, high processing temperature (~900-1100˚C) of this technique causes redistribution of dopants in silicon substrate during oxide growth and develop stress in silicon substrate that leads to wafer warpage [5-7]. Several new synthesis routes have been developed to reduce the process temperature. Atmospheric pressure chemical vapour deposition (APCVD) [8], plasma enhanced chemical vapour deposition (PECVD) [9], sputtering [10], wet anodic oxidation [11-14], liquid phase deposition (LPD) [15], sol-gel [16], etc. are few of the low temperature thin film deposition techniques. Each and every process has its own advantages and disadvantages. Among these low temperature techniques, anodic oxidation is one which can be operated even below room temperature [17]. Numerous research groups have investigated anodically grown oxide thin films for gate dielectric component in MOS devices [11, 14, 18]. Anodic oxidation process has several advantages over other techniques such as low cost, simple experimental set-up, room temperature process which minimizes the dopants redistribution, does not involve any toxic and expensive gases, etc.

In the present work, uniform SiO_2 thin film is grown at wafer-scale using anodic oxidation of silicon technique at room temperature. In order to explore anodic SiO_2 thin films as etch mask in surfactant added tetramethylammonium hydroxide (TMAH) solution for the fabrication of MEMS structures with sharp convex corners, the etch rate of the as-grown oxide is investigated in 0.1% v/v surfactant added 25 wt% TMAH at three different temperatures.

2. Experimental Details

Czochralski (Cz) grown three inch diameter P-type boron doped (resistivity 1-10 Ω cm) {100} oriented single side polished silicon wafers are used for the deposition of silicon dioxide using anodic oxidation at room temperature. Aluminum is deposited on the rough surface side using DC sputtering technique for ohmic contact purpose. In the present work, two-electrode electrochemical setup is utilized for the oxide deposition, the experimental setup utilized is as shown in the Fig. 1. A customarily designed wafer holder which provides gold contact on the back-side of the wafer is fixed as anode and the platinum gauge mesh (90% Pt, 10% Ir) as cathode. The distance between the two electrodes is kept 1.5 cm in the experiment. The design of the wafer holder is such that the 2.4 inch (6.09 cm) diameter area of three inch wafer surface is exposed to the electrolyte solution. Ethylene glycol solution containing 0.04M KNO_3 is used as an electrolyte. A small quantity, 2.7 vol% water is added into the electrolyte. The *pH* of the solution is maintained at 4.

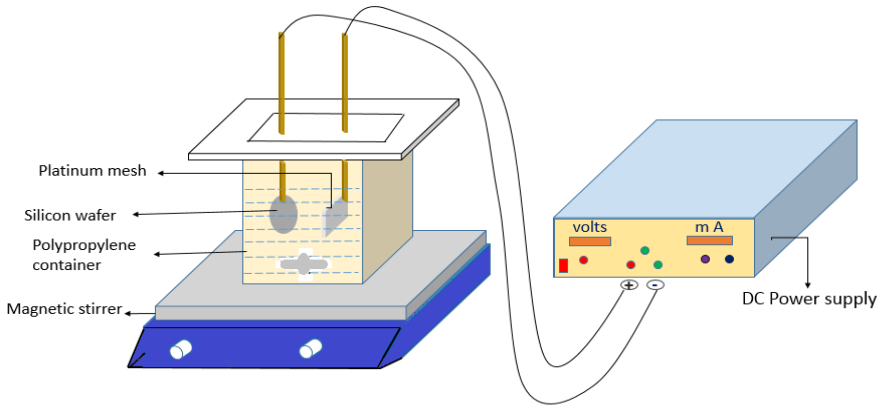


Figure 1: Schematic of anodic oxidation of silicon experiment set-up.

The deposition of oxide is executed in potentiodynamic mode in which the oxidation is carried out at constant current density of 8 mA/cm^2. In this mode, anodic oxidation is continued till the final voltage reaches to the predetermined voltage of 300 V. Thereafter, the process is continued in constant voltage (i.e. potentiostatic) mode at 300 V for 15 minutes. The variation in cell voltage during oxide growth is recorded at one minute intervals. Prior to anodic oxidation process, silicon wafers are ultrasonically cleaned sequentially in acetone and deionized water (DI) for 5 minutes

followed by removal of native oxide in 2% hydrofluoric acid (HF) and a thorough rinse in DI water. After the oxidation process, the oxidized samples are thoroughly cleaned in DI water to get rid of the adsorbed glycol solvent from the oxide surface. The oxide films deposited in 2.7 vol% water added electrolyte is patterned using UV photolithography (Midas Mask Aligner, model: MDA 400 M) for the fabrication of microstructures. The wafers are diced into small chips. Ellipsometry (J.A. Woolam, model: M-2000D) is employed to determine the thickness and the refractive index of the as-grown oxide. 0.1 vol% surfactant (Triton X-100) added 25 wt% TMAH (99.999%, Alfa Aesar) is used as etching solution. All etching experiments are performed in a Teflon container equipped with reflux condenser to prevent evaporation of solution (or to avoid concentration change) during etching process. The vessel is partially inserted in constant temperature water bath is as shown in Fig. 2. The samples are held vertically in a PFA made chip holder containing multiple slots in order to etch several samples at a time. Etching experiments are carried out at 60, 68 and 76 ˚C with the temperature accuracy of ±0.5 ˚C. The etch rates are calculated by measuring film thickness before and after etching using ellipsometry. Optical microscope (Olympus, model: STM6) is used to examine the quality of etched oxide surface and etched surface morphology of Si {100}. Etch depth, surface roughness and undercutting at convex corners are determined using 3D measuring laser microscope (Olympus, model: OLS4000).

Figure 2: Constant temperature bath for anisotropic etching of silicon.

3. Results and Discussion

3.1 Growth Characteristics

The variation in cell voltage during oxidation process is recorded for every minute and a graph plotted between cell voltage and anodization time. Fig. 3 presents the variation of cell voltage with time during anodic oxidation process. The curve in this figure represent the growth behavior of the oxide film deposited in 2.7 vol% water-added electrolyte at 8 mA/cm^2. It can be observed from the graph that the voltage increases continuously with time to draw the constant current until the forming voltage reaches the predetermined voltage i.e. 300 V. This behavior implies that the resistance of the film increases with oxidation time which is due to the increase of oxide thickness with time [19].

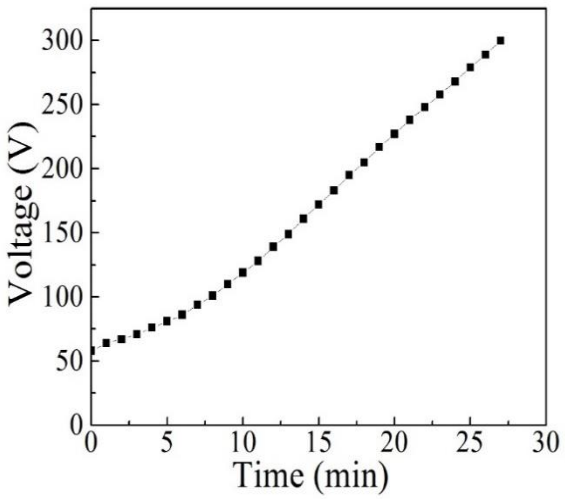


Figure 3: Cell voltage *vs* oxidation time for the oxide deposited in 2.7 vol% water added electrolyte at 8 mA/cm^2.

3.2 Ellipsometry Characterization

Spectroscopic ellipsometry is one of the widely used thin film characterization tools for measuring thickness, refractive index (n) and extinction coefficient (k) since it is non-destructive and contactless technique which avoids the sample damage. In this work, variable angle spectroscopic ellipsometry is used to measure the film thickness and its refractive index. The thickness of as-grown oxide films is measured at three different incidence angles of 65˚, 70˚ and 75˚. Thickness

of the film measured to be 155 nm. Furthermore, the analysis of the film thickness uniformity is performed by measuring oxide thickness at five different locations as shown in Fig. 4. It can be easily noticed that the film thickness is almost same at different locations, the variation in thickness is less than 8 Å which manifests high degree of thickness uniformity over the full 3-inch wafer.

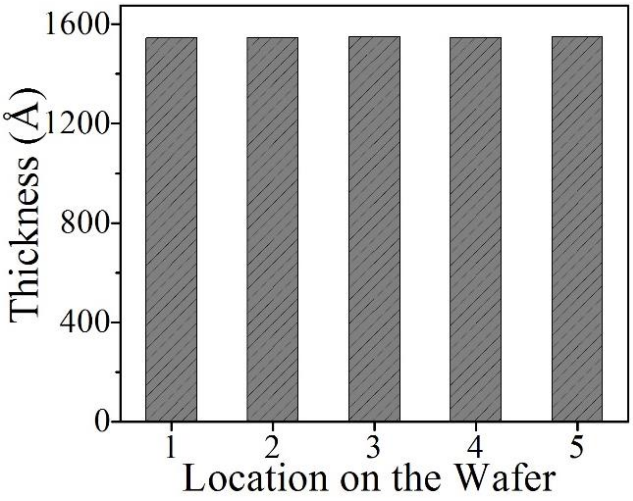


Figure 4: A comparison of film thicknesses measured at five different spots for the oxide deposited in 2.7 vol% water-added electrolyte at 8 mA/cm^2, 300 V.

The refractive index of the oxide film is measured using ellipsometry at fixed wavelength of 632.8 nm. For the as-grown anodic oxide, it is measured to be 1.47, which is slightly greater than that of the films deposited by thermal oxidation (1.462) [20]. A higher refractive index might be due to the high contents of silicon (or oxygen deficiency) in the as-grown oxide film [21].

3.3 Etch rate study

The etch rates of as-grown anodic oxide and Si{100} are investigated in 0.1% v/v Triton X-100 added 25 wt% TMAH at 60, 68 and 76 ˚C, they are presented in the following subsections.

3.3.1 Anodic oxide etch rate

The etch rate of the anodically grown oxide film is determined in 0.1% v/v surfactant added 25 wt% TMAH at three different temperatures. In order to determine the etch rate four samples are loaded at a time in the etchant and at every 30 minutes one sample is collected. Etch rate is

evaluated by measuring oxide thickness before and after etching using ellipsometry. Fig. 5 shows the etch rates of as-grown oxide film determined in 0.1 vol% surfactant added 25 wt% TMAH at 60, 68 and 76 ˚C. It can see from the figure that etch rate of the oxide increases with increase in the temperature.

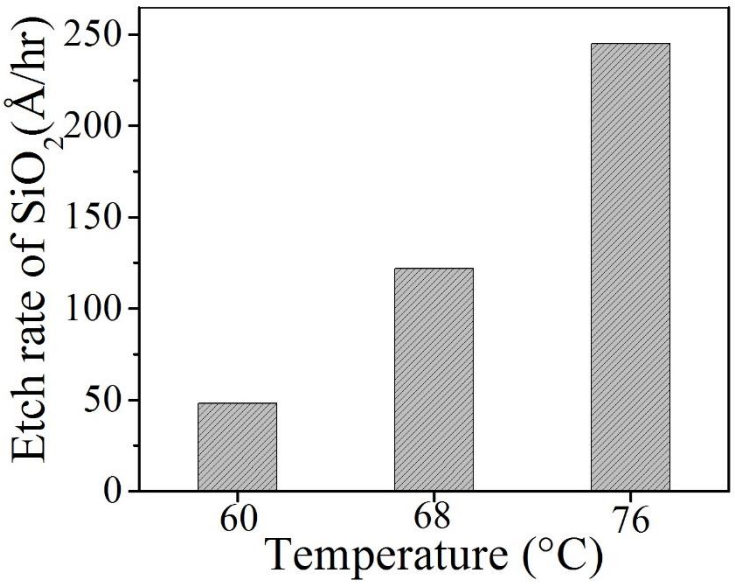


Figure 5: Etch rate of anodic silicon dioxide in 0.1 vol% surfactant added 25 wt% TMAH at different temperatures.

The increase in etch rate with temperature is due to improve in the wetting capacity of the etchant with temperature, as a result the etchant can easily diffuse to the sample surface consequently the etch rate increases with temperature [22].

3.3.2 Etch rate of Si{100}

The etch rate of Si{100} is determined in 0.1 %v/v surfactant added 25 wt% TMAH solution at three different temperatures. Etch rate is evaluated by measuring the etch depth after two hours of etching using 3D laser scanning microscope. Fig. 6 shows the etch rate of Si{100} in 0.1% v/v surfactant added 25 wt% TMAH at 60, 68 and 76 ˚C. From figure it can see that the etch rate increases as etching temperature increase. The reason for increase in etch rate with temperature is same as explained in the section 3.3.1. In the present work highest etch rate is observed at 76 ˚C.

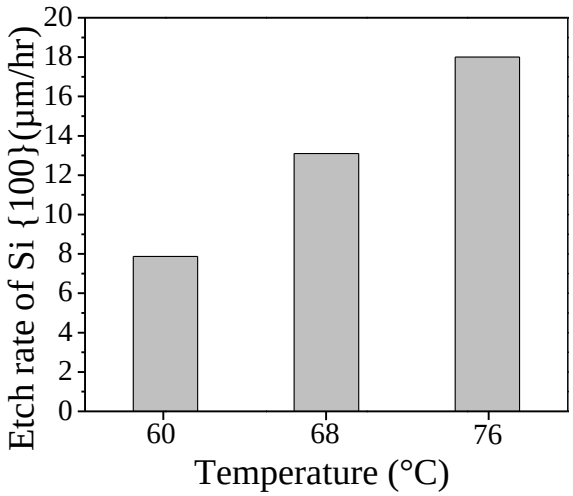


Figure 6: Etch rate of Si {100} in 0.1 vol% surfactant added 25 wt% TMAH at different

3.4 Investigation of etched surface morphology

The etched surface morphology is a major concern especially in optical MEMS and for the high efficiency solar cell. Surface roughness of the micromachined surfaces also influences the functionality of the fabricated microsystem devices. The etched surface morphology of anodic silicon dioxide as well as Si{100} surface after etching in the 0.1% v/v Triton added TMAH at different temperatures are inspected using Optical microscope and they are discussed in the following subsections.

3.4.1 Anodic Silicon Dioxide

It is important to inspect the etched oxide surface after etching in order evaluate the quality of the oxide. Fig. 7 illustrates the surface morphologies of the oxide etched at 60, 68 and 76 ˚C for 2 hours etching time. From the figure it can observe that at 60 ˚C the surface is smooth and pits free, as temperature increases pits starts forming, this is due to the small pinholes formed in the oxide during oxide growth and increase in the dissolution rate of the oxide with temperature.

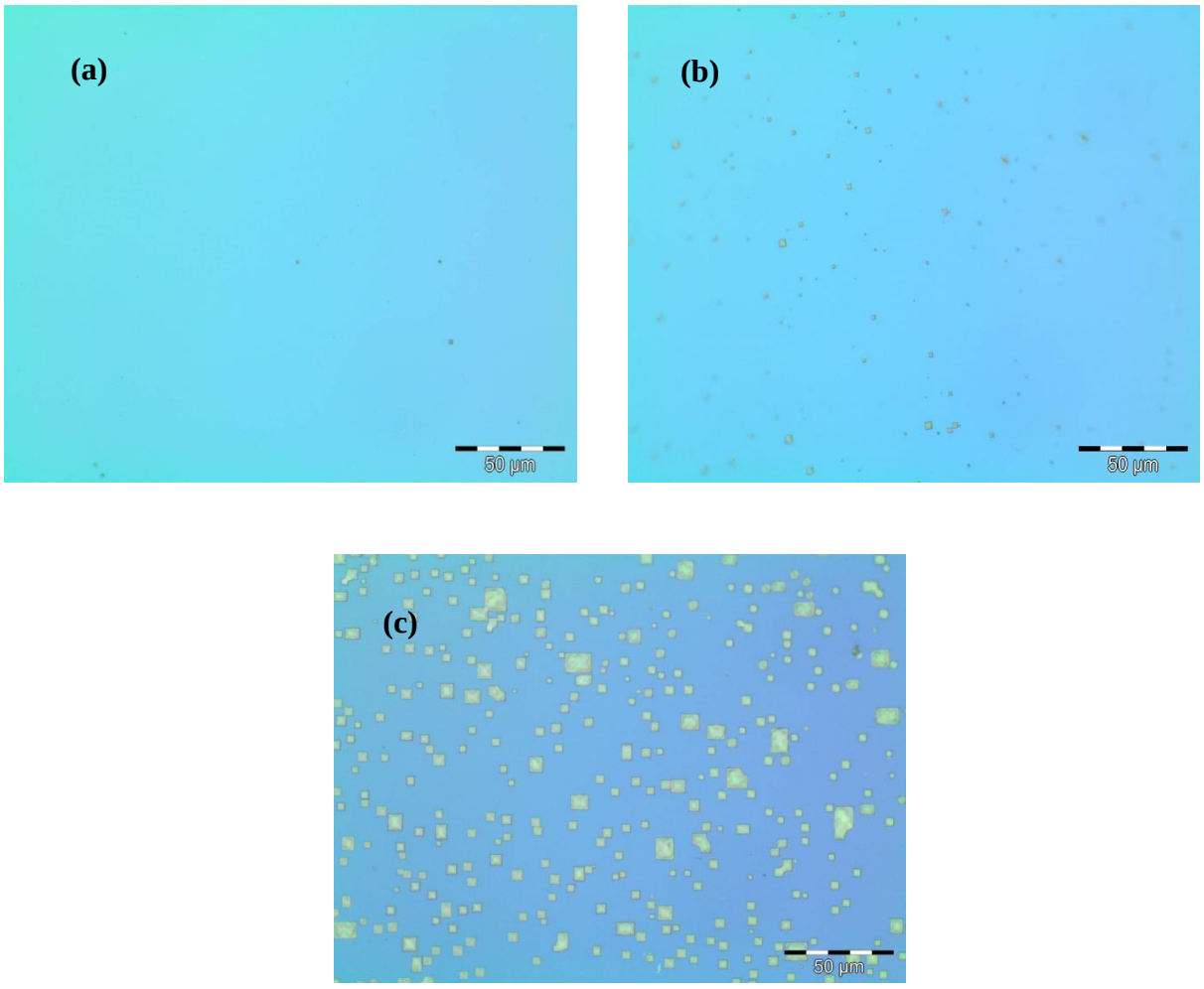


Figure 7: Optical micrographs of anodic oxide surface after two hours etching at different temperatures (a) 60 ˚C (b) 68 ˚C (c) 76 ˚C.

3.4.2 {100} Silicon Surface

The surface roughness of the etched Si{100) surface in 0.1% v/v surfactant added 25 wt% TMAH at 60, 68 and 76 ˚C is measured quantitatively using 3D laser scanning microscope. Fig. 8 shows the variation of the roughness with etching temperature after two hours of etching time. Fig. 9 shows the optical micrographs of the Si{100} after two hours of etching in 0.1% v/v surfactant added 25 wt% TMAH solution. From figure it can be easily identify that at 60 ˚C temperature surface is almost smooth, at 68 ˚C temperature hillocks starts forming and these are increasing as temperature increases to 76 ˚C. The hillocks forms due to sticking of hydrogen bubbles or etchant impurities on the sample surface, thus the etched surface roughness increases with the hillocks formation.

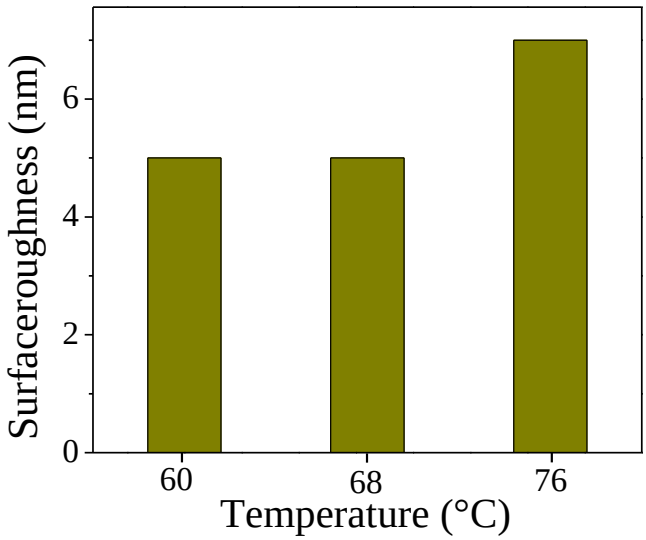


Figure 8: Surface roughness of Si {100} in 0.1% v/v surfactant added 25 wt% TMAH at different temperatures.

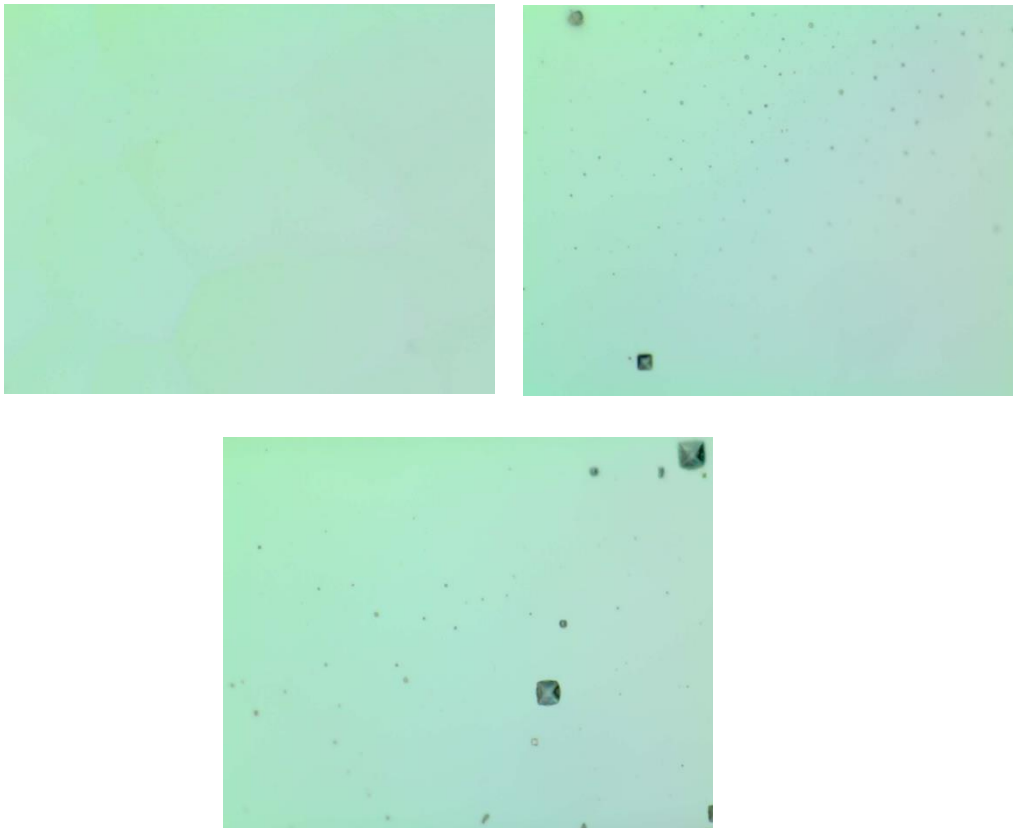


Figure 9: Optical micrographs of silicon {100} surface after two hours etching at different temperatures (a) 60 ˚C (b) 68 ˚C (c) 78 ˚C

3.5 Undercutting at convex corner

In bulk micromachined structures, two kinds of corners, namely, concave and convex, are frequently encountered. Their etching characteristics are completely opposite to each other. The convex corners in the mask patterns encounter significant lateral undercutting, while no undercutting is observed at the concave corners. A significant amount of research has been done in this area. The undercutting at the convex corners plays a major role in the fabrication of freestanding structures for example cantilever beam. This process helps to remove the underneath material. The undercutting rate defines the release time and therefore should be sufficiently high to minimize the etching time for the complete release of the structure. Whereas for the fabrication of proof masses for accelerometers, mesa structures and chip isolation grooves, the undercutting is highly undesirable where severe convex corner undercutting distorts the desired shape of the structure. The shape of the convex corner is preserved by providing additional (i.e. corner compensation) structures at the convex corner of regular mask pattern which is complex and time taking process. On the other hand, undercutting at convex corner can be considerably reduced by adding different types of additives into the anisotropic etchant (e.g. KOH, TMAH, etc.). The undercutting measured along the <110> direction at the convex corner in 0.1% v/v Triton added TMAH at 60, 68 and 76 ˚C for 2 hours of etching time is presented in Fig. 10, the corresponding optical microscope images of undercutting are presented in Fig. 11. From Fig. 10 & 11 it can be observed that undercutting increases with temperature.

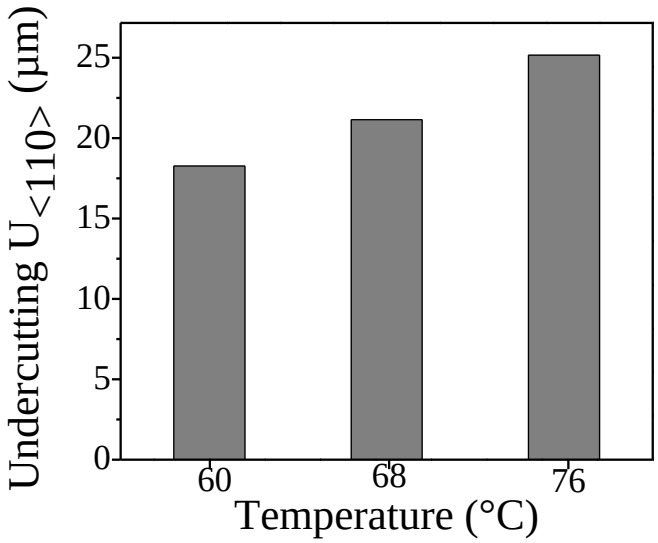


Figure 10: Undercutting of convex corner along silicon <110> direction in 0.1 % v/v surfactant added 25 wt% TMAH at different temperatures, etching time: 2 hours.

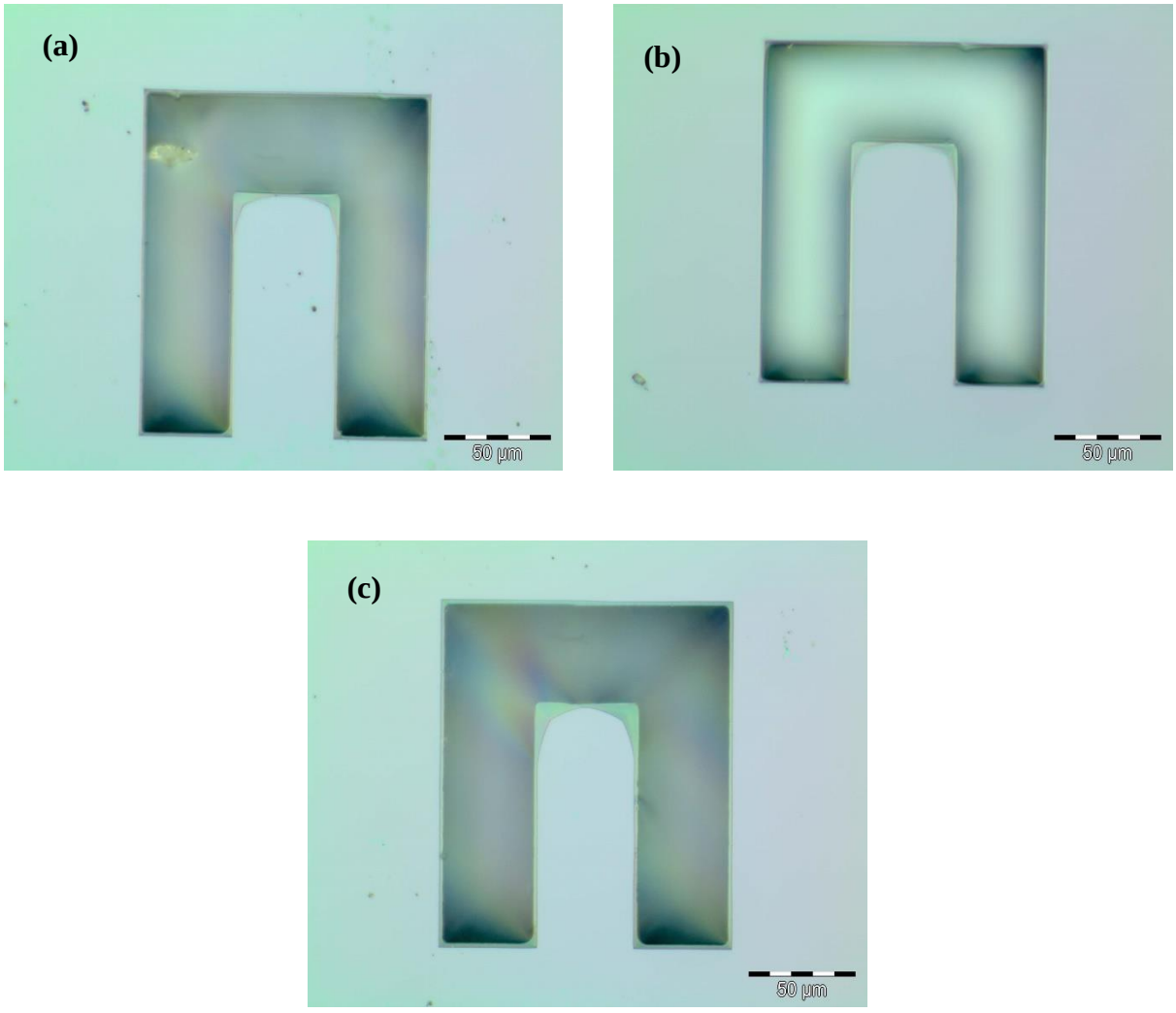


Figure 11: Optical micrographs of <110> direction oriented cantilever after etching of two hours in 0.1 vol.% surfactant added TMAH solution at different temperatures (a) at 60 ˚C (b) at 68 ˚C (C) 76 ˚C.

3.6 Fabrication of MEMS structures

In order to fabricate MEMS structures anodic silicon dioxide deposited silicon wafer is patterned using UV photolithography. The procedure of sample preparation is presented in Fig. 12. In photolithography process, mask edges are aligned parallel to <110>. The patterned wafer is diced into small chip sizes and etching is carried out in 0.1% v/v Triton added 25 wt% TMAH at different temperatures for different period of etching time. Fig.13 shows the different MEMS structures fabricated using anodic oxide as etch mask in 0.1 % v/v Triton added 25 wt% TMAH at 76 ˚C for 2 hours of etching time. From Fig. 13 it can observed that the undercutting is reduced at the convex

corner in surfactant added TMAH solution, this is due to the surfactant molecules adsorb as a dense layer on the high index planes at the convex corner. This surfactant layer inhibits the etchant to react chemically with the silicon atoms that results in dramatic reduction in the undercutting. From this study it is evident that anodic silicon dioxide can be used as etch mask for the fabrication of MEMS structures with almost sharp convex corners.

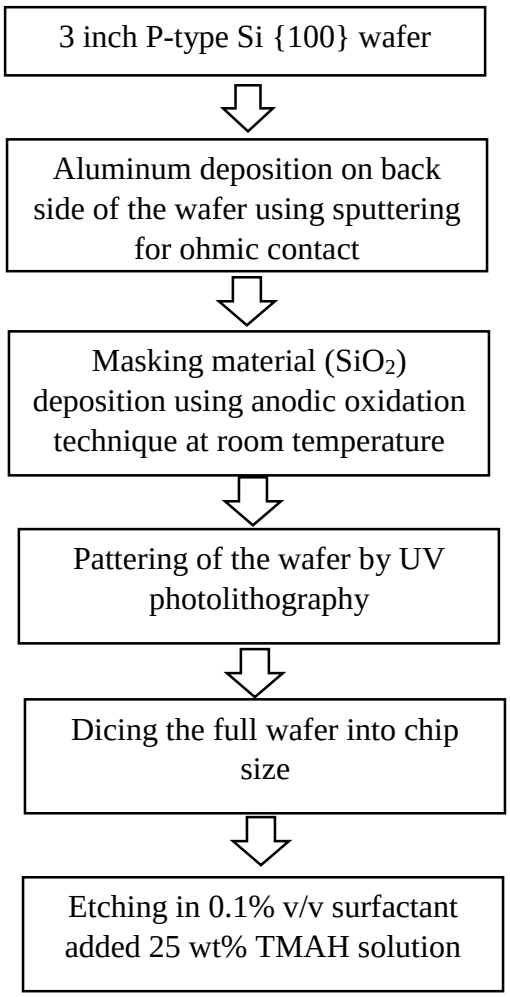
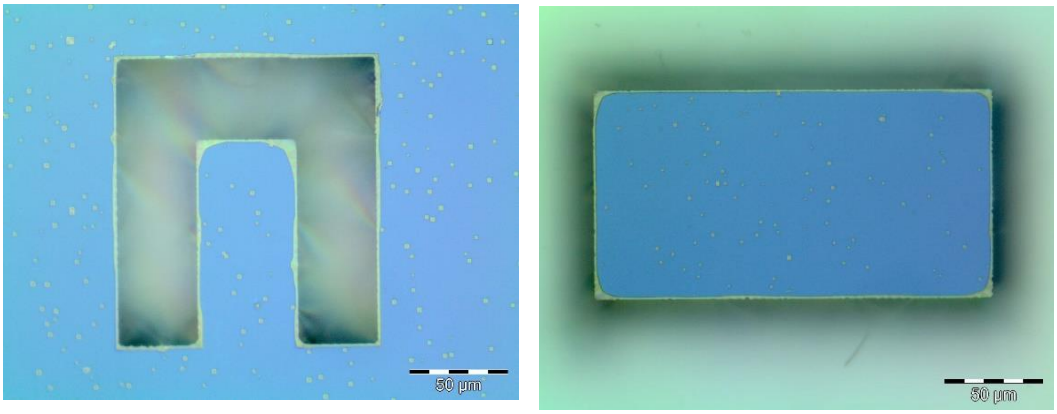


Figure 12: Sample preparation procedure.



(a) (b)

Figure 13: Various shapes microstructures fabricated in 0.1 vol% surfactant added 25 wt% TMAH at 76 ˚C, etching time: 2 hrs.

4. Conclusions

Silicon dioxide thin film is prepared on 3 inch wafer using anodic oxidation technique at room temperature. Ellipsometric measurements of the oxide film confirmed a high degree of thickness uniformity which is important parameter considered in MEMS fabrication. Refractive index of the as-grown oxide is slightly greater than thermally grown oxide film. The etch rate of the oxide increases with temperature. As temperature increases pits starts forming in the oxide. The as-grown oxide is demonstrated as etch mask for the fabrication of MEMS structures with sharp convex corners using 0.1% v/v surfactant added 25 wt% TMAH solution. Undercutting at convex corner and the etch rate of Si{100} increases as temperature increased. The surface roughness of {100} silicon worsens as temperature increased, at 76 ˚C the surface is covered by small hillocks.

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