ANALOG FRONT END FOR RF ENERGY HARVESTING

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Contents

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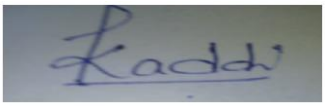

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Approval Sheet

This thesis entitled Analog front end for RF energy harvesting by Pramod Kaddi is approved for the degree of Master of Technology from IIT Hyderabad.

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Dedicated to

To my parents, Brother and
Sisters

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Abstract

This thesis proposes a design for ultra low power sensitive single and dual band RF energy harvesting system for UHF microwave frequencies at 2.4-GHz and 865-MHz to 960- MHz(ISM band). The system is designed to power a load and generate a constant 1-V output voltage for a battery-less passive energy harvesting circuit. Input power is fed from 50 RF source to emulate antenna at UHF microwave band. The design includes single band and dual band off-chip RF matching circuit, RF limiter, Differential Rectifier, Power On Reset (POR), Band Gap Reference (BGR) and Low Drop Out Regulator (LDO). The number of rectifier stages is optimized to obtain a better efficiency to generate 1V output voltage. The full system performance has been verified by simulations for equivalent received power from -20-dBm to -10-dBm. The overall RF energy harvesting system efficiency at -14-dBm (10 m Distance from 4W EIRP source) input power for single band matching at 2.4-GHz is 46.9% with 54Kohm load and for dual band matching at 953-MHz and 2.4-GHz we achieve an efficiency of 41.5% with 61K ohm load and 46% with load 54.4Kohm respectively. The technology node employed is 0.18_m technology. The simulations are carried out at schematic level with bond wire parasitic's and verified by post layout simulation. At the last we conclude by proposing a novel architecture for constant voltage battery charging.

Chapter 1
Introduction to RF energy Harvesting

Introduction: The conventional sources of energy like wind, light, water are employed for macro scale generation that serves day today needs. There exist need for micro scale energy harvesting also as more information is prone in areas which are out of reach or inhabitable. So it is becoming increasingly difficult to meet the energy needs for next generation applications which require energy in micro scale. The important sources of energy harvesting in micro-scale are solar, vibrational energy, thermo-electric energy which are available to power ULP (ultra low power) consuming devices. The basic source of harvested power is derived from environmental sources however at times energy from these sources is intermittent, unconditional and at micro scale.

A decade ago micro-scale energy harvesting could be fiction. The ever changing world has pushed through limits due to advances in device physics and scaling down of devices caused ultra-low-power (ULP) energy technology harvesting that has turned into reality. The ultra low power RF energy harvesting is bit challenging but its recent commercialization has pushed the designers to think beyond barrier make it a available. The RF energy harvesting technology is rapidly expanding field. The applications include usage in modern day wireless sensor nodes, RFID tags[1] used for advanced near field communication (NFC) system, supply chain, logistics, wear-able[2]and implantable devices[3] for pervasive computing within surveillance area for remote vital health signal monitoring applications[4] close to a RF source. These RF energy harvesting systems are classified into passive, semi-passive, active tags. The active systems use battery for long range communication and it incorporates a sensor that should be powered by battery. However the semi passive RF energy harvesting also includes a battery and communicates to the base station via back scatter communication technique. However the use of active and semi passive battery powered electronic devices for above applications have issues related to limited charging cycles and increase in the size and the cost of devices. Hence a passive RF energy harvesting system can mainly employed in the mentioned applications.

Radio frequency energy harvesting is fruitful whenever certain radiating source is available nearby (at distance of 10m min) as the amount of energy radiated by the source is restricted by band and is

decided by regulations of the country. Generally for RF energy harvesting is utilized in HF (13.56 MHz), UHF band (860-960 M Hz) also called as ISM band (Industry Scientific and Medical usage) along with 2.4 G Hz band. The RF energy harvesting can be majorly employed in RFID tags which are used in supply chain management, public transportation, library, checkout, building access and airport baggage control. There is also inching interest of utilizing RF energy harvesting for Wireless sensor networks also.

The most important requirement of RF energy harvesting system is extended life and minimum sensitivity without usage of any sort of storage element. Modern RF energy Harvesting circuit are used at high frequencies namely 860 MHz to 960 MHz and 2.4GHz which allows the utilization of smaller antennas and larger bandwidth of transmission. The major obstacles in such UHF energy harvesting system is impact of substrate parasitic increase as we move towards design of high frequency integrated circuits, another Effective Isotropic Radiated Power (EIRP) where power loss increases as wavelength decreases.

1.1 Aim and Motivation

There exists need to design of Ultra low power RF energy harvesting that can power remote wireless sensor nodes, biomedical devices which may be either implantable or or wearable devices. The requirement of such systems is to generate power with smaller form factor and low power consumption

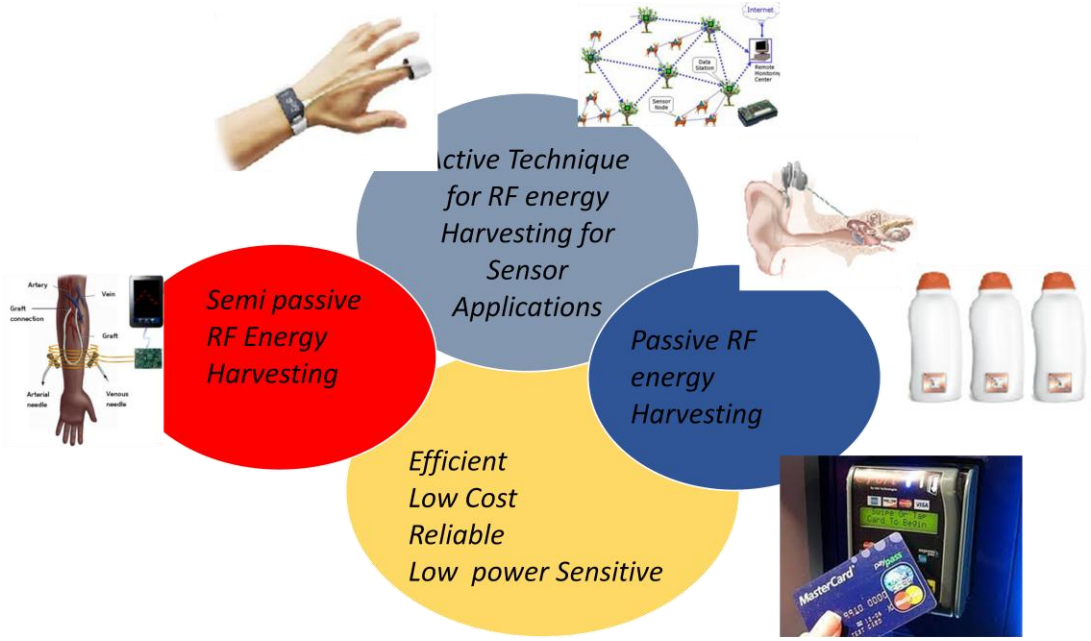


Figure1.1. Aim and Motivation

A typical energy harvesting system consists of a Antenna, AC- DC converter and power conditioning circuit and load consisting of charging and discharging source. The antenna is used capture radiation emitted by source may be RF reader and converters the electromagnetic energy in to the electrical energy in terms of voltage which is fed to the AC-DC converter. However to harvest RF energy use UHF ISM band(850MHz -960MHz), microwave(2.4GHz) for energy harvesting will lead to reduced antenna sizes, achieve a higher data rates adding advantage to further miniaturize and high performance wireless pervasive system. However regulations set on EIRP and path loss at higher frequencies limit the amount of power received by these devices with distance away from RF source. As such power received by any such devices will be in the range of 100uW (- 10dBm) and 10uW (-20dBm).

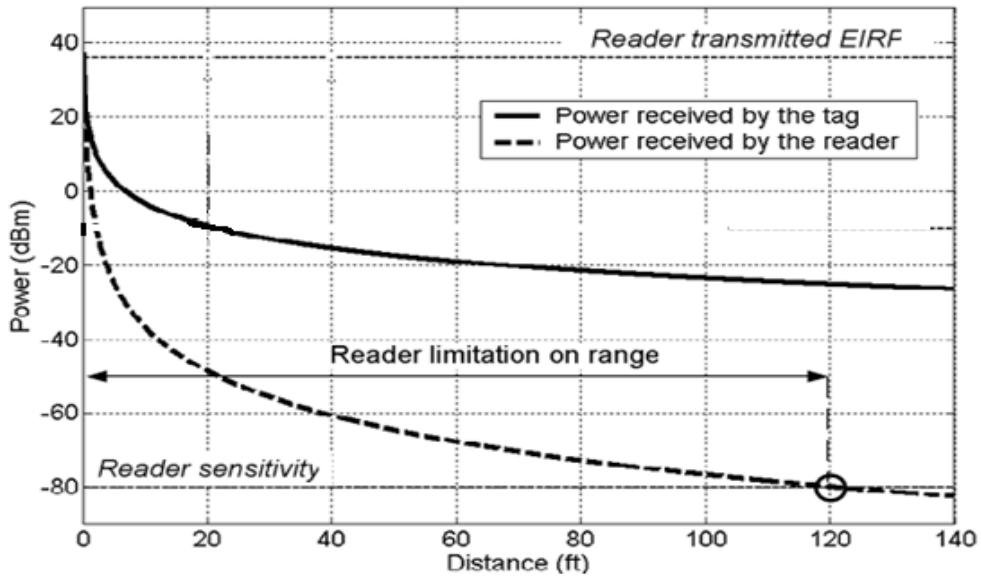


Figure 1.2 shows the Power in dBm vs. distance from Reader in standard RFID system.

1.2 Literature Survey

The major work in case RF energy harvesting chipset are done for passive RF energy harvesting as circuits are more reliable, have a long life, and less costly to the as they are not powering sensors as well as battery continuously. The work done till now consists of the single band RF energy harvesting. In this work we propose the scheme for RF energy harvesting scheme that can be employed in case Amplitude Shift Keying methodology as well as Frequency Shift Keying FSK reliably because of the dual band nature of the energy harvesting. In case of ASK we can employ

simple envelop detector for demodulating and can use a single band for Signal transmission. However we can use the dual band energy harvesting more efficiently for FSK modulation.

There a dual band RF energy harvesting should be employed should have comes in advantage with smaller form factors.

The amount energy available in case of the different Energy harvesting schemes are mentioned in Table.1 [19] which gives a approximate estimation of the energy that is available. The ambient light varies in case of indoor and outdoor as mentioned in table however the availability is intermittent and cannot be reliable because variation in weather as well as it not available during 50% of 24 hours in a day. However the as the resistance of varies with illumination so the requires a Maximum Power Point Tracking MPPT circuit for efficiently harvesting the energy from the solar cell. The MPPT unit continuously consumes power to generate the clock for the power converter. The solar energy harvesting scheme employs DC-DC converters name charge pump circuits namely Dickson charge pump, Fibonacci charge pumps with two phases to up convert dc voltage that is generated to power the load. In case vibrational energy can be harvested due human motion whose frequency varies in Hz to the Machines that generate vibrations in terms of Kilo Hertz. In here the problem is that it cannot be accessed in remote areas however it efficient for fault detection circuits embedded in machines. This scheme a better efficient transducer along with a cascade stages of rectifier circuit to harvest energy. The next available source of energy is temperature difference which can be employed in industries as well as incase smaller scale for biomedical applications where we harvest energy from a human body also. In all the mentioned applications are costly as they require efficient transducers.

Energy Sources	**Harvested Power**
Vibration/Motion	
Human	**4μW/cm^2**
Industry	**100μW/cm^2**
Temperature Difference	
Human	**25μW/cm^2**
Industry	**1-10mW/cm^2**
Light	
Indoor	**10 μW/cm^2**

Outdoor	**10mW/cm^2**
RF	
GSM	**0.1 µW/cm^2**
WiFi	**0.001 µW/cm^2**

Table 1.1 Available Sources of Energy

The Keyrouz et al[5] proposed a multi band energy harvesting scheme at -15 dBm input power having an system efficiency of 45 % at 900 MHz, 46 % at 1800 MHz and 25 % at 2.45 GHz. The overall system includes multiple sub systems powered by different antennas with individual off chip matching network, rectifier, and power management circuit leading to large aspect ratio of chip. Bo Li et al [6] group have proposed the another scheme for dual band energy harvesting at -19.3dBm input power level with efficiency for 12 % and 11 % at 900MHz and 1800MHz. Similar to Keyrouz et al[5] they use separate chain of matching and rectifier circuits to charge the battery. The Phirun Kim et al [7] proposed dual band RF energy harvesting scheme with an efficiency of 73.76 % and 63.06 % at 881MHz and 2.4GHz. However above scheme is sensitive at very high input power level of 160mW (22dBm) which does not suffice requirement for the wearable devices that are employed for 10m and above communication range. The Phongcharoenpanich et al [8] proposed a dual band antenna design for UHF RFID bandwidth 911-925.6 MHz, 2.32GHz-2.52GHz with respective directivity of 8.33dBi and 9-10.5dBi.

1.3 Contribution of Thesis

The work mainly focuses on reliable and efficient utilization of the harvested power in micro-scale to power ultra low power systems. The main contribution of the thesis is towards

- A novel dual band RF energy harvesting that can be powered by two different frequencies operating one at a time to drive a load continuously.
- A novel and efficient architectural scheme for power management for charging a battery to the higher voltages.
- The scheme was verified by the layout level simulations taking bond wire parasitic into the account.
- The novel architecture is being proposed which employs both rectifier and charge pumps for harvesting energy.

Chapter 2

Generation of Constant Supply Voltage for Driving a Load.

2.1 Introduction

The typical RF energy harvesting scheme employed for micro-scale transducers is that can be to drive a load circuit with a constant voltage is given below.

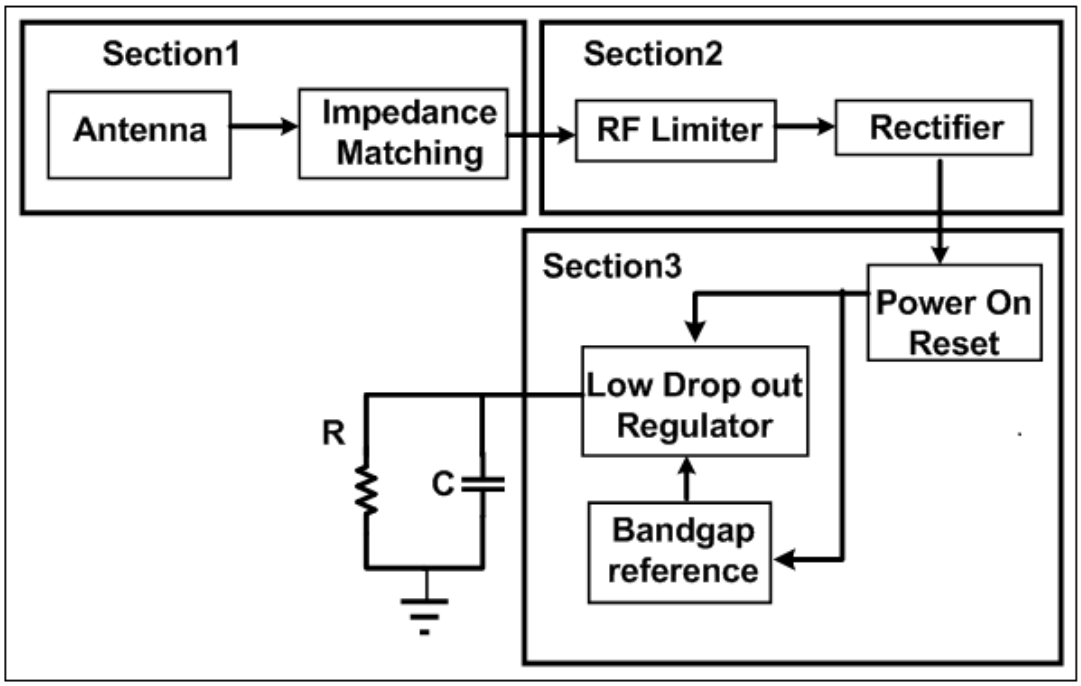


Figure 2.1 shows the architecture of complete system

The organization of next part of thesis is designed so that the upcoming chapters describe each of the section in detail in each chapter.

In this chapter we will cover in detail the first section of RF energy harvesting architecture that consists of the Antenna and Matching circuit.

2.2Antenna:

The requirement in our case is design of antenna which single band or dual band antenna that is needed to be matched to load i.e. RF energy harvesting circuit. The antenna circuits are generally

customized and designed to have a conjugate impedance of that of impedance measured by network analyzer of the designed chip [16]. Otherwise then there exists a requirement to match an antenna to RF energy harvesting system by interfacing with an impedance matching circuit. But in case of dual band RF energy harvesting we cannot customize the antenna to match the load requirements at two different frequencies there by pressing the need for the dual band impedance matching network. The Phongcharoenpanich et al [8] proposed a dual band antenna design for UHF RFID bandwidth 911-925.6 MHz, 2.32GHz-2.52GHz with respective directivity of 8.33dBi and 9-10.5dBi.

There are dual band antennas that can be interfaced to RF Energy harvesting. The Phirun Kim et al [7] proposed dual band RF energy harvesting scheme with an efficiency of 73.76 % and 63.06 % at 881MHz and 2.4GHz. However above scheme is sensitive at very high input power level of 160mW (22dBm) which does not suffice requirement for the wearable devices that are employed for 10m and above communication range.

2.2.1 Model for the antenna:

Antenna Impedance

The input impedance of an antenna is impedance seen from the antenna terminals. The antenna impedance will be affected by the ambience/objects around it. Here in our case we assume it is free from objects that tend to vary antenna impedance.

The impedance seen from antenna terminals consists of both real and imaginary part and is given by the equation mentioned below.

$$Z_{antenna}=R_{r+\Omega}+jX_{antenna}. \quad (1)$$

The antenna that receives the RF signal and having impedance $Z_{antenna}$ is connected to load impedance Zin. The strength of the RF signal received by antenna transducer is given by Va. The power delivered to the load is given by P_{load}

$$Pload = \frac{1}{2} Re(V^*_{in} I_{in}) \quad (2)$$

The Z_{in} is given by complex impedance $=R_{in}-jX_{in}$

Then P_{laod} is given by

$$P_{laod} = \frac{1}{2} Re\left\{\frac{V_a^2 (R_{in}-jX_{in})}{|R_{in}+R_{antenna}+j(X_{antenna}+X_{in})|^2}\right\} = \frac{1}{2} Re\left\{\frac{V_a^2 (R_{in})}{(R_{in}+R_{antenna})\text{^}2+(X_{antenna}+X_{in})^2}\right\} (3)$$

From the above equation we can derive that

$$P_{load} = \frac{V_a^2(1-|\Gamma|^2)}{8R_a} \quad (4)$$

Where Γ represents the reflection coefficient given by

$$\Gamma = \frac{Z_{in} - Z_{antenna}}{Z_{in} + Z_{antenna}} \quad (5)$$

If we assume the power that the load receives from the antenna under the condition the antenna is connected to the matched load ($Z_{in}=Z_a$, $R_{antenna}= R_{in}$.). The P_{load} , P_{avail} is given by

$$P_{avail} = \frac{V_a^2}{8R_a} \quad (6)$$

$$P_{load} = P_{avail}(1 - |\Gamma|^2) \quad (7)$$

2.2.2 Power Transfer in Free Space

The regulations on Effective Isotropic Radiated Power (EIRP) along with increase in path loss due to decrease in wavelength in particular range of operation limits the amount of energy received by the energy harvesting system. If we assume that transmitting antenna is capable to transmit power equal to Pt with gain Gt and gain of receiving antenna is Gr in

$$P_r = \frac{P_t G_t G_r \lambda^2}{(4\pi d)^2} \quad (8)$$

In case of RF technology domain we use a term Effective Isotropic Radiated Power EIRP which decides the licensing regulations of the specific country. It provides a notion how better (represented by transmitting antenna gain G_t) a transmitting antenna is compared to isotropic antenna and is given by

$$P_{EIRP} = P_t G_t \quad (7)$$

In the equation Pr, λ represents power and wavelength of the transmitted signal. The d is distance between the source of transmitter and the receiving antenna. However in practical case the amount of energy received by the receiving antenna decays in third order because of the obstructions and the absorption by objects nearby receiving antenna. The P_{avail} the available for the matching load is given by ($Z_a=Z_{in}$*) is given by

$$P_r = \frac{P_t G_t G_r \lambda^2}{(4\pi d)^2} = \frac{V_a^2}{8R_a} \quad (8)$$

The equivalent model of antenna is shown in Figure 2.7

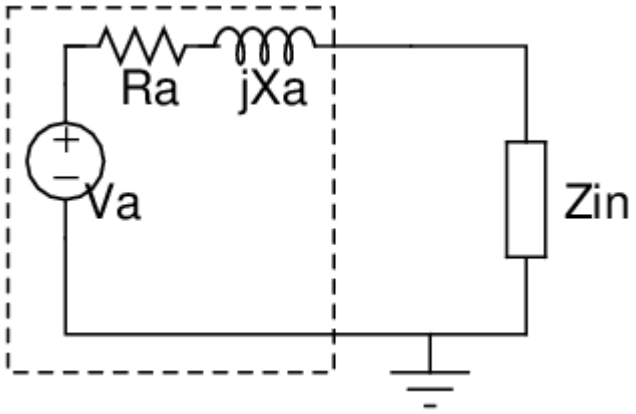


Figure 2.2 Antenna Model

In India, North America the EIRP 4W however in major parts of Europe it is 1W.

The above discussion helps us to model the simple antenna by power source in series with a resistance and equivalent inductive impedance. However for the ease of simulation it was model by port in series with resistance of 50Ω.The voltage available at the load is given by above equation which can be modified and can be written as

$$V_a = \sqrt{8R_{antenna}P_{avail}} \quad (9)$$

The Radiation resistance of antenna varies with physical dimensions and RF wavelength. In case of dipole antenna where length of antenna is less than quarter wavelength then it is given by

$$R_a = 20\frac{L}{\lambda}\pi^2 \quad (10)$$

The λ=C/f. Where f is the frequency of the operation and c is speed of light in free space. For 900MHz the length of antenna is about 7.5cm as the wavelength is about 33.3 cm.

The value of Radiation resistance of the antenna can be 10 to 100's of ohms.

2.3 Matching Circuit:

The primary function of impedance matching is to reduce the reflection between antenna and rectifier circuit allowing the maximum power transfer to the load. It must also provide a voltage resonance at frequency of the interest there by increasing the sensitivity of the system. The P_{avail} is power available at input terminals of antenna; P_{load} power delivered to the load is given by equations below

$$P_{load} = P_{avail}(1 - |\Gamma|^2) \quad (11)$$

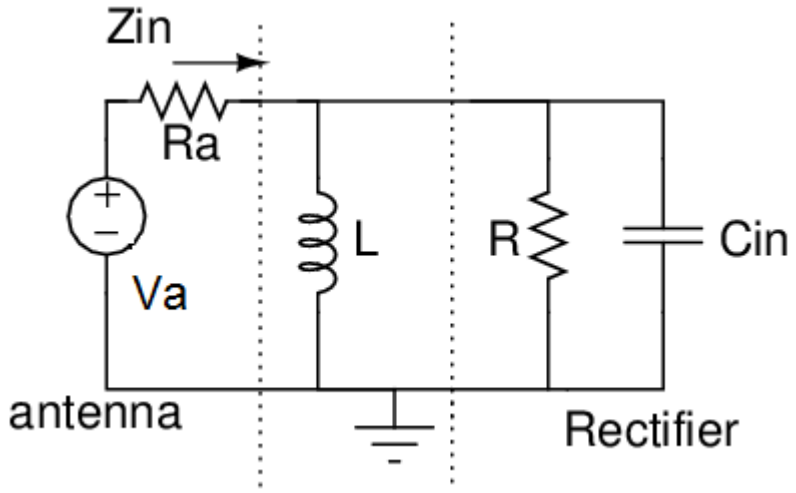
where Γ represents the reflection coefficient due to mismatch between antenna impedance and load circuitry impedance. The Ra represents the radiation resistance of the antenna, Va is antenna open circuit voltage. The antenna is modeled by port with input power range -20dBm to -10dBm and having a constant resistance of 50 for the purpose of simulation.

There are three different types of matching techniques, i.e. transformer matching, Series inductor matching and parallel inductor matching. The parallel inductor matching an off chip an external inductor is placed in parallel with input capacitance of the chip C_{in}. In case of series inductor matching output current is Q times the input current at resonant frequency where imaginary part of inductor cancels with the capacitance C_{in}. The chip input impedance R and $R_{antenna}$ must be matched by proper design of antenna along with rectifier. In case of parallel inductor matching it provides a good Electro Static Discharge protection. At weak RF input power as current will only be multiplied by factor of Q hence sensitivity of the circuit is unchanged.

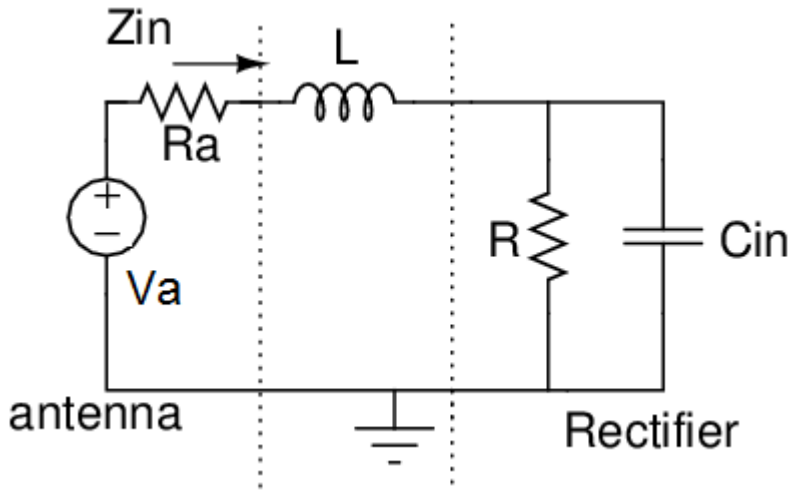
Transformer matching is generally avoided as they are too costly in nature. The series impedance matching networks help in boosting the sensitivity of the circuit as output voltage of the circuit is Q times the input voltage. The sensitivity of RF energy harvesting circuit is the minimum value of input voltage that can be converted to DC value. The series inductor matching the inductor is placed in series with input capacitance of Zin so that imaginary of the impedance cancels off. In case of parallel inductor matching a large value of Ra is required to generate a required input voltage that can be converted into DC output voltage. One problem with this is we require a large value of Ra we require a very large length of antenna at longer wavelength designing a small size antenna with large Ra and longer length is a challenge. The antenna resistance remains in the range of few tens to hundreds of ohm.

In case of rectifiers provides a better power conversion efficiency with increase input voltage amplitude/ power level.

2.3.1 Single Band Matching



(a)



(b)

Figure 2.3 (a) Parallel Inductor matching (b) Series Inductor matching.

The series and parallel inductor matching are low cost but these matching circuit provide a smaller range of frequencies over which required Q is obtained by resonance circuit. As we deviate from the central resonance frequency our efficiency tends to degrade heavily. In case of series and parallel inductor matching the centre of the resonance frequency depends on both value of Cin and inductor L and is given by $\omega_o \approx \sqrt{\frac{1}{LC_{in}}}$.

If we look at the resonant circuit from antenna side the real part of impedance seen consists of parasitic impedance along with a real part of equivalent parallel resistance of rectifier circuit and it is given by

$$Z_{in} = \frac{\omega L}{Q_L} + \frac{R}{1+Q_{tank}^2} \qquad (12)$$

Where R impedance of the rectifier and parasitic resistane of inductor is given by $= \omega L/Q_L$. The $Q_{tank}= \omega C_{in} R$ Tank quality factor. As available off chip inductor comes with high quality factor Q_L=50. At 900MHz the parasitic resistance of inductor with quality factor=50 is equal to 3.4 ohm. The Quality factor of inductor says that how store energy in inductor with minimum losses. Substituting for $\omega = \omega_0 = \sqrt{\frac{1}{LC_{in}}}$ then assuming a higher quality of inductor and as well as of tank circuit

$$Z_{in} = \frac{1}{C_{in}\omega_0}\left(\frac{1}{Q_L} + \frac{1}{Q_{tank}}\right) \quad (13)$$

In case of matching antenna resistance is equal to the input impedance of the rectifier must be equal to the antenna resistance.

$$P_{recieved} = P_{avail}\frac{\frac{R}{1+Q_{tank}^2}}{\frac{R}{(1+Q_{tank}^2)} + \frac{\omega_0 L}{Q_L}} \quad (14)$$

$$P_{recieved} = \frac{P_{avail}}{1+\frac{1+Q_t^2}{Q_L}\frac{\omega_0}{R}} = \frac{P\_avail}{1+\frac{1+Q_t^2}{Q_t Q_L}} \quad (15)$$

Since the rectifier output voltage is given by

$$V_r = \sqrt{2P_{recieved}R} \quad (16)$$

As we have tank quality factor given by $V_r = \sqrt{\frac{2P_{avail}\,R}{1+Q_{tank}/Q_L}} = \sqrt{\frac{2P_{avail}(Q_{tank}Q_L/(Q_{tank}+Q_L))}{\omega_0 C_{in}}}$

From the above equation we arrive at conclusion that

1. The input capacitance value should be as small as possible. It can be observed that by differentiating with respect to term containing Cin i.e. tank quality factor the optimum value should be equal to one. This provides a leverage to either keep Cin smaller or keep R large as far as possible. The Cin cannot be decreased further otherwise pad parasitic as well as ESD protection diode will decide the resonance frequency. The another impact is that the Radiation resistance of the antenna must be equal to the Zin. As Zin inversely proportional to Cin so for a very smaller value of of Cin implies large value of Zin hence a we need to design a antenna with large radiation resistance. This cause is larger size of the antenna.

2. A quality factor of the inductor should be as large as possible

The large value of the Q_L implies that the $P_{recieved}$ is will be equal to $P_{available}$ when Q_L is large as possible compared to the Tank quality factor.

$$P_{recieved} = \frac{P_{avail}}{1 + \frac{1 + Q_t^2}{Q_t Q_L}} \quad (17)$$

2.4 Dual Band Matching Circuit:

We propose a mechanism is for deriving the values of dual band RF Energy harvesting system. In case we actually identify the values for series inductor matches and series capacitor matching for the two bands. The constraints for which are derived described below.

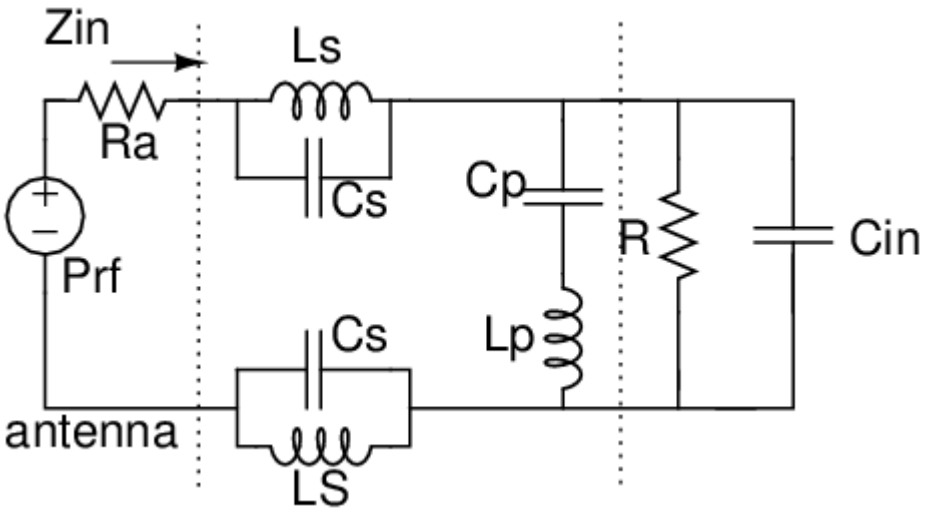
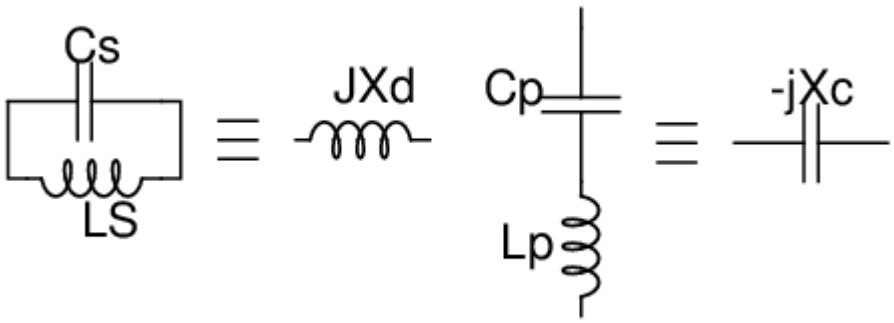


Figure 2.4 Dual Band RF energy Harvesting Circuit



(a) . (b).

Figure 2.5 (a) Series Parallel resonator. (b) Parallel Series resonator.

Here we neglect the impact of parasitic resistances. In case to Series to parallel resonator scheme the

$$\frac{\left(jX_L + \frac{X_L}{Q_L}\right)\left(-jX_C + \frac{X_c}{Q_c}\right)}{jX_L + \frac{X_L}{Q_L} - jX_C + \frac{X_C}{Q_c}} = -jX_{cd} \tag{18}$$

$$X_{cd}(X_L - X_c) - jX_{cd}\left(\frac{X_L}{Q_L} + \frac{X_c}{Q_c}\right) = X_L X_c\left(1 + \frac{1}{Q_C Q_L}\right) + j\left(\frac{1}{Q_c} - \frac{1}{Q_L}\right)X_L X_c \tag{19}$$

$$X_L X_c\left(1 + \frac{1}{Q_C Q_L}\right) = X_{cd}(X_L - X_c) \tag{20}$$

$$\left(\frac{1}{Q_C} - \frac{1}{Q_L}\right)X_L X_c = -jX_{cd}\left(\frac{X_L}{Q_L} + \frac{X_c}{Q_c}\right) \tag{21}$$

Solving for the frequency ω_1,

$$\frac{L_p}{C_p}\left(1 + \frac{1}{Q_L Q_c}\right) = \frac{1}{\omega_1 \mathrm{C_{d1}}}\left(\frac{\omega_1^2 L_p C_p - 1}{\omega_1 \mathrm{C_p}}\right) \tag{22}$$

$$\mathrm{C_{d1}}\omega_1^2 \mathrm{L_p}\left(1 + \frac{1}{Q_L Q_c}\right) = \left(\omega_1^2 L_P C_p - 1\right) \tag{23}$$

Similarly we can solve for ω_2

$$\omega_2^2 \mathrm{C_{d2}} \mathrm{L_p}\left(1 + \tfrac{1}{Q_L Q_C}\right) = \omega_2^2 \mathrm{L_P C_p} - 1 \tag{24}$$

Equating the equations we obtain

$$\omega_1^2 \mathrm{C_{d1}}\left(1 + \tfrac{1}{Q_L Q_c}\right) - \omega_1^2 \mathrm{C_{p=}}\ \omega_2^2 \mathrm{C_{d2}}\left(1 + \tfrac{1}{Q_L Q_c}\right) - \omega_2^2 \mathrm{C_p} \tag{25}$$

$$C_p(\omega_2^2 - \omega_1^2) = (\omega_2^2 C_{d2} - \omega_1^2 \mathrm{C_{d1}})(1 + \tfrac{1}{Q_L Q_c})$$

Solving for C_p

$$C_p = \frac{(\omega_2^2 C_{d2} - \omega_1^2 C_{d1})(1 + \frac{1}{Q_L Q_c})}{\omega_2^2 - \omega_1^2} \tag{26}$$

From imaginary parts

$$(\tfrac{1}{Q_c} - \tfrac{1}{Q_L})X_L X_c = -X\_cd(\tfrac{X_L}{Q_L} + \tfrac{X_c}{Q_c}) \tag{27}$$

At ω_1

$$\left(\frac{1}{Q_c}-\frac{1}{Q_L}\right)\frac{L_p}{C_p}=\frac{-1}{\omega_1 C_{d1}}\left(\frac{\omega_1 L_p}{Q_L}+\frac{1}{\omega_1 C_p Q_c}\right) \quad (28)$$

At ω_2

$$\left(\frac{1}{Q_c}-\frac{1}{Q_L}\right)\frac{L_p}{C_p}=\frac{-1}{\omega_2 C_{d2}}\left(\frac{\omega_2 L_p}{Q_L}+\frac{1}{\omega_2 C_p Q_c}\right) \quad (29)$$

Equating both equations we can find value of

$$L_p=\frac{Q_L(\omega_1 C_{d1}-\omega_2 C_{d2})}{\omega_1\omega_2 C_p Q_c(\omega_1 C_{d2}-\omega_2 C_{d1})} \quad (30)$$

For the series branch we can write the equation

$$jX_{Ls}+\frac{X_{LS}}{Q_L}-jX_{cs}+\frac{X_{cs}}{Q_c}=jX_{Ld}$$

Equating imaginary terms

$$X_{Ls}-X_{cs}=X_{Ld}$$

At ω_1 and ω_2

$$\omega_1 L_S-\frac{1}{\omega_1 C_s}=\omega_1 L_{d1}$$

$$\omega_2 L_S-\frac{1}{\omega_2 C_s}=\omega_2 L_{d2}$$

Equating both the equations we have

$$L_s=\frac{\omega_1^2 C_s L_{d1}+1}{\omega_1^2 C_s}=\frac{\omega_2^2 C_s L_{d2}+1}{\omega_2^2 C_s} \quad (31)$$

Solving the above equations

$$C_s=\frac{\omega_1^2-\omega_2^2}{\omega_1^2\omega_2^2(L_{d1}-L_{d2})} \quad (32)$$

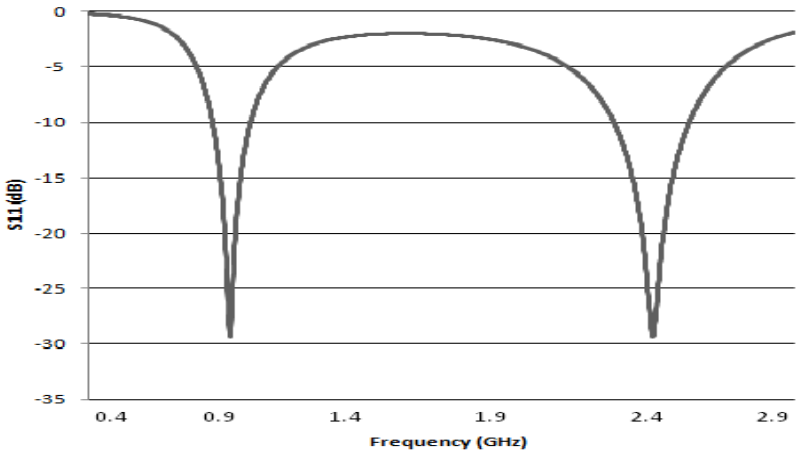


Figure2.6 shows the Dual Band Matching network Reflection coefficient.

Chapter 3:

AC to DC converters

3.1 Introduction

The power decreases drastically as distance between transiting antenna and receiving antenna increases. This provides limitation on the power that is available as receiving side of antenna. Hence we require a highly efficient AC- DC converter that can provide a better power conversion at lower input received power. As limited power/voltage is available at the RF energy harvesting circuit we cannot go conventional rectifier circuits.

In this chapter we review the already exiting charge pumps and accordingly chose one of the efficient rectifiers to design a energy harvesting system. We will also discuss the need for RF limiter and working principle also at the end of the chapter.

3.2 Dickson Charge pump based Rectifiers

Dickson based [18] charge pumps are widely used in many application domains for RF energy harvesting. The original circuit was proposed by Dickson in 1976 that consists of only diodes. In modern day RFID tags the diode are replaced by diode connected MOSFET's whose threshold voltage is |Vth|. Generally Vth of the MOSFET in 0.18um technology is 450mV. If the input voltage is small the overall voltage at output obtained by the Dickson charge pump will be small which does not suffice the requirements of long range RFID tags.

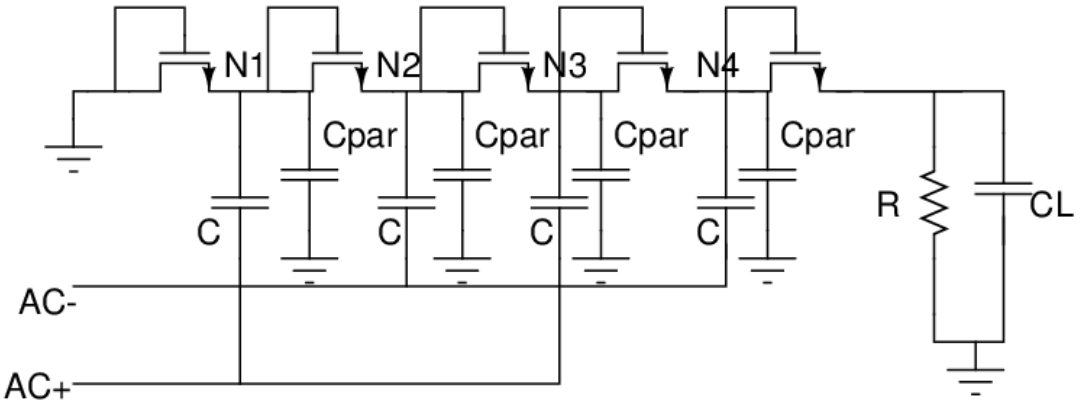


Figure 3.1 Schematic of the Conventional Dickson 4 stage Rectifier circuit.

The performance of the proposed Dickson Charge pump is majorly affected by threshold voltage of the rectifier. Te forward voltage drop across each NMOS is |Vth|. In ideal case the output voltage m stage is M(Vin-|Vth|). However the output voltage is less because the body effect causes the threshold voltage to increase as we move towards load.

Assume AC+ and AC- voltage magnitude is Vin then voltage fluctuation at node N1 is given by the voltage due to parasitic.

$$\Delta V_{N1} = Vin\left(\frac{C}{C + C_{par}}\right) - \frac{I_0}{f(C + C_s)} \qquad (33)$$

Where I_0 is the output current, V_{in} is the input voltage, f is the frequency of operation.

When Vin+(AC+) is high the voltage pumped to next node is $V_{in}+\Delta V_{N1.}$ Once the voltage is pushed to next node the corresponding NMOS pumping charge to next node turns off.

The necessary condition for the charge to be pushed to next node is given by

$$\Delta V > V_{tn}$$

where V_{tn} is the threshold voltage of the NMOS. The voltage gain from node1 to node2 is given by

$$GV = V_2 - V_1 = \Delta V - V_{tn}(V_2) \qquad (34)$$

The $V_{tn}(V_2)$ is the threshold voltage at node 2 modified by body effect of MOST whose gate is connected to node N_2. If the W/L ratio of transistors is kept small then complete charge transfer will not possible within the time period of AC signal hence the gain each stage decreases.

As the voltage of the input AC signal decreases then gain associated with each stage decreases. However to increase the gain Dickson rectifier and eliminate body effect the floating gate MOSFET are used.

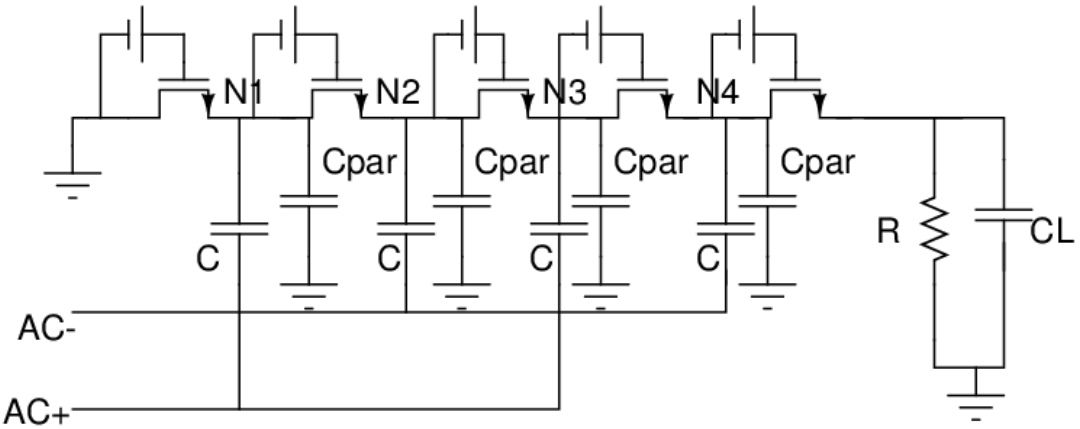


Figure 3.2 Schematic of the Modified 4stage Dickson rectifier with Gate Biasing.

The conventional Dickson based rectifier is modified by applying externally generated gate voltage to compensate threshold voltage of the MOSFET. The compensation can be ideally provided by applying a static bias offset between the gate and drain terminals of the transistors. This arrangement has the same effect of a net reduction of the MOSFET threshold voltage, thus yielding an improvement of the rectifier performance.

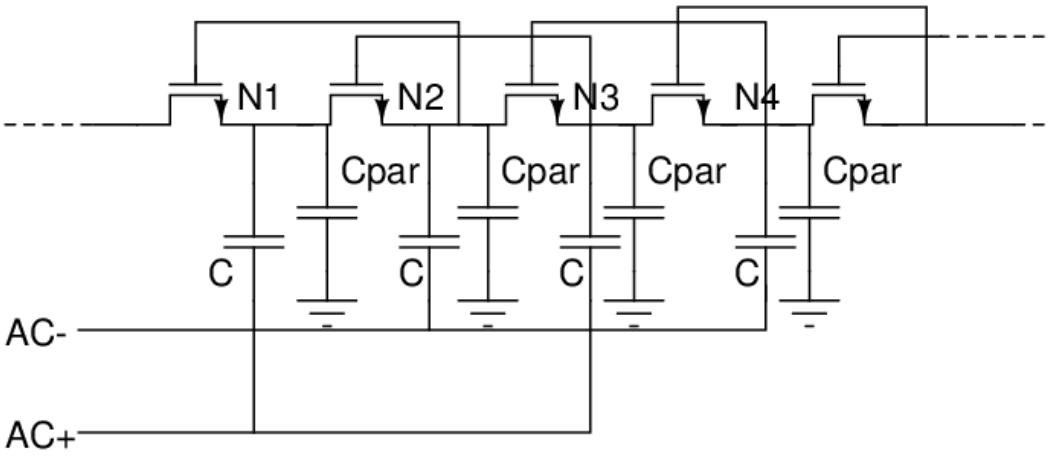


Figure3.3 Basic Implementation for Self Compensation in case of Dickson Based Rectifier.

The Dickson based rectifier can also provide self compensation by changing the order of compensation[19]. The aim for improving the performance a generalized self-compensation methodology is shown Figure3.3. It consists of extending the length of compensating bridges to increase the gate bias offset. The "order" of compensation (i.e., the length of the gate connections) is chosen based on the process threshold voltage and required output voltage. The only even-order compensations are possible because of differential input feed. The maximum efficiency recorded in this case is 21%.

The full wave rectifiers are implemented using odd-order compensations for symmetrical topologies only for delivering power to the load during positive as well as negative phases of ac input. The odd-order compensations can be obtained using cross-coupling bridges[20], as
shown in Fig. 3.3. Here, as charge moves from one coupling capacitor to the next in terms of packets only one NMOS transistor is encountered instead of two complementary transistors. This causes reduction in series losses and improves the overall efficiency of system.

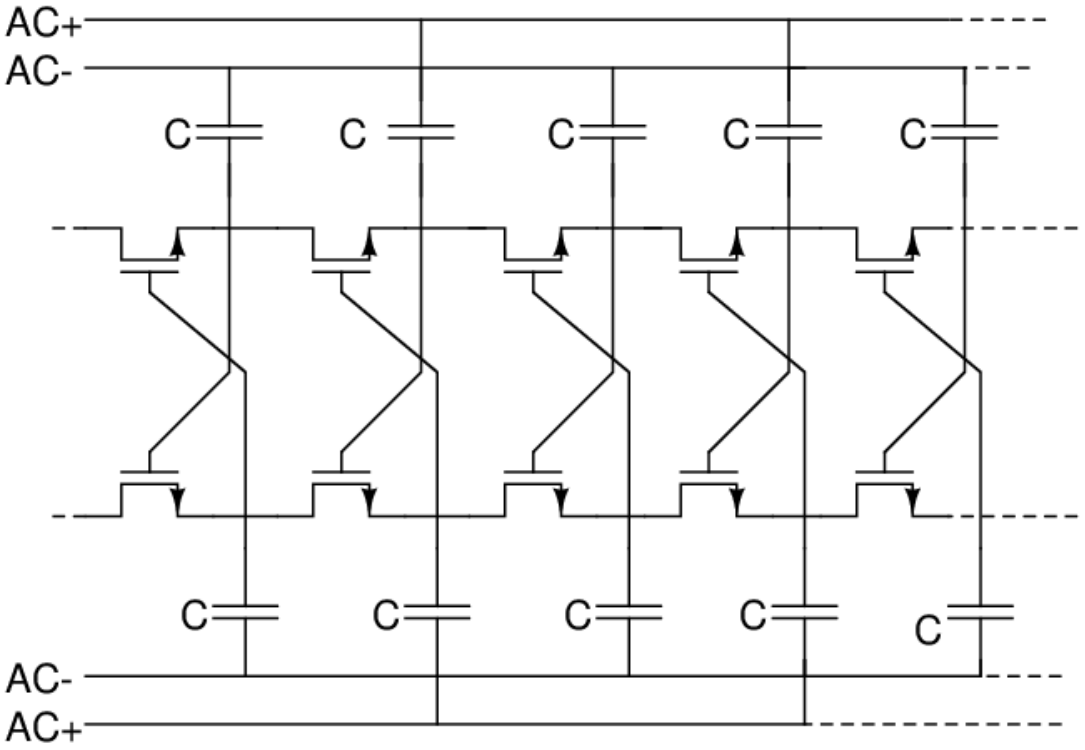


Figure.3.3 Full rectifier with self compensation

3.3 Differential Rectifiers with Dynamic Vth cancellation

There are different types of threshold volatge Static Vth cancellation(SVC) technique[8] and Dynamic Vth Cancellation(DVC) technique are used to other types of design rectifier. Static Vth cancellation is used Koji Kotani et. al [13] achieves an efficiency of 23.2%. A. Sharif Bakhtiar et. al [16] have designed a dynamic Vth cancellation techniques using an auxiliary driver circuit. This circuit gives a better efficiency for less than -20dBm input power, but with increase in input voltage magnitude the efficiency degrades drastically due to reverse current losses.

The better dynamic Vth cancellation technique was pro-posed by the Atsushi Sasaki et. al which provide good efficiency and better sensitivity. The rectifier circuit is shown in Fig.3.5. The advantage of differential drive rectifier circuit is, the MOS transistor will be either in complete turn on or off condition for most of cycle due to the differential dual RF

feed from antenna.

In case static V_{th} cancellation the rectifier Power conversion efficiency (PCE) can be increased by compensating V_{th} constantly regardless of RF voltage applied to the gate of the MOSFET's. Although here the effective ON resistance of MOST's decreases but in case when MOST need to completely turned off there will be comparative large leakage current leading to higher losses and reducing the PCE.

In case of the of the differential drive rectifier it is active V_{th} cancellation technique where in forward bias condition R_{on} will be minimized and in a reverse bias condition the R_{off} increases drastically due cross coupled differential input feed.

The PCE of the rectifier is given by ratio of power delivered to the load P_{out} to input power P

$$PCE = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out}+P_{loss}} \quad (35)$$

Here the P_{loss} is loss due diode connected MOST hence overall loss is equal to the $N.P_{diode}$

$$P_{diode} = P_{FWD} + P_{REV} \quad (36)$$

Where P_{FWD} and P_{REV} are loss in forward bias and reverse bias condition which are recognized by turn on voltage and reverse leakage current of diode respectively. Generally reverse leakage current will be less and reverse bias losses are minimal compared to forward bias.

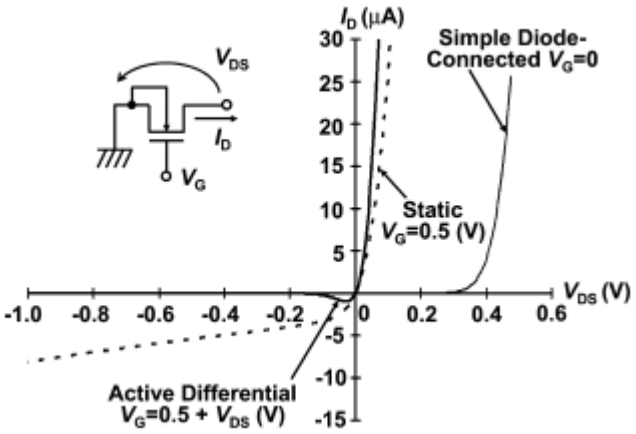


Figure 3.4 V I characteristics of diode connected n channel MOSFET.

In case of differential drive rectifier CMOS rectifier configuration consists of the cross coupled differential CMOS configuration with a bridge structure. In differential schemes the gate of the transistors are actively biased by a differential mode signal.

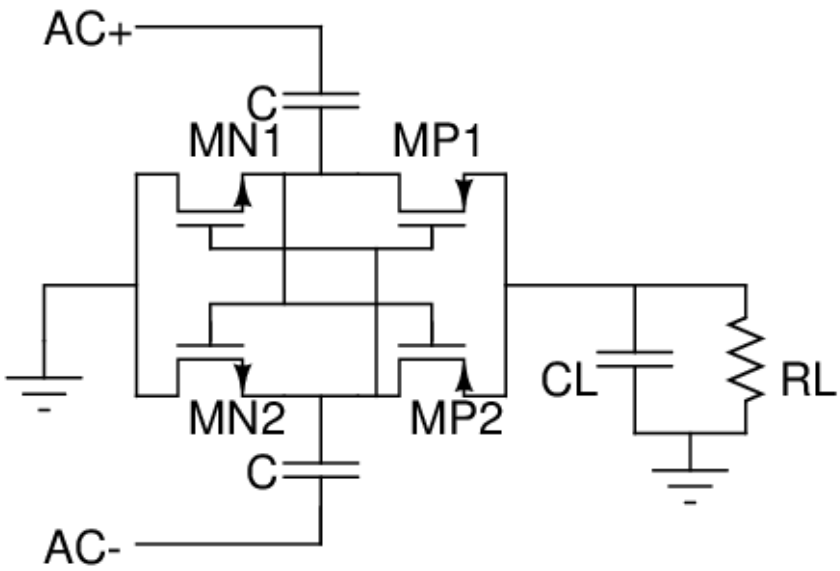


Figure 3.5 The 4 T Differential drive rectifier

The operation mechanism of the rectifier circuit is described as follows. Let us assume sufficient amount of input power is applied, the rectifier starts to rectify and reaches to steady state within short time. The three components, namely, forward-transferred charges, reverse-transferred charges and charges flowing to an output load are balanced for understanding the operation of the rectifier circuit. At first forward-transferred charges are larger than the sum of reverse transferred and charge transferred to load, the output DC voltage increase towards their steady-state value.

$$Q_{FMN1} - Q_{RMN1} = Q_{FMP1} - Q_{RMP1} = Q_1$$
$$Q_{FMN2} - Q_{RMN2} = Q_{FMP2} - Q_{RMP2} = Q_2$$
$$Q_1 + Q_2 = \frac{V_{DC}T}{R_L}$$

Q_{FMN1}, Q_{FMP1}, Q_{FMN2}, Q_{FMP2} are the amount of charge that is transferred in forward direction i.e. MN1, MP1, MN2, MP2 respectively. Q_{RMN1}, Q_{RMP1}, Q_{RMN2}, Q_{RMP2} are the amount of charge that is transferred in reverse direction MN1, MP1, MN2, MP2 respectively.

T is the time period of the RF signal, RL is load impedance. And Q1 Q2 is net amount of charge transferred in forward direction in single period T through upper path composed of MN1 MP1 and MN2 MP2 respectively

The efficiency of the four-transistor cell first decreases by decreasing the input amplitude (VRF), however it peaks at V_{RFopt} and then drops. This is happens because as input amplitude becomes small, the transistors not completely turned on resulting in a large drop between drain-source terminals of conducting transistors. The minimum voltage drop on conducting transistors (V_{DSmin}) can be reduced by increasing gate-source voltage (V_{GS}) of those transistors.

If input amplitude is large enough, transistors conduct a reverse current from the decoupling capacitor back to nodes for a small instance of time just prior and after PMOS transistors turn on. This effect is seen in Figure

3.6. The rectifier efficiency drops because of the reverse current flow. The condition for reverse current flow is given by

$$V_{RF} > |V_{thNMOS/PMOS}| + 2|V_{DSPMOS/NMOS}|min$$

3.3.1 PCE Dependence on Output Load and Transistor Sizing

When output load resistance RL increases the PCE curve shifts to smaller input region **[].** The value of peak PCE increases slightly with increase in $R_{L.}$ The PCE depends on transistor sizes, the gate length of NMOS transistors fixed at 0.18µm. The power conversion does vary with ratio of width of NMOS and PMOS transistors. And it reaches optimum efficiency for width of NMOS equal to 3.6µm and PMOS equal to 18 µm. If they are too small, the voltage drop on them becomes too large and if they are too wide both the parasitic capacitance on the input RF nodes and reverse current leakage increase. In either case the efficiency degrades.

3.3.2 Cascading of Differential Drive Rectifier

The 4T Differential Drive rectifier stages can be cascaded as shown in Fig.8 to get higher output voltage. The output efficiency decreases as the number of stages increases. The
number of stages defines the minimum input power that is required to generate a desired output voltage. The simulation are carried out by cascading 3 stage and 4 stage rectifier
circuit.

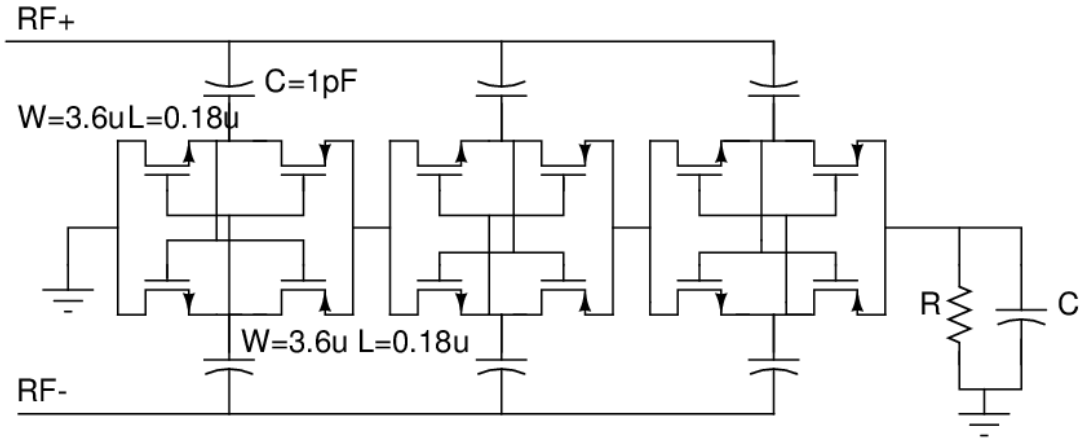


Figure 3.6 Cascaded stages of the 4T Differential Drive rectifier.

The comparison of 3 stage and 4 stage rectifier circuit shown in Fig.9 and Fig.10 respectively for given input voltage with a variable load condition. We were able to achieve a output voltage higher than 1V for load >= 10K Ohm in both cases. So we fixed number of stages cascaded to 3.

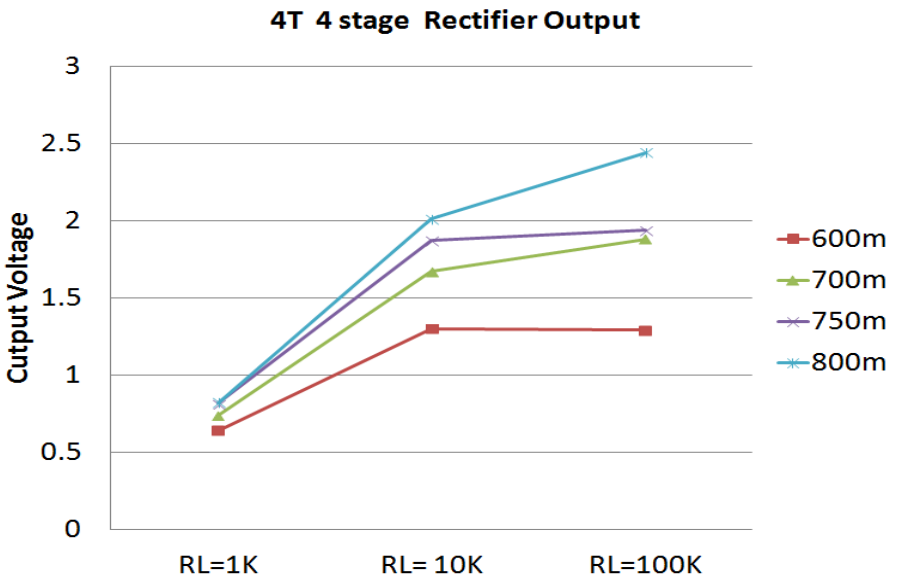


Figure 3.7 Voltage gain of the 4Stage Rectifier circuit

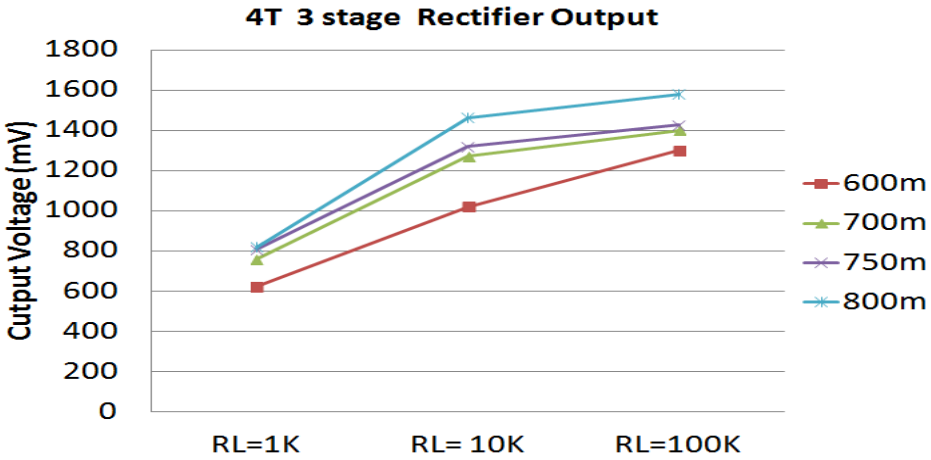


Figure 3.8 Voltage gain of the 3Stage 4T Rectifier circuit

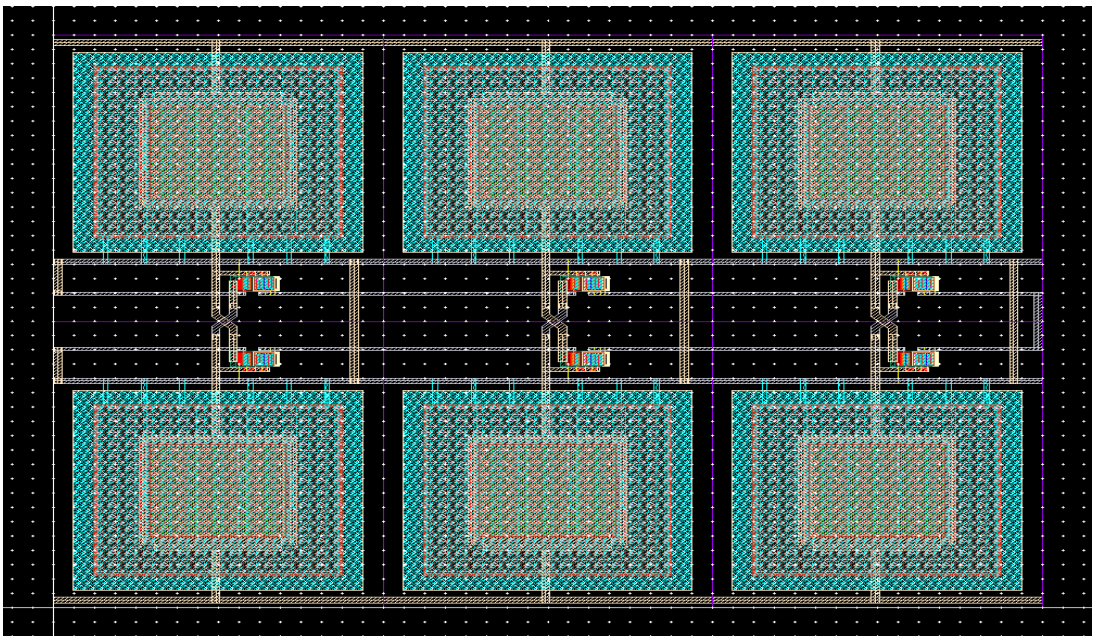


Figure 3.9 Layout of the 3 stage 4T Differential Rectifier stage

The simulation results of Layout of the 3 stage 4T Differential Rectifier stage are shown in the figure 3.10.

We will discuss briefly the operation of modified differential drive rectifier with auxiliary differential driver for each stage.

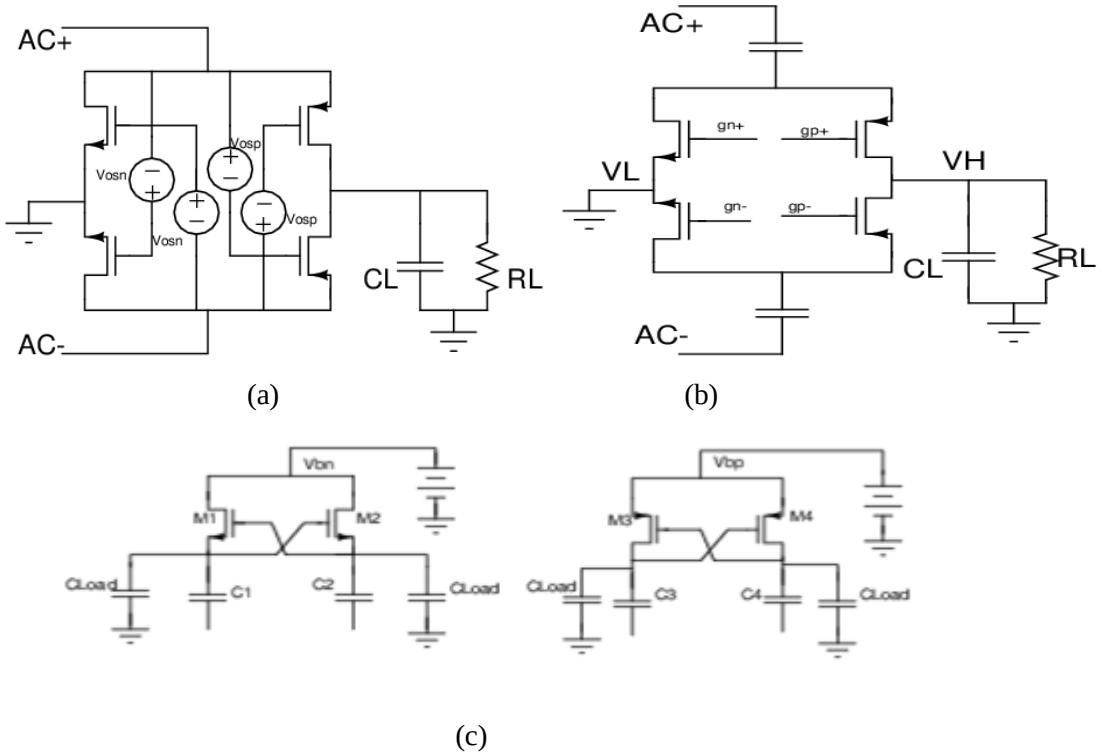


Figure 3.10 (a) Concept of Rectifier with Driver Circuit (b) Bias Generation circuit

The concept of the behind a differential driver rectifier circuit is applying an extra bias voltage to gate terminal so that of the of the transistor is reduced by$V_{b.}$. The V_{osn}, V_{osp} are the bias voltages applied to gate of NMOS and PMOS respectively which are dependent on power input and applied load condition. It utilizes two driver stages for each rectifier stages that drives each NMOS and PMOS stages. The problem with such circuit is the rectifier efficiency is better for input power lesser than -20dBm as we are interested in power levels between -10dBm and -20dBm we did not use it.

3.4 RF Limiter

The input voltage to antenna varies between 300mV's to 20V [1] depending on how close RF Energy harvesting system to reader. So as to avoid the breakdown of the transistor at

higher input voltages we need to limit the RF input feed to rectifier circuit (in our case it is 1.8V). The limiter converges to certain value once variations are limited. The schematic of RF Limiter circuit is shown in the Fig. 3.11.

It includes a single stage voltage multiplier circuit consisting of M1 M2 C1 C2 followed by a RC low pass filter network to eliminate fluctuations in voltage. Any higher fluctuation in the input voltage greater than threshold voltage of the transistors is clamped to the capacitors C1 C2. The voltage across C2 is refined by 2 stage RC low pass filter to remove fluctuations. The Voltage across C4 is less than the set value it turns off cascoded NMOS transistors M3 and M4 preventing any loading to rectifier circuit.

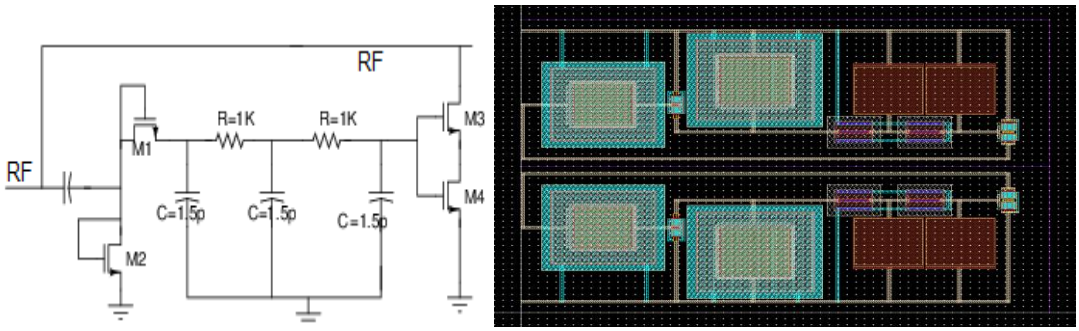


Figure 3.11(a) Schematic Diagram of RF limiter circuit, (b) Layout RF Limiter

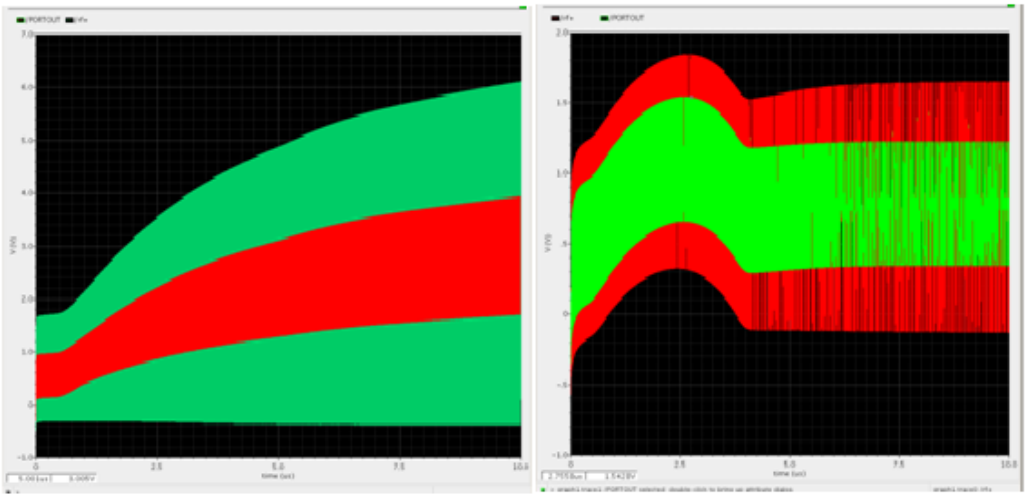


Figure 3.12 Output plot showing comparison between of RF feed with and without RF limiter at 5dBm input power

Chapter 4:

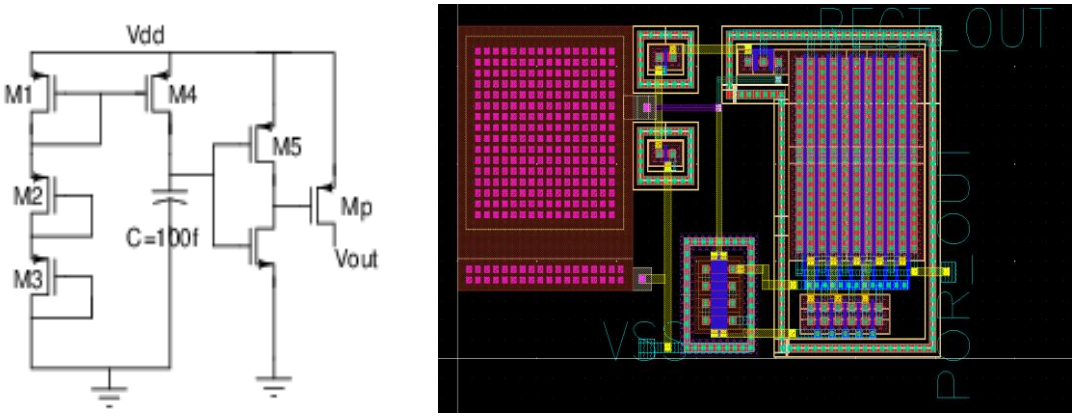
Power Converter Circuit

4.1 Introduction

The power converter circuit is designed to power a load with constant rectifier load circuit it consists mainly of Power On Reset circuit followed by Band gap reference followed by the Differential amplifier with diode connected negative feed back circuit. The requirement of power Converter circuit is suitably power the load consuming lesser power as far as possible.

4.2 Power On Reset Circuit

The POR circuit is used to charge intermediate off chip storage super capacitor (1.2nF). This is done to isolate capacitor from BGR, LDO and load until output voltage of the capacitor reaches to near 1V. The super capacitor limits sudden voltage drop during the start up phase. The POR [17] circuit is designed for near 1V voltage and inverter threshold voltage has been set at 0.7V. The power consumed by POR circuit is at 1V and 2V input voltage.



(a) (b)

Figure 4.1(a) shows the schematic as Power On Reset (POR) circuit (b) Layout of the POR

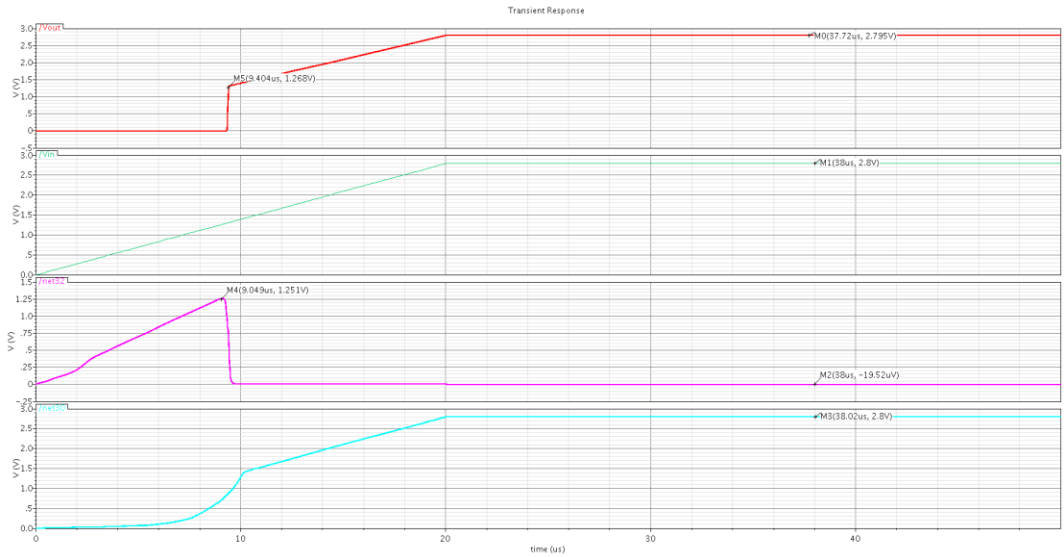


Figure 4.2 shows the transient simulation of the POR circuit that was designed.

The dimensions of the transistors M1 M2 M3 M4 M5 and M6 are

MOSFET	M1	M2	M3	M4	M5	M6	Mp
W/L	240n/280n	400n/180n	400n/180n	240n/280n	4u/180n	240n/4u	100u/180n

Table 4.1 Size of MOS FETs used in POR

4.3 Band Gap Reference circuit:

The Sub-threshold BGR [17] circuit consumes 30.7 ηW to 80.5 ηW at 1V and 2V input voltage respectively. The BGR is used to provide constant reference voltage of 500 mV and bias voltage of 260 mV to the LDO. It consists of bias circuit with cascoded current mirror circuits. The current I_C is controlled by negative feedback from the output which drives transistor (MF) in saturation region.

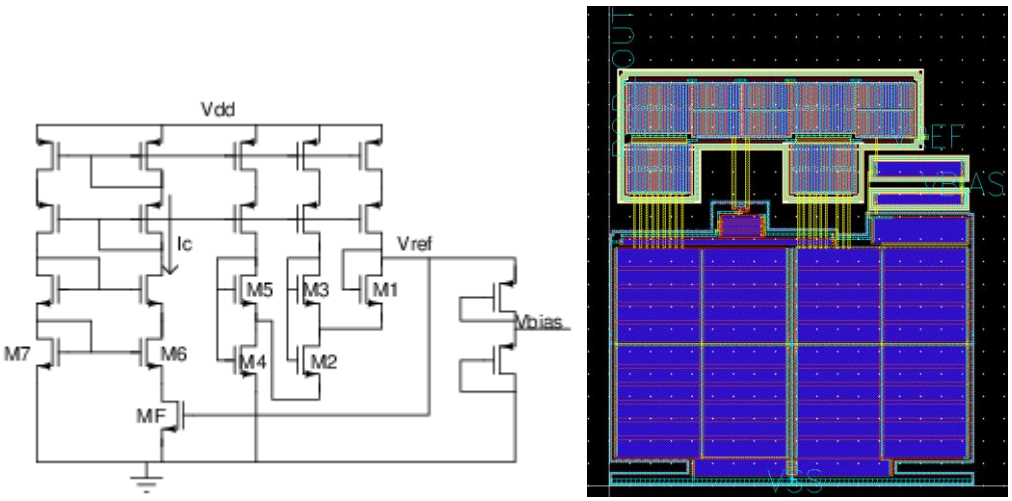


Figure 4.3(a) Schematic of Band Gap Reference (BGR) circuit (b) Layout of the BGR

For $V_{ds} > 4\ V_T$ the current flowing through the MOS FET is given by eqn. (37)

$$I = KI_0\, e^{(V_{gs}-V_{th})/V_T\eta} \qquad (37)$$

where η of the transistor is given by the ratio of the oxide capacitance to the sum of oxide and the depletion capacitance, $I_0 = \mu C_{ox} V_T^2$ and K=W/L

$$V_{gs} = V_{th} + \eta V_T \ln\left(\frac{I}{KI_0}\right) \qquad (38)$$

The current I_C is given by equation considering M6, M7 are similar transistors and are operating in sub-threshold region. The V_{gs} and current I_C is given by equation (10) and (11) below

$$V_{gs7} = V_{gs6} + I_C R_{MF} \qquad (39)$$

$$I_C = \eta V_T \ln\left(K_6 / K_7\right) R_{MF} \qquad (40)$$

where R_{MF} is given by $R_{MF} = \frac{1}{\mu C_{ox} K_{MF}(V_{gs}-V_{th})}$.

The reference voltage temperature compensation is provided by V_{th} and V_T which have the opposite temperature coefficient given by equation.

$$V_{ref} = V_{gs3} - V_{gs2} + V_{gs5} - V_{gs4} + V_{gs1} \quad (41)$$

$$V_{ref}=V_{th1}+mV_T \quad (42)$$

where m is constant . Using above equation we can write V_{ref} as

$$V_{ref} = V_{th1} + V_T \ln\left(\frac{6I_C K_2 K_4}{I_0 K_1 K_3 K_5}\right) \quad (43)$$

Adjusting properly aspect ratio of the transistor the temperature dependency can be eliminated.

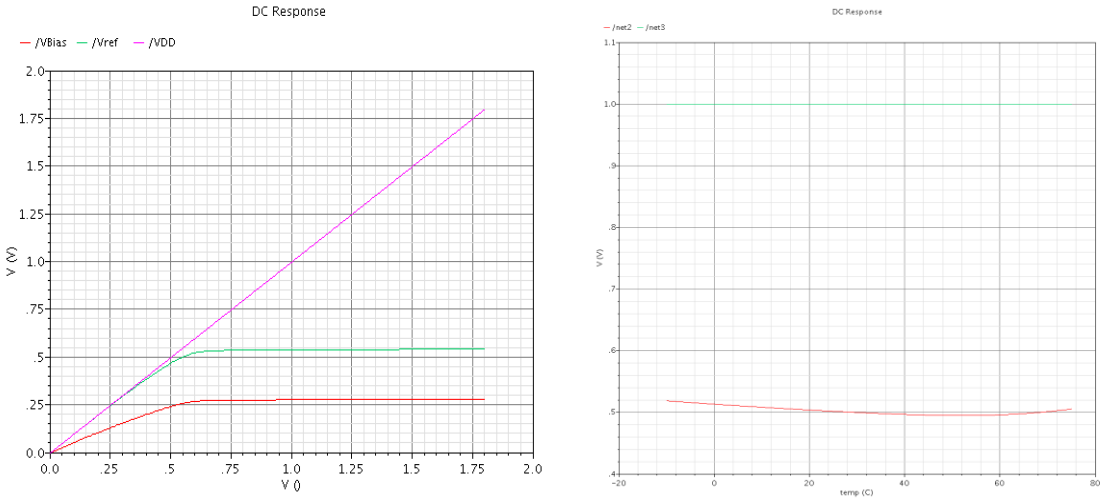


Figure 4. Shows the (a) output voltage of the BGR v/s Input voltage, (b) output voltage with respect to temperature variation

Quiescent Current	30.663 n Amperes (1V) 40.38 n Amperes (2V)
Power consumption	30.7nW to 80.5nW
Input Voltage Range	1V -2V
Settling time	2ms at 1V input for load capacitance of 250f Farads
Output voltage	500mV and 260mV
Temperature coefficient	200uV/K

Table 4.2 Specification of BGR

The W/L ratio of the transistors is mentioned as below.

MOSFET	M1	M2	M3	M4	M5	M6	M7	MF
W/L	4.9u/25u	4.9u/25u	5u/10u	4.9u/25u	5u/25u	600n/9u	600n/9u	300n/50u

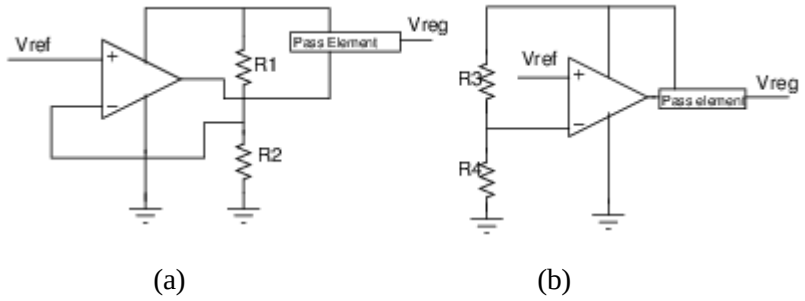
Table 4.3 Size of MOSFET's used in BGR

4.4 Low Drop out regulator:

The Regulators are classified as Switching regulators and linear regulators. The switching regulators are classified by Step up convertor, Step down Convertor. The linear regulator are classified further Series and Shunt regulators. The switching regulator use Capacitor for smoothing, inductor and MOS FETs as switches

Generally switching regulator (convert power) efficiency is greater than linear regulator (waste power). The constraint for using switching regulator is that because it is applicable only case of where power is available in terms of tens and hundreds of mili watt. This is because requires its own clock circuit. The inductor we need to use becomes very large and difficult to integrate with system.. In case the clock frequency of the circuit can interfere with modulation clock. As result of which it cannot be used for ULP RF energy harvesting applications.

The Series and Shunt linear regulator



(a) (b)

Figure 4.5 Types of the linear regulator (a) Series regulator (b) Shunt regulator

The linear regulator requires an error amplifier connected in negative feedback that calculates error w.r.t reference voltage fed to inverting terminal. The pass element is an PMOST whose input gate voltage is regulated linearly by error amplifier hence called linear regulator. The performance of the linear regulator depends on the sensitivity of the error amplifier so the gain of error amplifier must be large enough to regulate a voltage for minor changes.

In case of the shunt regulator control path is connected in parallel to the load hence called shunt regulator. The shunt regulators have a smaller sensitivity to the variation in supply voltage. The Current across bias path is independent of the load connected to output.

The Series regulator are called low drop out regulators where

$$V_{regulated} = V_{ref}(1 + \frac{R_1}{R_2})$$

The advantages of the LDO are No high frequency current switching's are generated.

Output regulated voltage will always be less than the supply voltage.

The LDO consists of the simple differential amplifier circuit followed by the circuit a voltage divider circuit consisting of the diode connected transistors (MF1 MF2 MF3 MF4), pass transistor (MP) which is driven by the output of the differential amplifier. The Low drop out regulator drives the charging device (capacitor) and loading device (resistor). The LDO circuit is shown in Fig.3.5.

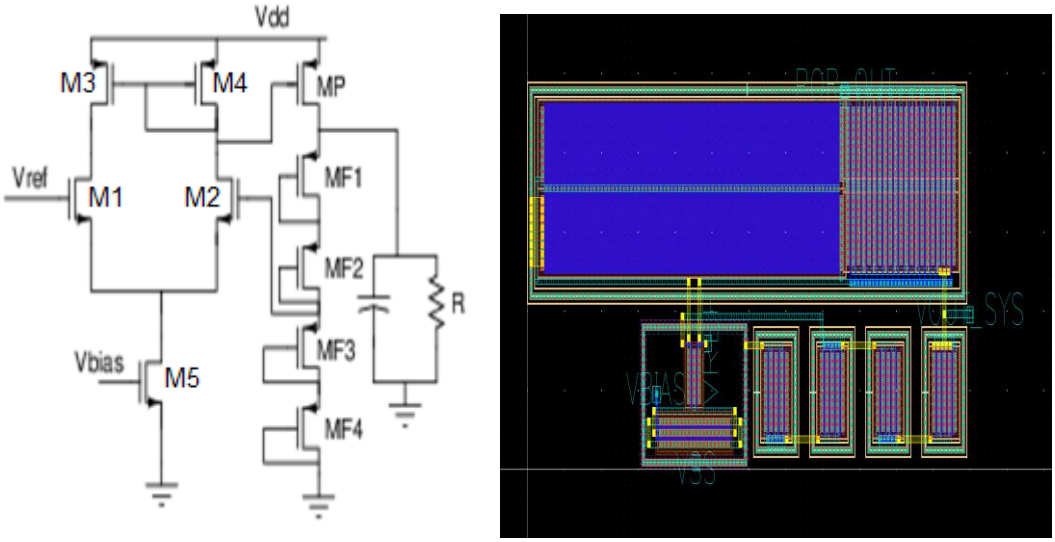


Figure 4.6 Schematic and Layout of the Low Dropout Regulator.

MOSFET	M1	M2	M3	M4	M5	MP	MF
W/L	3.5u/180n	3.5u/180n	4.75u/40u	4.75u/40u	19.3u/180n	100u/180n	240n/20u

Table 4.4 Sizes of MOSFET's used in LDO

Gain Margin dB	50dB
Phase margin	108 degrees
Unity Gain Bandwidth	457.09 KHz
Quiescent Current	453.663nAmperes (1V) 923.38nAmperes (3V)
Input Voltage Range	1V -3V
Designed gain in dB	43.087 dB

Table 3.5 Specification of Error Amplifier

Chapter 5:

Simulation results and Comparison with Existing system

5.1 Comparison with Existing Literature: The Keyrouz et al[5] proposed a multi band energy harvesting scheme at -15 dBm input power having an system efficiency of 45 % at 900 MHz, 46 % at 1800 MHz and 25% at 2.45 GHz. The overall system includes multiple sub systems powered by different antennas with individual off chip matching network, rectifier, power management circuit leading to large aspect ratio of chip. Bo Li et al [6] group have proposed the another scheme for dual band energy harvesting at -19.3dBm input power level with efficiency for 12 % and 11 % at 900MHz and 1800MHz. Similar to Keyrouz et al[5]they use separate chain of matching and rectifier circuits to charge the battery.

The Phirun Kim et al [7] proposed dual band RF energy harvesting scheme with an efficiency of 73.76 % and 63.06 % at 881MHz and 2.4GHz. However above scheme is sensitive at very high input power level of 160mW (22dBm) which does not suffice requirement for the wearable devices that are employed for 10m and above communication range. The Phongcharoenpanich et al [8] proposed a dual band antennadesign for UHF RFID bandwidth 911-925.6 MHz, 2.32GHz-2.52GHz with respective directivity of 8.33dBi and 9-10.5dBi.

Frequency (GHz)	Power Level (dBm)	Topology	Rectifier Efficiency	Reference
f1=0.9 f2=1.9	-19.3	Dual chain	12%@ f1 11%@ f2	[5]
f1=0.88 f2=2.4	22	Dual band Matching	73.7%@f1 69%@f2	[6]
f1=0.9 f2=1.8 f3=2.4	-15	Triple chain	45 %@f1 46%@f2 25%@f3	[7]
f1=0.953 f2=2.4	-14	Proposed Topology	41.87%@f1 46.95%f2	This work

Table 4.1 shows the comparison of full system simulation with other systems with rectifier output.

5.2 Final Chip layout and Simulations Results

The complete Layout of the system is shown in Figure 4.1 below

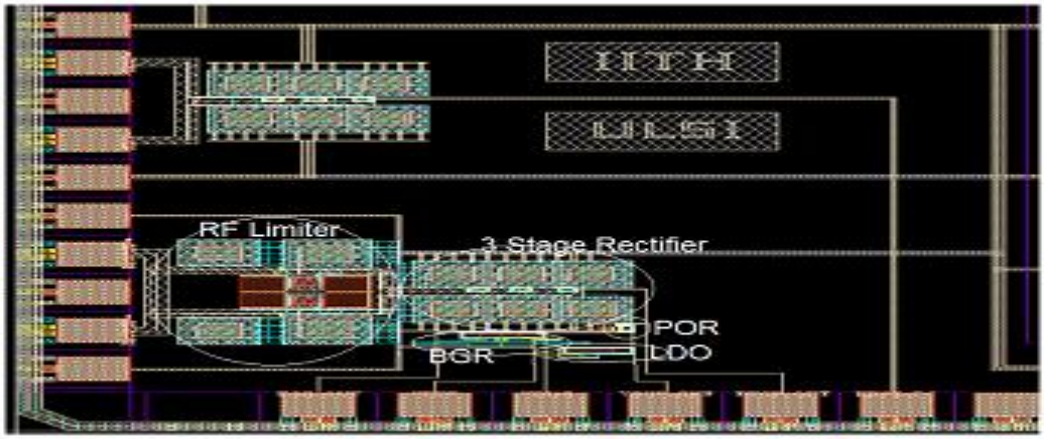


Figure 5.1 Final Chip layout.

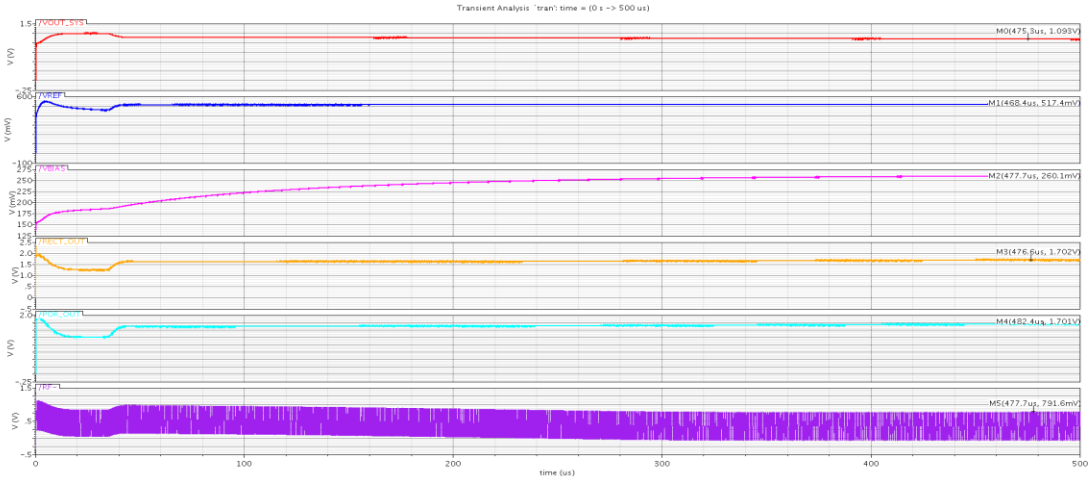


Figure 5.2 Shows the Final chip Layout simulation.

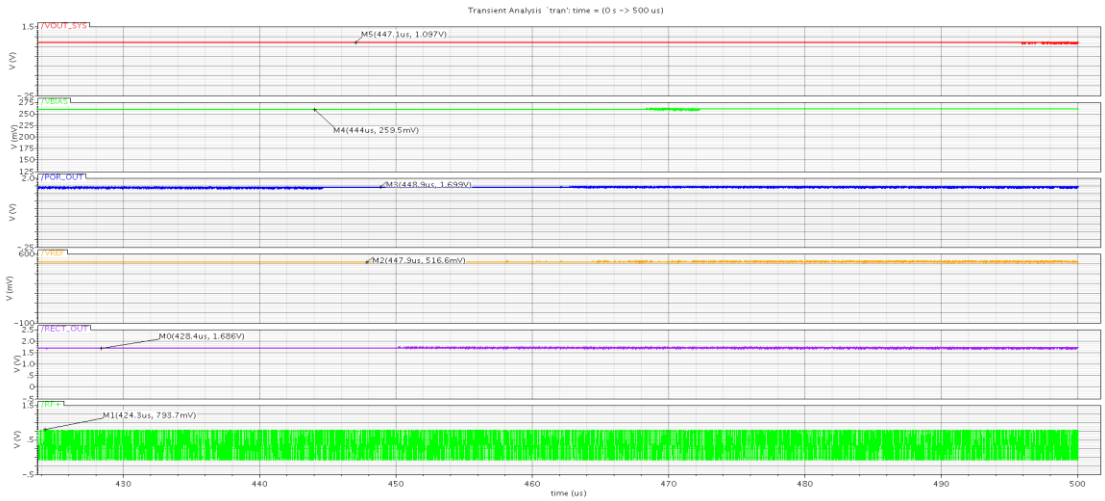


Figure 5.3 Steady state output of full chip simulation.

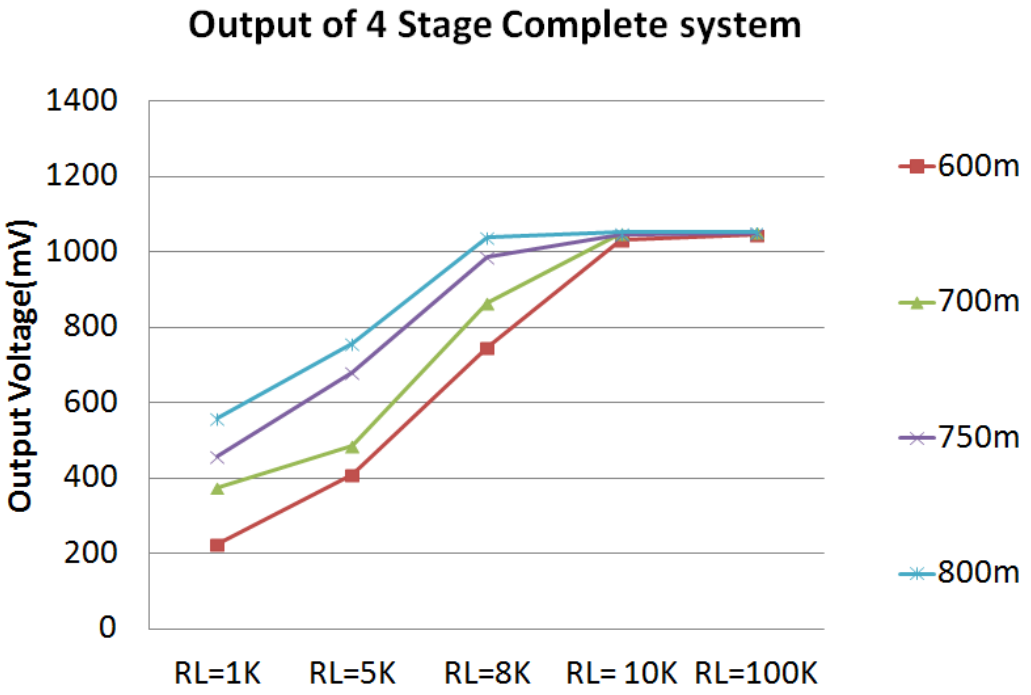


Figure 5.4 Voltage gain of the complete system with 4 cascaded Rectifier Stages.

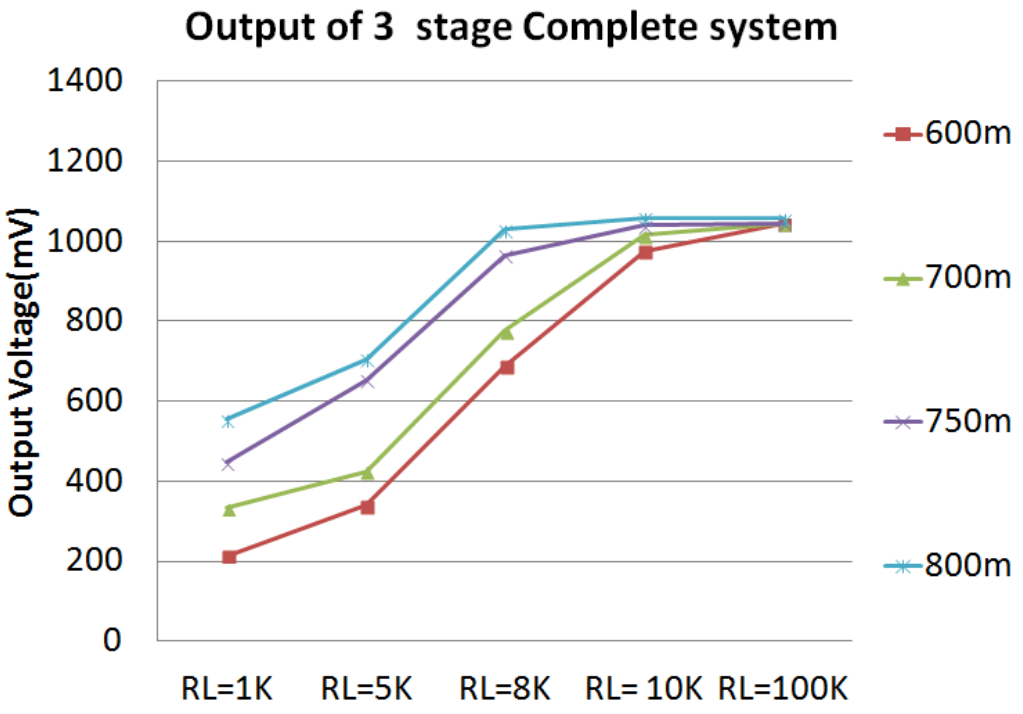


Figure 5. Voltage gain of the complete system with 3 cascaded Rectifier Stages.

Chapter 6:

Future Work: A novel architecture for Constant Voltage charging of a battery

6.1 Introduction: Here we propose the architecture for the constant voltage charging o f the battery. In this architecture we have 2 steps mechanism to charge a battery by charging intermediate super capacitors.

The DC limiter is added at output of the rectifier to precisely limit the maximum voltage that is fed to the next stages. The power on reset circuit has a self generated reference voltage comparator which has cutin voltage of 1.31V and cutoff voltage of 1.2V. This does the same function POR on reset circuit as mentioned in the above chapter 3.

The charge pump used can be a linear charge pump or Fibonacci charge pump. The number of the stages can be fixed by the amount of voltage gain that is needed to provide by the regulator. The

charging of the battery depends on min and maximum voltages that are needed to charge a battery which is decided by cutin voltage of POR and DC limiter output voltage respectively. The low power clock generation circuit is designed that generates a constant output voltage and constant frequency whenever POR is completely turned on otherwise it will decrease the clock frequency when Power On Reset is partially turned on. The free running clock has a frequency of 22 MHz.

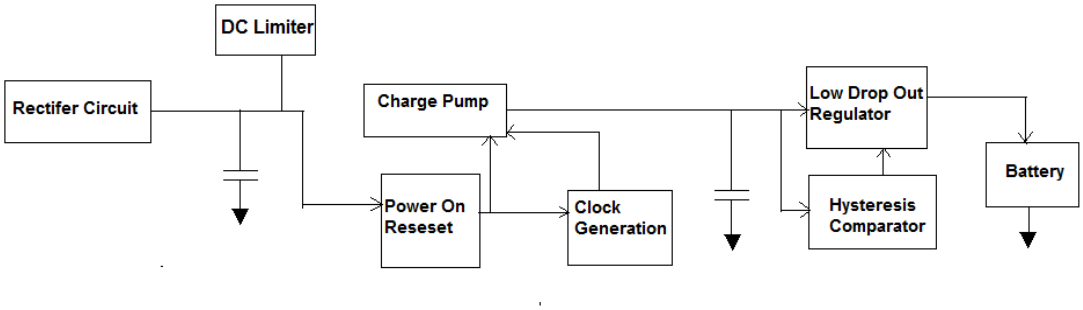


Figure 6.1 shows a novel structure of complete system simulation for constant voltage battery charging.

6.2 Schematic and Simulation results

The figure shows a single stage Charge Pump.

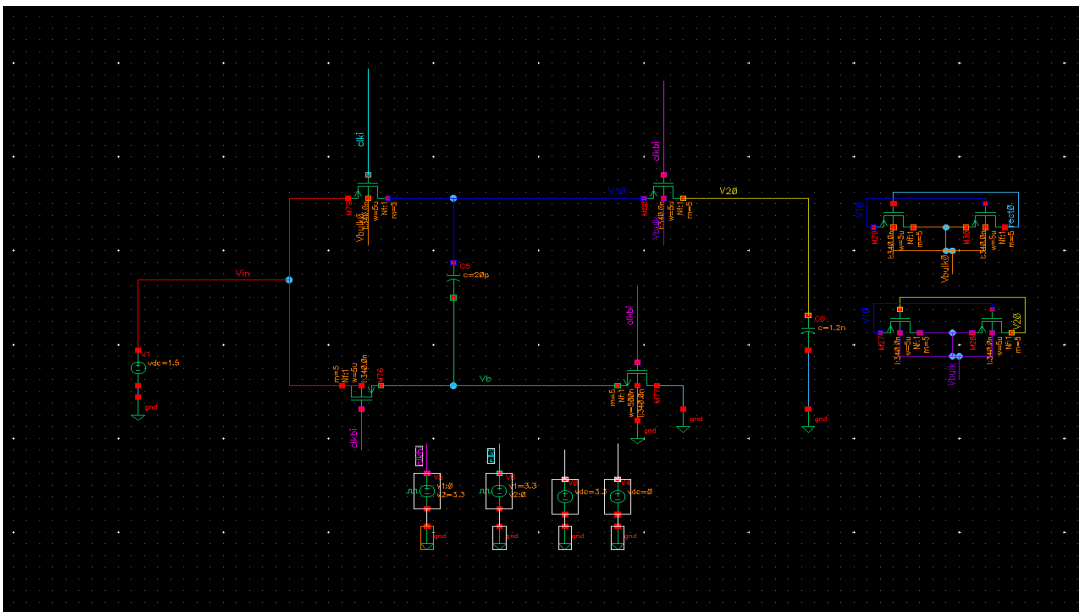


Figure 6.2 shows a single stage charge pump

The output of the charge pump is shown in Figure5.3

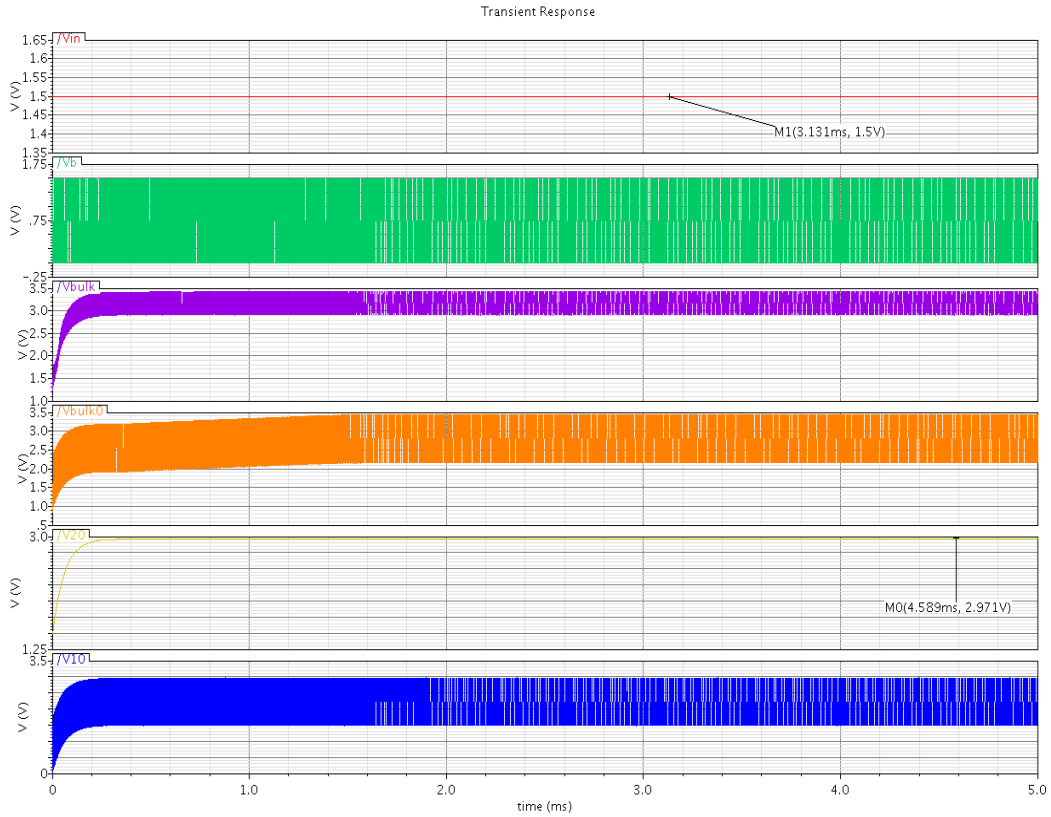


Figure 6.3 Shows output of single stage charge pump

The power on reset circuit is shown in the figure below has cutin and cutoff voltages off 1.31V and 1.9V respectively.

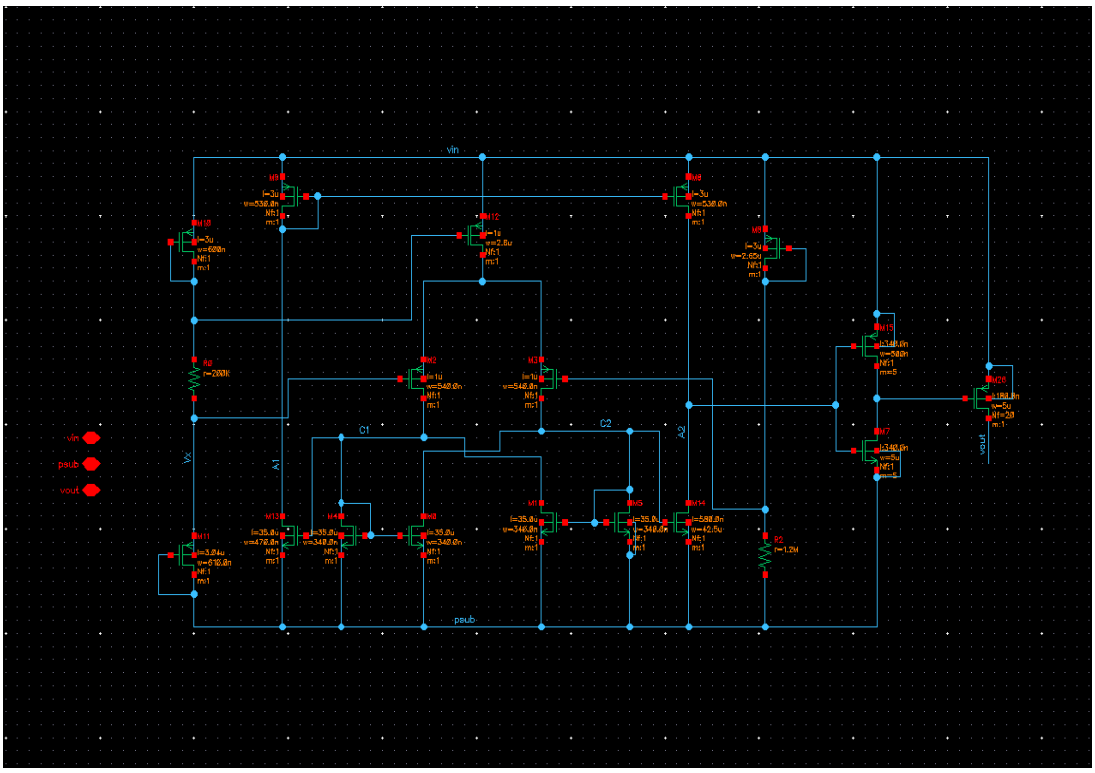


Figure 6.4 shows the Power reset circuit.

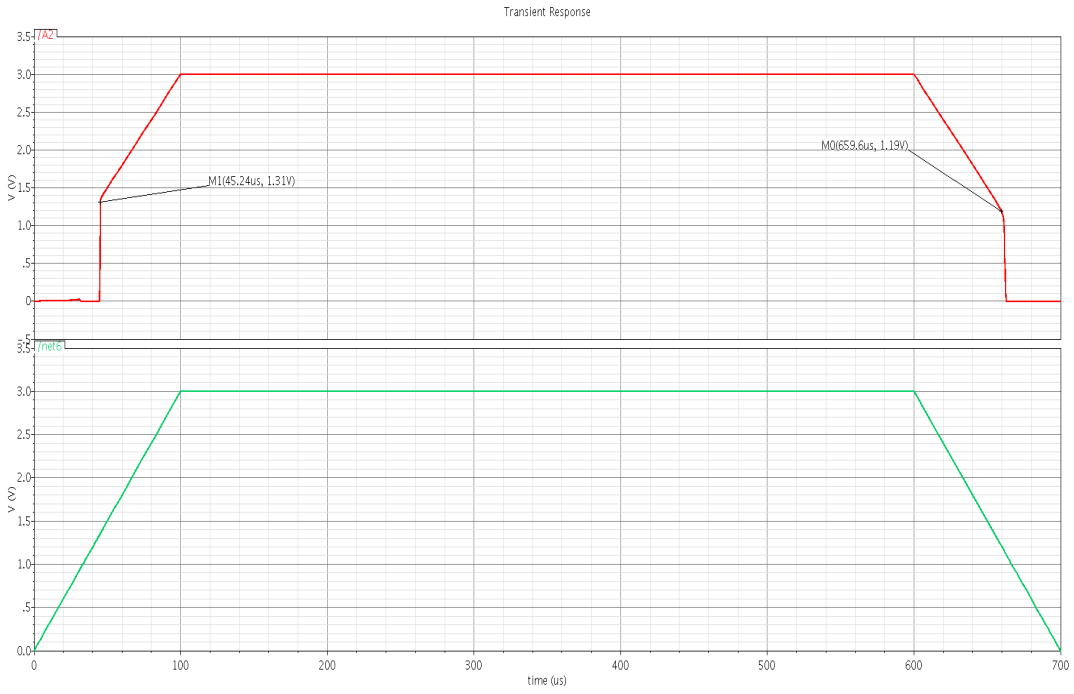


Figure 6.5 Transient simulation of power on Reset circuit.

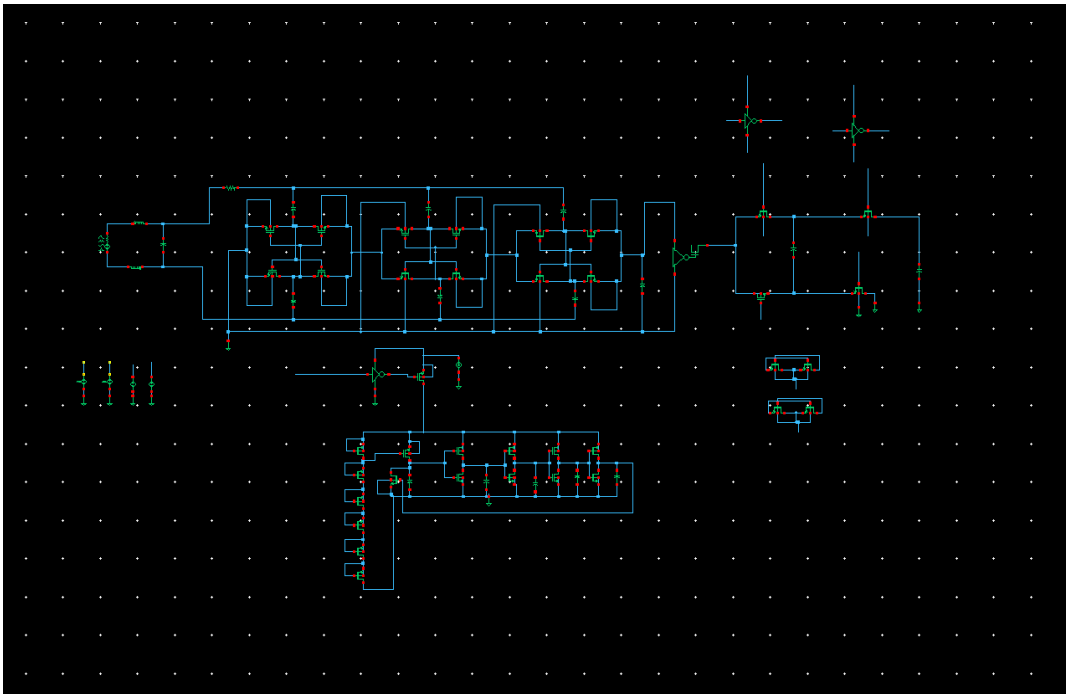


Figure6.6 first phase simulation of the circuit without DC limiter

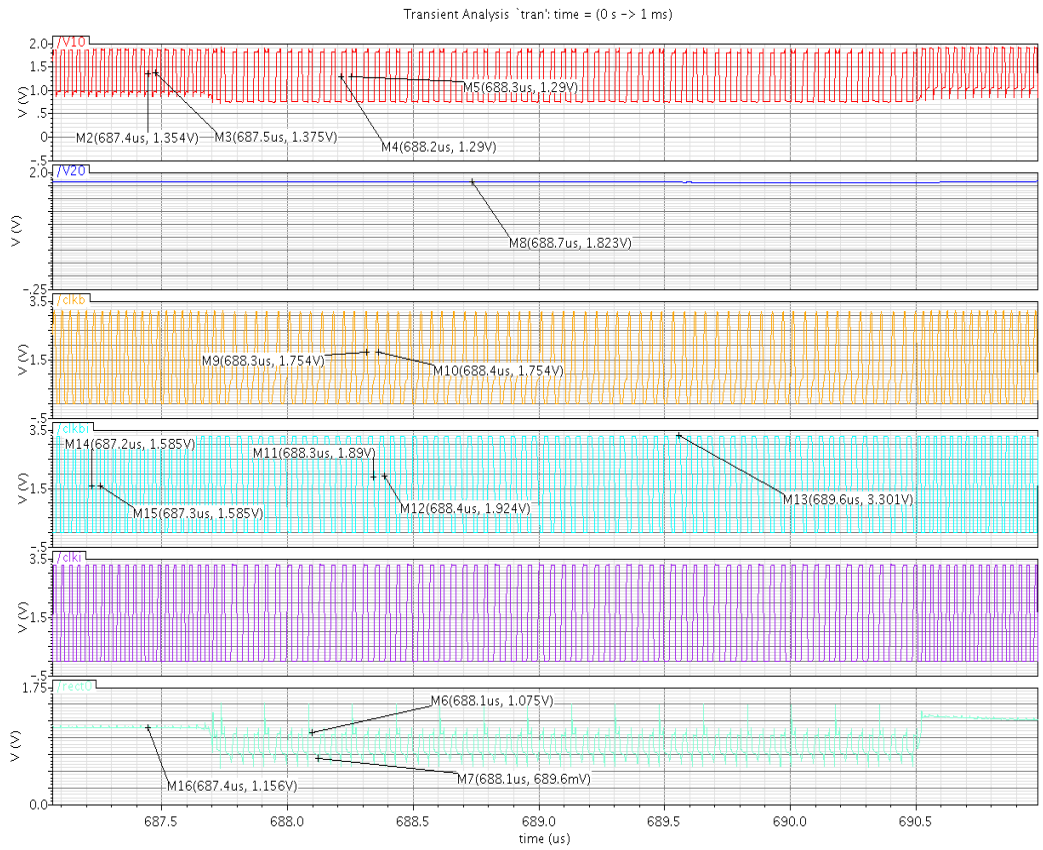


Fig. 6.7 Complete System output with own clock generation having two phases of operation.

The three phases of operation are

- **Complete turn on of Power on Reset block** (Rectifier output voltage is between 1.3V and DC limiter output voltage)

There will be free running clock frequency of 22MHz and the charge packet transfer happening at faster rate leading to faster settling of output.

- **Partial turn on Power on Reset** (Rectifier output voltage is between 1.9V to 1.3V)

Here clock frequency is reduced to 15MHz and 2^{nd} super capacitor is charged at small rate.

- **Turn off state** in which first super capacitor is charged by rectifier and rest of the system will be cutoff from supply i.e less than 1.9V

Chapter 7:

Conclusion

The thesis presents a remotely powered dual band RF energy harvesting system at 953MHz and 2.4GHz frequencies. The simulations were carried out at both schematic and layout level 0.18 m technology for complete system with 4W EIRP transmitted from RF source. Through simulations optimum number of stages of rectifier to generate an output voltage of 1V is identified. The power management circuit is designed. For given input power there exists an optimum load resistance where maximum system efficiency is obtained because of limitations associated with LDO. Finally comparison with existing literature shows the proposed Dual band RF energy harvesting system has a better power conversion efficiency and a smaller form factor for energy harvesting system with lesser hardware and ultra low power sensitivity devices. It concludes with idea of constant voltage and constant current charging of the battery.

References

[2] Mokwa Wilfred, Uwe Schnakenberg“Micro Transponders for Medical Applications IEEE Transc. Instrumentation and Measurements.

[3] Kouji Kiyoyama, Yoshito Tanaka, Mashahiro Onoda,Takafumi,Fukushima,Tetsu Tanaka, Mitsumasa Koyanagi “A Closed-loop Power Control Function for Bio-implantable devices ”,IEEE Asian Solid-State Circuits, Nov. 2008.

[4] S Keyrouz,y, H J Visseryand A G Tijhuis, “Multi-band Simultaneous Radio Frequency Energy Harvesting,EUCAP 2013, 2013.

[5] C Phongcharoenpanich, R Suwalak ,“Dual-band RFID-reader antenna using annular plate with curved and rectangular slots”,ICEAA,pp. 633- 636, 2010.

[6] Bo Li, Xi Shao, Negin Shahshahan, Neil Goldsman, Thomas Salter, George M Metze“ An Antenna Co-Design Dual Band RF Energy Harvester,IEEE TCAS-I VOL. 60, Dec. 2013.

[7] Phirun Kim, Girdhari Chaudhary, and Yongchae Jeong A Dual-Band RF Energy Harvesting Using Frequency Limited Dual-Band Impedance Matching, Progress In Electromagnetics Research,Vol. 141, pp.443-461, 2013.

[8] Toshiyuki Umeda, Hiroshi Yoshida, Shuichi Sekine, Yumi Fujita, Takuji Suzuki, Shoji Otaka “A 950-MHz Rectifier Circuit for Sensor Network Tags With 10-m Distance”,IEEE Journal Of Solid-State Circuits,Jan. 2006.

[9] Atsushi Sasaki, Koji Kotani, Takashi Ito “Differential-Drive CMOS Rectifier for UHF RFIDs with 66 % PCE at -12 dBm Input”, IEEE Asian Solid-State Circuits Conference,Nov. 2008.

[10] Ka Nang Leung, Philip K T Mok “A CMOS Voltage Reference Based on Weighted 4VGS for CMOS Low-Dropout Linear Regulators”,IEEE Journal Of Solid-State Circuits,Jan. 2003.

[11] R. Barnett, J. Liu, and S. Lazar “A RF to DC voltage conversion model for multi-stage rectifiers in UHF RFID transponders”,IEEE Journal of Solid-State Circuits, 2009.

[12] Ming-Dou, Shih-Lun Chen, Chia-Shen Tsai“Design of Charge Pump Circuit with consideration of Gate oxide Relaibility in Low voltage CMOS Process ”, IEEE Journal of Solid-State Circuits, 2006.vol. 41, pp. 1100 to 1106.

[13] Koji Kotani,Takashi Ito“High Efficiency CMOS Rectifier Circuit with self Vth Cancellation and Power regulation Functions for UHF RFIDs”, IEEE Asian of Solid-State Circuits Conference, Nov.12 - 2007, Jeju Korea
.
[14] U. Karthaus, M. Fischer, ”Fully Integrated Passive UHF RFID Transponder IC With 16.7-_W Minimum RF Input Power,” IEEE Journal of Solid-State Circuits, vol. 38, no. 10, pp. 1602-1608, Jan 2003.

[15] S. Mandal, R Sarpeshkar, “Low power CMOS Rectifer Design for RFID Applications” IEEE Transactions on Circuits and system -I, vol. 54, no. 6, pp. 1177-1188, July, 2007.

[16] Onur Kozanc,A. Jose, Manuel Delgado, Franco Maloberti, Catherin Dehollian “Far Field UHF Remotely Powered front end Patient monitoring with wearable antenna”, IEEE, 2013.

[17] Chia-Chin Liu and Chunhong Chen“An Ultra-Low Power Voltage Regulator. for RFID Application”, IEEE, 2013.

[18]. J. F. Dickson, “On-chip high-voltage generation in NMOS integrated circuits using an improved voltage multiplier technique,” IEEE J. Solid-State Circuits, vol. SSC-11, no. 3, pp. 374–378, Jun. 1976.

[19] F. Carrara, G. Papotto, and G. Palmisano, “Methodology and circuits for threshold compensation in voltage multipliers,” IT patent appl. no.MI09A001646filed, Sep. 9, 2009.

[20] M.-D. Ker, S.-L. Chen, and C.-S. Tsai, “Design of charge pump cir-cuit with consideration of gate-oxide reliability in low-voltage CMOS processes,”IEEE J. Solid-State Circuits, vol. 41, no. 5, pp. 1100–1107, May 2006.