State Separate Modular Modeling Methodology of Multioutput DC–DC Converters

Nithin Thomas Abraham, *Graduate Student Member, IEEE*, Gajendranath Chowdary, *Member, IEEE*, and Dhanaraj Kakkanattu Jagalchandran, *Member, IEEE*

***Abstract*—Conventional modeling and simulation of n-output dc–dc converters requires $(n+1) \times (n+1)$ matrix computations. This approach increases the modeling approach's complexity and increases the design and simulation time required for the modeling process. A state separate modeling methodology is proposed where each state of the dc–dc converter is considered separately and combined with the help of a multiplexer. The proposed modeling approach is modular and thus improves the scalability to multiple outputs. The proposed methodology aids the designer in designing and modeling multioutput dc–dc converters faster, enabling fast prototyping. The proposed model outperforms the existing mathematical models in terms of computation time. The output voltage variation to duty cycles has a root mean square error in between 0.08 and 0.22 V.**

***Index Terms*—DC–DC converters, modeling, multioutput.**

I. Introduction

RECENT developments in wireless sensor nodes and energy scavenging techniques paved the way for implementing autonomous sensors. These sensors have a wide range of applications in biomedical implants, the Internet of Things (IoT), and emerging devices in 5G. Both battery operated and energy harvesting systems demand a custom power management unit (PMU) to meet various power supply requirements of the sensors and actuators. In modern portable electronic devices, a power management integrated circuit (PMIC) plays a vital role in delivering power from an input battery source to different modules in such devices. Regardless of the battery's state of charge (SoC), PMU should provide different voltages. It also should maintain high efficiency in light load as these devices spend a significant portion of their lifetime in idle or sleep mode. Moreover, the PMIC should be small in size to meet the sizing requirements of portable electronic devices. A single inductor multiple-output (SIMO) converter [1]–[12] provides an elegant solution in terms of area and efficiency which is capable of meeting multioutput requirements.

Manuscript received 29 December 2021; revised 3 April 2022 and 25 May 2022; accepted 19 June 2022. Date of publication 27 June 2022; date of current version 20 February 2023. This article was recommended by Associate Editor N. Wong. *(Corresponding author: Nithin Thomas Abraham.)*

Nithin Thomas Abraham and Dhanaraj Kakkanattu Jagalchandran are with the Department of Electronics and Communication, National Institute of Technology Calicut, Kozhikode 673601, India (e-mail: nithinthomasabraham93@gmail.com).

Gajendranath Chowdary is with the Department of Electrical Engineering, Indian Institute of Technology Hyderabad, Hyderabad 502285, India.

Digital Object Identifier 10.1109/TCAD.2022.3186492

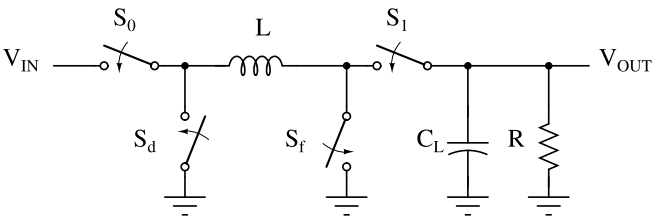

Fig. 1. Four switch topology of a buck-boost converter.

Modeling and simulation of a dc–dc converter is an important step in designing and developing a PMIC. For a multioutput dc–dc converter, equations become more complicated, making the designing process time-consuming and hard. Many modeling techniques were introduced during the past years [13]–[21] for single output dc–dc converters. Among them, state-space averaging (SSA) and circuit averaging (CA) plays a prominent role in accurately predicting the converter behavior.

The portable electronics market demands a smaller size, and hence off-chip components of PMIC will have certain size limitations. Also, another demanding requirement of a portable electronic device is low battery consumption. Low power modes are adopted to reduce battery consumption, and hence sensors may have to stay in light load conditions more often. A dc–dc converter based on PWM operates either in continuous conduction mode (CCM) or discontinuous conduction mode (DCM). Even though CCM ensures low peak current and high efficiency, DCM is a stringent requirement for small inductance and light load situations. Among the various DCM models ([11], [13], [20], [22], [23]), Sun *et al.* [20] claimed the highest accuracy. However, this article validates its model under specific conditions and fails to generalize this model to all types of converters. The CA method proposed by Vorpérian [22] often proved better than improved SSA [20] in some conditions [23]. Both CA and SSA together inspire researchers to come up with more accurate models. The main problem with the SSA and CA is the derivation of small-signal equations that needs to be repeated whenever the circuit topology changes. Fig. 1 represents a generalized circuit representation of a single inductor single-output (SISO) dc–dc converter. Recent developments in PMIC design allow designers to use a single shared inductor for multiple output topologies. Thus, an SISO to single inductor dual output (SIDO) conversion only requires an extra switch and an extra

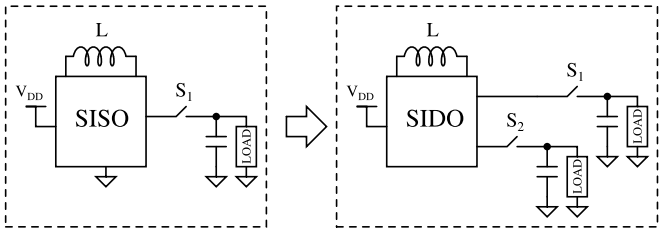

Fig. 2. SISO to SIDO conversion.

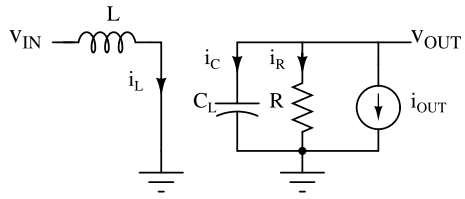

Fig. 3. State 0.

capacitor as shown in Fig. 2. However, this simple change in topology requires repeating the small-signal derivation. Thus, it makes the modeling process time consuming.

Even though many SIMO architectures are proposed in the literature, only a few [24], [25] are available for the modeling and simulation of SIMO converters. Patra *et al.* [24] proposed a model which is further modified accurately by Abbasi *et al.* [25]. Both models provide a modeling approach to single inductor multiple output dc–dc converters. However, they are not generalized to an n-output scenario. The model becomes highly complex when the number of outputs (n) increases. This article proposes a fast, modular approach to model multiple output dc–dc converters using multiplexed states of a single output dc–dc converter. Existing models require $(n+1)\times(n+1)$ matrices to predict the behavior of n-output dc–dc converter, whereas the proposed model requires only 2×2 matrices. Hence, compared to other mathematical models, the time required to calculate the model parameters in the proposed model will be significantly less. The approach reduces the designing complexity and motivates a more generalized method for the modeling and simulation of multioutput dc–dc converters. Section II starts with the general mathematical modeling of dc–dc converters and addresses the various problems faced in the modeling process. Section II also introduces the new modeling methodology and compares this methodology with other existing models in the literature. Results and simulation can be found in Section III, where the proposed model is compared with existing models in the literature and physical model simulation.

II. Mathematical Modeling of DC–DC Converters

SSA is governed by two equations

$$\dot{x} = Ax + Bu \tag{1}$$

$$y = Cx + Du \tag{2}$$

state space (1) and the output (2) where x is the state vector, y is the output vector, A, B, C, and D are state, input, output, and feed-through matrix, respectively.

Circuit behavior can be captured through A, B, C, and D matrices. This article addresses common problems in modeling dc–dc converters and proposes a novel generalized fast modeling technique.

A. DC Analysis of Single Inductor DC–DC Converters

Conventional four-switch buck-boost topology is shown in Fig. 1. A buck-boost topology is the most generalized topology for a dc–dc converter, where both buck and boost outputs can be generated. There are three states in the operation of a four-switch buck-boost dc–dc converter. In State 0, S_0 and S_f are closed and S_d and S_1 are open. State 0 represents energizing state during which inductor gets energized. In State 1, S_0 and S_f are open and S_d and S_1 are closed. State 1 represents discharging state during which inductor discharges to the output capacitor. A state set, "States" can be defined as States = {State 0, State 1, State DCM} for single output dc–dc converters, where State DCM is the state in which both S_0 and S_1 are open and S_d and S_f are closed. In State DCM, inductor current freewheels through S_d and S_f. The "States" set can be expanded to include multiple outputs such that States = {State 0, State 1, State 2, ..., State n, State DCM}, where State 0 is the energizing state, State 1, State 2,..., State n are the discharging states and State DCM is the state where inductor current remains constant by freewheeling.

State 0: In State 0, S_0 and S_f switches will be ON and S_1 and S_d switches will be OFF. The inductor L, will be energized from battery source v_{IN} and output will be disconnected from the inductor during State 0. The circuit equivalent model for state 0 of the buck-boost topology is given in Fig. 3. The inductor current is given by (3) and the capacitor voltage is given by (4) where, v_C is the voltage across capacitor C_L, i_L is the inductor current, and i_{OUT} shows the load modulation at the output [24]

$$\frac{di_L}{dt} = \frac{v_{\mathrm{IN}}}{L} \tag{3}$$

$$\frac{dv_C}{dt} = \frac{1}{C_L}\left(\frac{-v_C}{R} - i_{\mathrm{OUT}}\right). \tag{4}$$

From the (3) and (4) the state and output equations can be formulated as follows:

$$\begin{bmatrix} \dot{i_L} \\ \dot{v_C} \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & \frac{-1}{RC_L} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{-1}{C_L} \end{bmatrix} \begin{bmatrix} v_{\mathrm{IN}} \\ i_{\mathrm{OUT}} \end{bmatrix} \tag{5}$$

$$\begin{bmatrix} v_{\mathrm{OUT}} \\ i_L \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} v_{\mathrm{IN}} \\ i_{\mathrm{OUT}} \end{bmatrix}. \tag{6}$$

State 1: In State 1, S_0 and S_f switches will be OFF and S_1 and S_d switches will be ON. The inductor L, will get discharged to the output, charging the output capacitor. The circuit equivalent for state 1 of the buck-boost topology is given in Fig. 4. The inductor current is given by (7) and the capacitor voltage is given by (8)

$$\frac{di_L}{dt} = \frac{-v_C}{L} \tag{7}$$

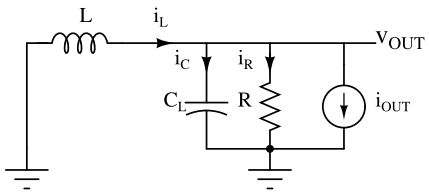

Fig. 4. State 1.

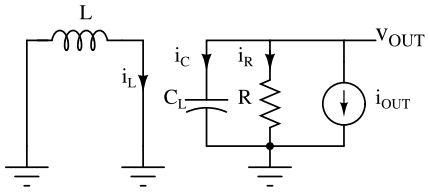

Fig. 5. State DCM.

$$\frac{dv_C}{dt} = \frac{1}{C_L}\left(i_L - \frac{v_C}{R} - i_{\text{OUT}}\right). \tag{8}$$

From (7) and (8) the state and output equations can be formulated as (9) and (10), respectively

$$\begin{bmatrix} \dot{i_L} \\ \dot{v_C} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-1}{L} \\ \frac{1}{C_L} & \frac{-1}{RC_L} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & \frac{-1}{C_L} \end{bmatrix} \begin{bmatrix} v_{\text{IN}} \\ i_{\text{OUT}} \end{bmatrix} \tag{9}$$

$$\begin{bmatrix} v_{\text{OUT}} \\ i_L \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} v_{\text{IN}} \\ i_{\text{OUT}} \end{bmatrix}. \tag{10}$$

State DCM: In State DCM, inductor L is given a freewheeling path so that the inductor current remains constant. A freewheeling path can be provided to the inductor current when S_d and S_f are closed. An equivalent circuit model of state DCM of the buck-boost topology is given in Fig. 5. The inductor current in State DCM and the capacitor voltage are given by

$$\frac{di_L}{dt} = 0 \tag{11}$$

$$\frac{dv_C}{dt} = \frac{1}{C_L}\left(\frac{-v_C}{R} - i_{\text{OUT}}\right). \tag{12}$$

From (11) and (12) the state and output equations can be formulated as follows:

$$\begin{bmatrix} \dot{i_L} \\ \dot{v_C} \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & \frac{-1}{RC_L} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & \frac{-1}{C_L} \end{bmatrix} \begin{bmatrix} v_{\text{IN}} \\ i_{\text{OUT}} \end{bmatrix} \tag{13}$$

$$\begin{bmatrix} v_{\text{OUT}} \\ i_L \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} v_{\text{IN}} \\ i_{\text{OUT}} \end{bmatrix}. \tag{14}$$

B. State Separate Model

SSA is a method to combine all the states into a single state-space equation. When the number of outputs increases, the state space equations become more complicated and require huge time for deriving state and output equations. It is important to consider the complexity of the equation in terms of dimensionality as it imports a huge toll in time taken to derive the model. For an n output, single inductor dc–dc converter, matrices of order $(n+1)$ are required. SSA can be represented by (15) and (16), where, A_0, A_1, A_{DCM}, B_0, B_1, and B_{DCM} are the state and input matrices of State 0, State 1, and State DCM, respectively. d_0 and d_1 are duty cycle variable for State 0 and State 1. Duty cycle for State DCM is $1 - d_1 - d_0$. Averaged state matrix A, and averaged input matrix B can be written as follows:

$$A = A_0 d_0 + A_1 d_1 + A_{\text{DCM}}(1 - d_0 - d_1) \tag{15}$$

$$B = B_0 d_0 + B_1 d_1 + B_{\text{DCM}}(1 - d_1 - d_0). \tag{16}$$

On evaluating (15) and (16), the equations can be rearranged to get

$$\dot{x} = \underbrace{(A_0 x + B_0 u)}_{\text{State 0}} d_0 + \underbrace{(A_1 x + B_1 u)}_{\text{State 1}} d_1 + \underbrace{(A_2 x + B_2 u)}_{\text{State DCM}} d_{\text{DCM}} \tag{17}$$

where $d_{\text{DCM}} = 1 - d_0 - d_1$. Small signal equations of each state can be derived separately using (17). These states can be combined with the help of a multiplexer, as shown in Fig. 6, and averaging can be done using a low pass filter (LPF). Multiplexer inputs are selected using D_0, D_1, and D_{DCM}, where D_0, D_1, and D_{DCM} are the clock signals corresponding to State 0, State 1, and State DCM. An LPF at the output of the multiplexer is added to reduce the abrupt change in state transitions. This novel method simplifies the modeling process and provides an effective way to generalize the same for multiple output dc–dc converters.

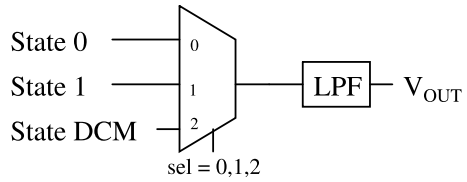

Fig. 6. Multiplexing different states into one output.

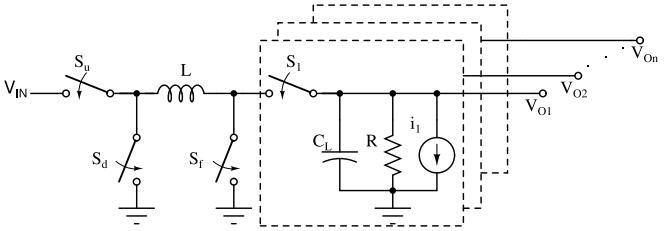

Fig. 7. Single inductor multiple output topology.

Fig. 7 represents a single inductor multiple output dc–dc converter topology with n outputs with $i_1, i_2, \ldots, i_n$ as output currents. S_u and S_f switches are used to charge the inductor, S_d and S_i are used to discharge to each output V_{O1} to V_{On}. Since there are n outputs, there will be $n+2$ states ($n+1$ states for CCM and one state for DCM) and the state set can be defined as States = {State 0, State 1, State 2, ..., State n, State DCM}.

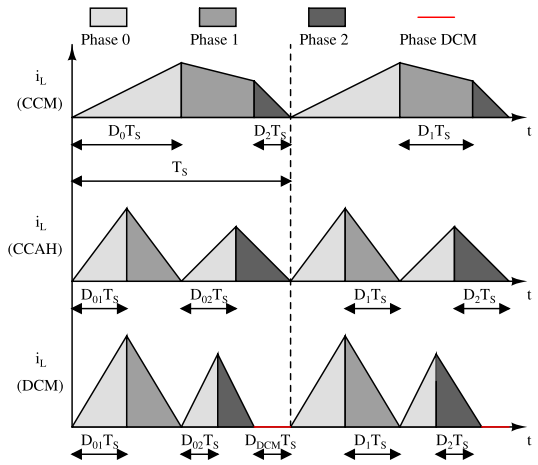

Fig. 8. Inductor current waveform for various clocking schemes.

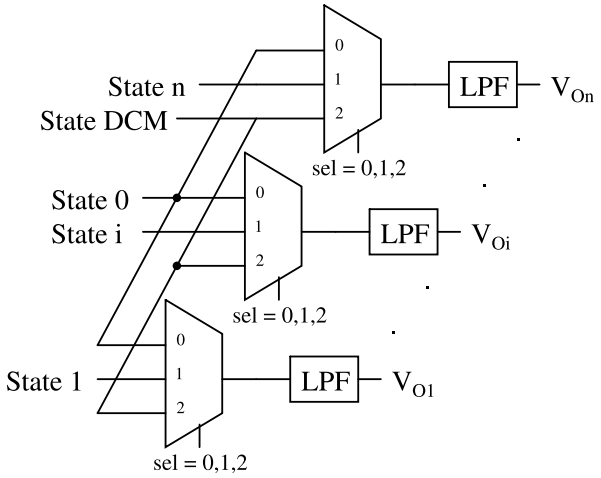

Fig. 9. Generalized block schematic of multiple output dc–dc converter.

Even though there are $n+2$ states, for simplicity these states can be categorized into three states, State 0, State 1, and State DCM. State 0 represents the energizing state, State 1 represents the discharging state corresponding to V_{Oi}, and State DCM represents idle state. Fig. 8 shows the various clocking schemes for single inductor multiple output dc–dc converters, such as CCM, constant charge auto hopping (CCAH) [26], and DCM. From Fig. 8, it is clear that, all clocking schemes can be realized using three states (State 0, State i, and State DCM, where $i = 1,\ 2, \ldots,\ n$). Steady state inductor current in State 0 can be represented using (18), State i using (19), and State DCM using (20)

$$\frac{di_L}{dt} = \frac{V_{\text{IN}}}{L} \tag{18}$$

$$\frac{di_L}{dt} = \frac{V_{\text{IN}} - V_{Oi}}{L},\ i = 1,\ 2, \ldots,\ n \tag{19}$$

$$\frac{di_L}{dt} = 0. \tag{20}$$

By using this idea, the model in Fig. 6 can be modified to a more generalized model which incorporates multiple outputs. It is to be noted that, unlike CCM, CCAH, and DCM have separate charging state for each output. Hence, there can be $2n+1$ states for an n output dc–dc converter. It is also to be noted that, pseudo CCM (PCCM) [27] is a special case of DCM where inductor current remains at a constant dc level instead of zero inductor current. However, assuming CCM operation, all the charging states can be combined as one state, limiting the total number of states to $n+1$.

Fig. 9 shows a generalized model for multiple output dc–dc converter, where each multiplexer selects the states according to state selection control. The multiplexer generates individual outputs, which is further smoothed to reduce switching effects using an LPF. This approach can be used to create multioutput models from available single input models of dc–dc converters by extracting individual states and combining with the help of multiplexers to generate multiple outputs. The approach is demonstrated and compared in the following section. The model created by this methodology will be mentioned as the proposed model hereafter.

C. Comparison With Existing Models

An SIDO dc–dc converter is chosen for the comparison with existing models, where D_0 is the duty cycle during the energizing state, and D_1 and D_2 are the duty cycles corresponding to discharging state of each output, V_1 and V_2.

1) State Space Averaging: The A and B matrices of the state space averaging model is shown in the following:

$$A = \begin{bmatrix} 0 & -\dfrac{D_1}{L} & -\dfrac{D_2}{L} \\ \dfrac{D_1}{C_L} & -\dfrac{1}{RC_L} & 0 \\ -\dfrac{D_2}{C_L} & 0 & -\dfrac{1}{RC_L} \end{bmatrix} \tag{21}$$

$$B = \begin{bmatrix} \dfrac{D_0}{L} & 0 & 0 & -\dfrac{V_1}{L} & -\dfrac{V_2}{L} \\ 0 & -\dfrac{1}{C_L} & 0 & \dfrac{i_L}{C_L} & 0 \\ 0 & 0 & \dfrac{-1}{C_L} & 0 & \dfrac{i_L}{C_L} \end{bmatrix}. \tag{22}$$

2) Ripple Space Model: The A an B matrices of the model is shown in the following:

$$A = \begin{bmatrix} 0 & -\dfrac{D_1}{L} & -\dfrac{D_2}{L} \\ \dfrac{D_1}{C_L} & -\dfrac{1}{RC_L} - \dfrac{D_1T_s}{LC_L} - \dfrac{D_0D_1T_S}{2LC_L} & 0 \\ -\dfrac{D_2}{C_L} & -\dfrac{D_1D_2T_s}{LC_L} + \dfrac{D_0D_1D_2T_S}{2LC_L} & -\dfrac{1}{RC_L} \end{bmatrix} \tag{23}$$

$$B = \begin{bmatrix} \dfrac{1}{L} & 0 & 0 & -\dfrac{V_1}{L} & -\dfrac{V_2}{L} \\ \sigma_4 & -\dfrac{1}{C_L} & 0 & \dfrac{i_L}{C_L} - \sigma_2 & 0 \\ D_2\sigma_3 & 0 & \dfrac{-1}{C_L} & V_{in}\sigma_3 & \sigma_5 \end{bmatrix} \tag{24}$$

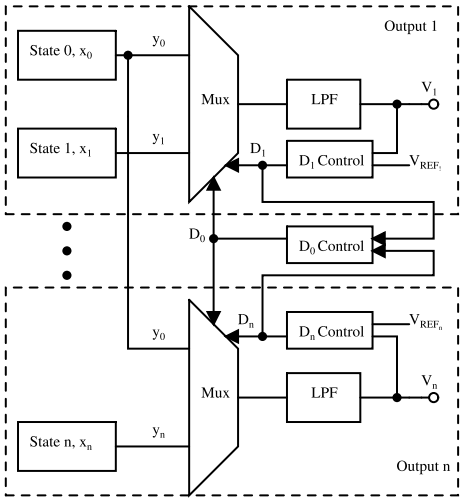

Fig. 10. Block diagram representation of proposed model for single inductor n output dc–dc converter.

where

$$\sigma_0 = \frac{D_0 T_S}{LC_L}, \sigma_1 = \frac{D_1 T_S}{LC_L}$$
$$\sigma_2 = V_1\left(\sigma_1 - \frac{D_0 D_1 T_S}{2LC_L}\right)\sigma_3 = \sigma_1 - \frac{D_0 D_1 T_S}{LC_L}$$
$$\sigma_5 = \frac{i_L}{C_L} - \sigma_2 + V_{\text{in}}\sigma_3 \quad \sigma_4 = D_1\left(\frac{\sigma_0}{2} - \sigma_1 - D_1\sigma_0\right).$$

After defining A and B matrices for state space model and ripple space model, state equations can be defined using (1) and (2) where

$$C = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}, \quad D = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}. \tag{25}$$

Since the modeling is only done for dual output converters, the number of rows of the A, B, C, and D matrices of the state equations is three. Finding A and B matrices, even for a dual output converter, is time consuming and mathematically complex. To design a model for n output dc–dc converter finding A and B matrices of the order $n+1$ acts as a bottleneck for multiple output modeling and simulation.

3) Proposed Model: The proposed model simplifies the modeling and simulation process by separating states combining them later based on the clocking scheme. For an n output dc–dc converter, there will be $n+1$ states, and each state can be represented by a 2×2 matrix. A 2×2 matrix makes modeling and computation easier than an $(n+1)\times(n+1)$ matrix. Fig. 10 shows the schematic block diagram of the proposed model for an n-output single inductor dc–dc converter. For a two-output dc–dc converter, the proposed model uses scaled addition of states to get outputs V_1 and V_2. The state equation in (1) can be rearranged as follows:

$$\dot{x} = (A_0 d_0 + A_1 d_1 + A_2 d_2)x + (B_0 d_0 + B_1 d_1 + B_2 d_2)u \tag{26}$$
$$\dot{x} = (A_0 x + B_0 u)d_0 + (A_1 x + B_1 u)d_1 + (A_2 x + B_2 u)d_2 \tag{27}$$

where

$$A_0 = \begin{bmatrix} 0 & 0 \\ 0 & \dfrac{1}{RC_L} \end{bmatrix}, \quad B_0 = \begin{bmatrix} \dfrac{1}{L} & 0 \\ 0 & -\dfrac{1}{C_L} \end{bmatrix} \tag{28}$$

$$A_1 = \begin{bmatrix} 0 & -\dfrac{1}{L} \\ \dfrac{1}{C_L} & -\dfrac{1}{RC_L} \end{bmatrix}, \quad B_1 = \begin{bmatrix} 0 & 0 \\ 0 & -\dfrac{1}{C_L} \end{bmatrix}. \tag{29}$$

From (2) and (25), the output equation can be represented as follows:

$$y = C\int \dot{x} = C\int \sum_{i=1}^{2}\left[\left(\frac{A_0}{k_0}x + \frac{B_0}{k_0}u\right)d_0 + (A_i x + B_i u)d_i\right] \tag{30}$$

where, k_0 is the state weight and $i = 1$ and 2. Each state can be separated and multiplied with clock variables d_0 and d_i to generate output equation as in (30). State weight k_0 is calculated by taking the number of state sets for the discharging state. Since the number of discharging states is the same as the number of outputs. $k_0 = n$. The weighted addition of states is done by the multiplexer, and the integration function is implemented as an LPF at the output. The converter outputs V_1 and V_2 for the designed dual output converter are modeled as follows:

$$V_1 = \frac{1}{k_0}y_0 + y_1 \tag{31}$$
$$V_2 = \frac{1}{k_0}y_0 + y_2 \tag{32}$$

where $y_0 = C\int(A_0 x + B_0 u)d_0$, $y_1 = C\int(A_1 x + B_1 u)d_1$, and $y_2 = C\int(A_2 x + B_2 u)d_2$. k_0 is state weight which is calculated using number of charging/discharging states.

Fig. 10 is the block diagram representation of the proposed model structure. The proposed model is compared with the ripple space model and SSA for dual output dc–dc converter. For an n output dc–dc converter the model can be generalized as follows:

$$y = C\int \sum_{i=1}^{n}\left[\left(\frac{A_0}{k_0}x + \frac{B_0}{k_0}u\right)d_0 + (A_i x + B_i u)d_i\right] \tag{33}$$
$$V_n = \frac{1}{k_0}y_0 + y_i \tag{34}$$

where, $y_0 = C\int(A_0 x + B_0 u)d_0$ and $y_i = C\int(A_i x + B_i u)d_i$ and k_0 is the scaling factor for each state depending upon the use cases (charging/discharging) of dc–dc converters.

III. Results and Simulations

The proposed model is validated comparing its result with that of an experimental setup and physical model simulation. For the experimental setup and evaluation, an operating frequency of 15 and 100 kHz is chosen whereas for model evaluation and comparison with existing models, an operating frequency of 1 MHz is chosen.

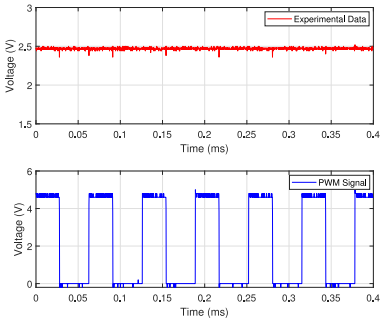

Fig. 11. Steady-state response of experimental circuit and corresponding PWM signal for single output dc–dc converter.

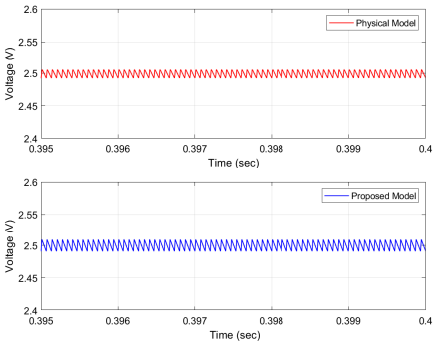

Fig. 12. Steady-state response of the physical model and proposed model for single output dc–dc converter.

A. Experimental Setup and Results

A single output buck dc–dc converter is chosen first, for the comparison with the proposed model. Fig. 11 shows the experimental results of an SISO converter with an operating frequency of 15 kHz, input voltage $V_{\text{IN}} = 5$ V and output voltage $V_1 = 2.5$ V using a 680-μH inductor and 50-μF capacitor. A physical model designed in MATLAB Simulink is also used to compare the simulation results with the proposed model with $V_{\text{IN}} = 5$ V and operating frequency of 15 kHz. The proposed model uses a two-input multiplexer with State 0 and State 1 as inputs. A 15-kHz PWM signal is used to switch between State 0 (energizing) and State 1 (discharge). An LPF is used to filter the effects of multiplexer switching. Fig. 12 shows the steady-state responses of the proposed model and physical model. A steady-state error of -36, 3, and 5 mV is obtained for experimental, physical, and proposed models, respectively. Fig. 13 shows the steady-state response of dual output dc–dc converter with a steady-state error of 20 mV for V_1 and -26 mV for V_2. The model is also evaluated in the same setup with an operating frequency of 100 kHz using a 100-μH inductor and 50-μF capacitor. Steady-state error for experimental, physical, and proposed models are shown in Table I. Even though the physical model has the lowest average steady-state error, the computational time require to generate the required output is extremely high ($>$ 65 min) whereas the proposed models compute the output values within seconds.

Dynamic responses are evaluated using the physical model. Fig. 15(a) and (b) compares the physical model and proposed model for different closed-loop reference voltage. In Fig. 15(a), V_{REF_1} is changed from $V_{\text{REF}_1} = 3.3$ V to $V_{\text{REF}_1} = 2.5$ V driving V_1 from boost mode to buck mode. Similarly in Fig. 15(b), V_{REF_2} is changed from $V_{\text{REF}_2} = 2.5$ V to $V_{\text{REF}_2} = 3.3$ V driving V_2 from buck mode to boost mode. A 1% average deviation and 15% maximum deviation is observed between the proposed and physical model simulations. Patra *et al.* [24] observed a 5% average deviation and 10% maximum deviation between the proposed and physical model. Transient response of the proposed model differs from the physical model based on the parameters of the LPF. An LPF with higher cut-off frequency can be used to enable a faster transient response. A higher-order filter also should be used to mitigate the multiplexer switching noise. An initial delay in transient response is observed while using higher-order filters. Fig. 15(a) and (b) demonstrates the comparison of transient behavior of the physical model with that of: 1) proposed model using a first-order LPF of cutoff frequency 500 Hz as an output filter and 2) the proposed model using a 10th order LPF of cutoff frequency 500 Hz as output filter. The

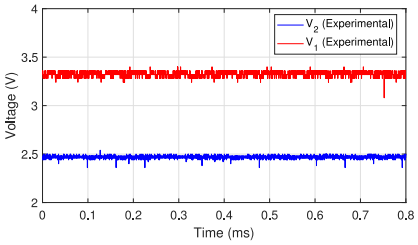

Fig. 13. Steady-state response of V_1 and V_2 of experimental circuit for dual output dc–dc converter.

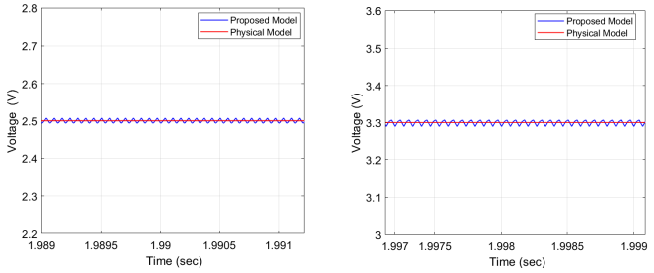

Fig. 14. Steady-state response of (a) V_1 and (b) V_2 for the physical model in comparison with the proposed model.

TABLE I
STEADY-STATE ERROR FOR EXPERIMENTAL, PHYSICAL, AND PROPOSED MODELS

	Steady State Error (in mV)					
	15 kHz			100 kHz		
	SISO	SIDO		SISO	SIDO	
	V_1	V_1	V_2	V_1	V_1	V_2
Experimental	-36	20	-26	16	24	20
Physical Model	3	0.1	0.12	2	0.3	0.34
Proposed Model	5	0.3	0.3	2.8	0.4	0.48

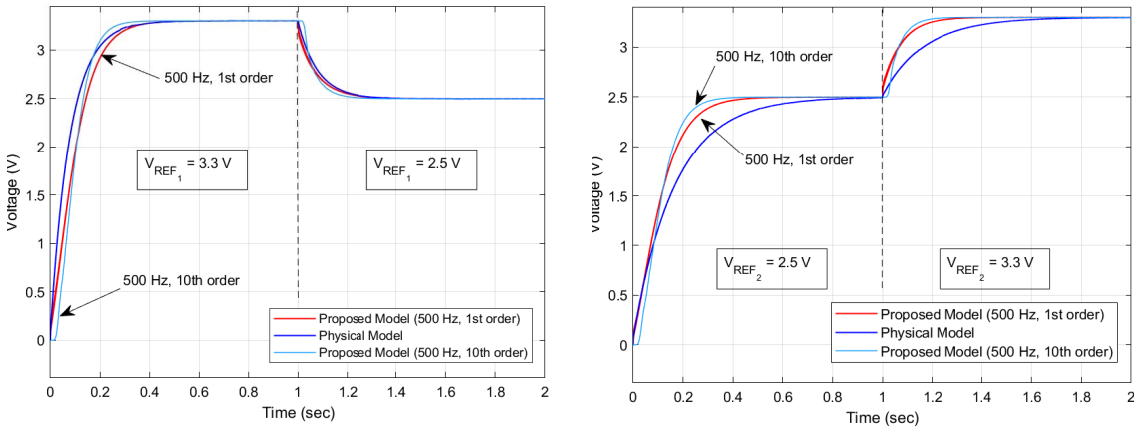

Fig. 15. (a) Transient response of V_1 for the physical model with proposed model at $V_{\text{REF}_1} = 3.3$ V and $V_{\text{REF}_1} = 2.5$ V. (b) Transient response of V_2 for the physical model with proposed model at $V_{\text{REF}_2} = 3.3$ V and $V_{\text{REF}_2} = 2.5$ V.

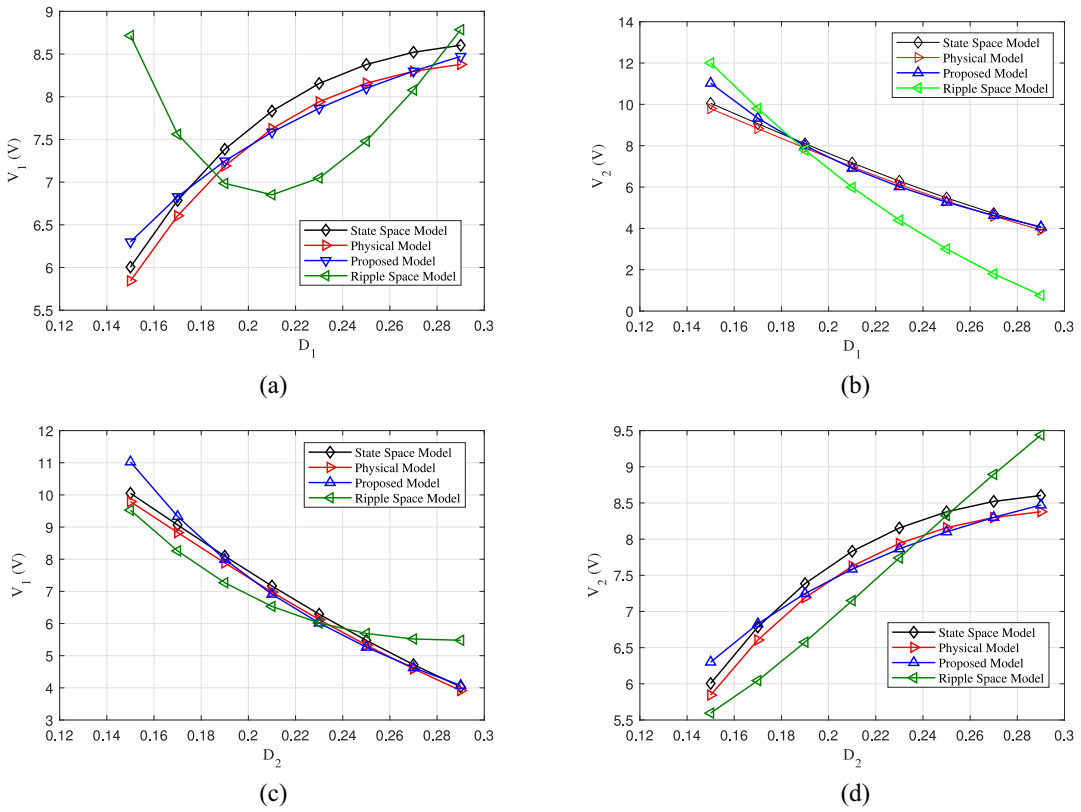

Fig. 16. (a) Change in V_1 with D_1 while keeping D_0 and D_2 constant. (b) Change in V_2 with D_1 while keeping D_0 and D_2 constant. (c) Change in V_1 with D_2 while keeping D_0 and D_1 constant. (d) Change in V_2 with D_2 while keeping D_0 and D_1 constant.

initial delay in response can be avoided using a higher cutoff frequency for the LPF. An LPF with higher order and higher cutoff frequency can be used for a faster dynamic response which further increases the complexity of the model.

B. Model Evaluation and Comparison With Existing Models

Model evaluation is performed with an operating frequency of 1 MHz, $V_{\text{IN}} = 2.7$ V, and expected output voltages of $V_1 = 3.3$ V and $V_2 = 2.5$ V using a 4.7-μH inductor and 10-μF capacitor. Fig. 16 shows the comparison of open-loop output voltage with change in duty cycle for both physical and mathematical models. D_1 and D_2 is taken less than 30% (as in [24]) because, converter topology considered demands more duty cycle for D_0 since the charge accumulated during D_0 is feeding both V_1 and V_2. Table II shows the root mean square error and worst-case error of mathematical models in comparison with the physical model for Fig. 16. Even though, the proposed model is a low complex model, it gives comparable accuracy in comparison with existing mathematical models.

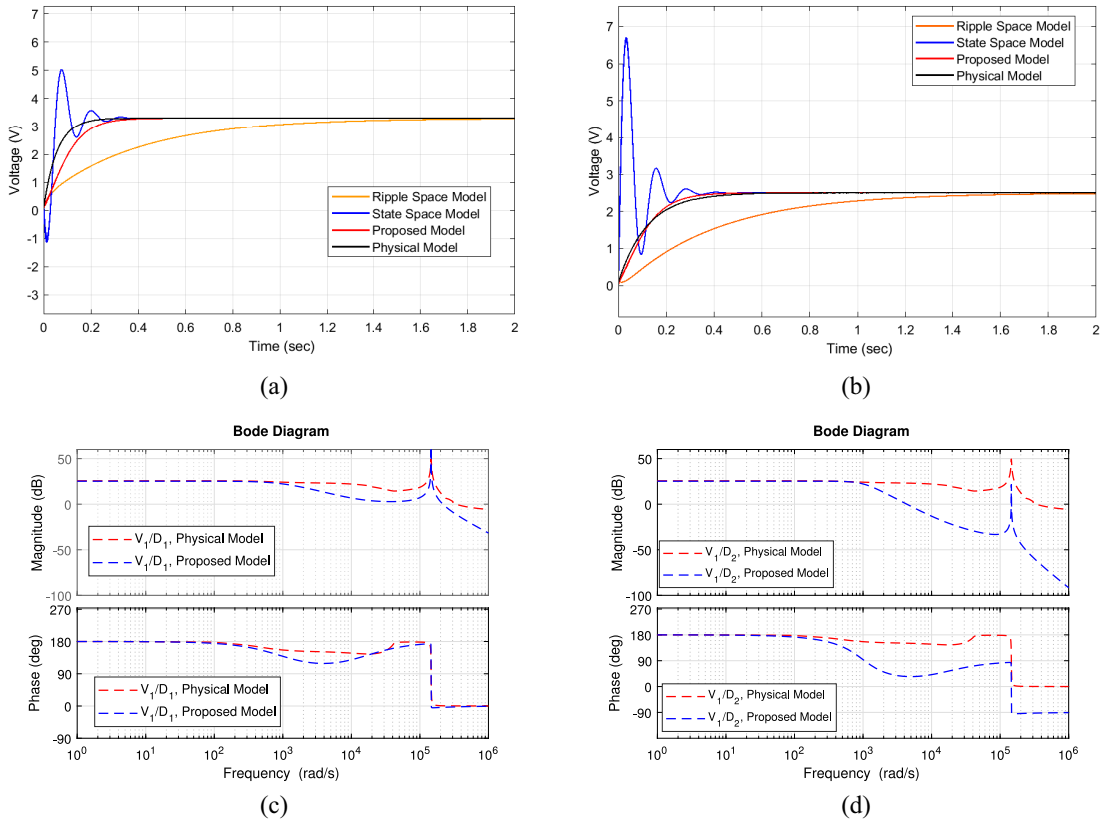

Fig. 17. (a) Output voltage V_1. (b) Output voltage V_2. (c) Control transfer function, $(V_1/D1)$. (d) Cross-coupled transfer function, $(V_1/D2)$.

TABLE II
ROOT MEAN SQUARE AND WORST-CASE ERROR FOR MATHEMATICAL MODELS IN COMPARISON WITH THE PHYSICAL MODEL

	State Space Model		**Ripple Space Model**		**Proposed Model**	
	Root mean square error (V)	Worst case error (V)	Root mean square error (V)	Worst case error (V)	Root mean square error (V)	Worst case error (V)
V1 vs D1 (Fig. 16(a))	0.2	0.28	0.18	2.4	0.08	1.2
V2 vs D1 (Fig. 16(b))	0.18	0.27	0.98	2.2	0.22	1.23
V1 vs D2 (Fig. 16(c))	0.18	0.25	0.1	1.5	0.22	0.55
V2 vs D2 (Fig. 16(d))	0.2	0.22	0.03	1	0.08	0.45

Duty cycle ranges used for D_0, D_1, and D_2 are in between 10% and 90%. 10% buffer is given because, the product term for that particular duty cycle will tend to zero and output will tend to zero for duty cycles near to 0%. If duty cycles are near to 100%, other duty cycles do not have enough time to contribute.

Output convergence plot for mathematical models can be viewed in Fig. 17. Fig. 17(a) shows the output voltage V_1 which is expected to be at 3.3 V and Fig. 17(b) shows V_2 which is expected to be at 2.5 V for an input voltage $V_{\text{IN}} = 2.7\ V$. All three models are simulated with the same control block. The proposed model converges faster than other models. It is observed that both the proposed model and the state space model have comparable steady-state responses. Computation time and steady-state error obtained for the mathematical models are as given in Table III when the mathematical models and physical model are simulated using an Intel Xeon E5 CPU with NVIDIA Quadro K2000 having 8-GB RAM and 500-GB HDD with a base clock of 3.75 GHz. It is observed that for multiple output models, proposed model performs better than existing mathematical models. Control transfer functions and cross-coupled transfer functions of the proposed model and physical model, for the output V_1, for duty cycles D_1 and D_2 are given in Fig. 17(c) and (d). Frequency responses are comparable with that of Patra *et al.* [24]. A peak is observed in the magnitude response plots at *L–C* resonant frequency. Control transfer function dc gains for (V_1/D_1) is obtained as 23.8 dB and (V_2/D_2) is obtained as 22.6 dB which are matching with expected values. Cross coupled transfer function dc gains for (V_1/D_2) is obtained as 23.4 dB and (V_2/D_1) is obtained as 21.4 dB which are matching with expected values. Frequency responses of the proposed model is matching with that of the physical model. At higher frequencies, the frequency response of the proposed model

TABLE III
COMPUTATIONAL TIME AND STEADY-STATE ERROR FOR DIFFERENT MODELS

	Computation Time (in ms)		Steady State Error (in mV)	
	SISO	SIDO	SIDO	
			V_1	V_2
Physical Model	960000	3900000	0.2	0.2
State Space Model	205.3	998.8	0.15	0.15
Ripple Space Model	378.6	1037.5	20	16
Proposed Model	232.5	**382.2**	0.16	0.2

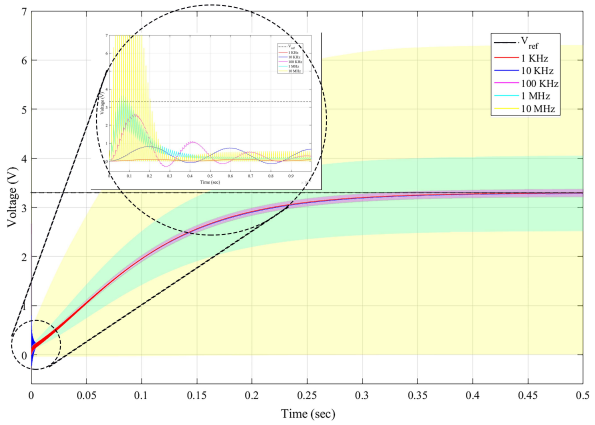

Fig. 18. Output voltage ripple with different corner frequencies of LPF.

tends to diverge from the physical model due to the extra poles introduced by the output LPF in the proposed model which is in agreement with the dynamic responses of the proposed model and the physical model.

The output LPF is an important component in the proposed model which filters any abrupt changes in output due to state switching. Fig. 18 shows the ripple behavior of output during different corner frequencies of the LPF. At corner frequency = 10 MHz, maximum ripple is observed. A similar behavior can be observed in the absence of LPF. The corner frequency of the LPF is decided in such a way that, it limits the state switching but it allows the transient behavior of the dc–dc converter model. An LPF with a higher cutoff frequency which is closer to the switching frequency of the dc–dc converter can be used to enable a faster transient response. In such a case, an LPF with a very sharp roll-off should to be used. This will enable fast transient response while mitigating switching noise at the expense of complexity of the LPF.

This article studied the effectiveness of the model in getting steady-state responses in comparison with the physical model as well as the experimental circuit. The frequency responses are obtained and compared with existing literature. The results of the proposed model are in good agreement with those of the physical model and experimental circuit. The computationally efficient proposed model can be easily extended to simulate multioutput dc–dc converters.

IV. CONCLUSION

The proposed modeling technique treats states separately and combines them by multiplexing. It is compared with the traditional SSA model and ripple space model. Both the traditional models require a high amount of time to design for multiple outputs, whereas the proposed methodology solves the bottleneck by considering states separately and adding them later with the help of a multiplexer. The main advantage of the proposed model is that it requires only 2×2 matrices for the design and computation of multiple output dc–dc converters, whereas other models of the same genre require $(n+1) \times (n+1)$ matrices. The state separate model has an inherent advantage of using multiplexed states of available single output models and converting them to a multioutput dc–dc converter model. Using the proposed methodology, it is easier to scale any available single output dc–dc converter models to multiple output dc–dc converter models. The scalability offered by the proposed model allows the designer to create a multioutput model in a fast and modular way.

ACKNOWLEDGMENT

The authors would like to thank the Department of Science and Technology, Government of India for supporting this work under the FIST scheme No. SR/FST/ET-I/2017/68 with the required computational facilities. The authors also would like to thank the Special Manpower Development Program for Chips to System Design (SMDP-C2SD) of the Government of India for the CAD tools and lab facilities.

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Nithin Thomas Abraham (Graduate Student Member, IEEE) received the B.Tech. degree in electronics and communication engineering from Government Engineering College Barton Hill, Thiruvananthapuram, India, in 2014, and the M.Tech. degree from the College of Engineering Chengannur, Chengannur, India, in 2016.

He worked as a Wireless Test Engineer with Broadcom, Bengaluru, India, in 2017. He currently working as a Research Scholar with the National Institute of Technology Calicut, Kozhikode, India. His research interests include power management IC design and low power VLSI circuits and systems.

Gajendranath Chowdary (Member, IEEE) received the B.E. degree from Osmania University, Hyderabad, India, in 2006, and the M.Tech. and Ph.D. degrees from the Indian Institute of Technology (IIT) Delhi, New Delhi, India, in 2008 and 2016, respectively.

He worked as an Analog Circuit Design Engineer with ST-Ericsson, Bengaluru, India, from 2008 to 2010 and with Aura Semiconductor, Bengaluru, India, in 2011, 2013, and 2016. Since April 2017, he has been with the Department of Electrical Engineering, IIT Hyderabad, Hyderabad. His research interests include ambient energy harvesting, high-speed analog and mixed-signal circuits, and power management circuit design for ultralow-power applications.

Dr. Chowdary was a recipient of the "Early Career Research Award" from the Science and Engineering Research Board, India.

Dhanaraj Kakkanattu Jagalchandran (Member, IEEE) received the B.Tech. degree in electronics and communication engineering and the M.Tech. degree in digital systems and communication engineering from the National Institute of Technology Calicut, Kozhikode, India, in 2003 and 2007, respectively, and the Ph.D. degree from the Indian Institute of Technology Delhi, New Delhi, India, in 2017.

He is currently working as an Assistant professor with the National Institute of Technology Calicut. His research interests include power management IC design, low power analog/digital IC design for neuromorphic and neural network chips, architectures for signal processing, and cryptographic systems.