A Fully Analog Autonomous QRS Complex Detection and Low-Complexity Asystole, Extreme Bradycardia, and Tachycardia Classification System

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***Abstract*— This article presents a power-efficient fully analog classifier architecture for the detection of critical cardiac abnormalities, i.e., asystole, extreme bradycardia, and tachycardia. To reduce power consumption and hardware complexity, an analog QRS complex detection circuit and arithmetic counter-based classification modules are introduced. The QRS detection circuit is autonomous and consumes an average current of 34 nA only, vis-à-vis state-of-the-art QRS detection designs that are digital signal processor (DSP) assisted and consume tens of microwatts of power. Furthermore, a heart-rate estimator provides the number of QRS complexes per minute. Each of the proposed modules is successfully validated through real electrocardiogram (ECG) test signals taken from the PhysioNet database. The proposed beat detector circuit exhibits a sensitivity of 97.85% and a positive prediction of 98.3%. Experimental results based on bedside monitor data show that the proposed classification module provides an overall sensitivity of 96.25% and a positive prediction of 96.97%. The complete classification architecture, implemented fully on analog platform, is simulated in the UMC 0.18-μm CMOS process and consumes 119-nW power with an active silicon area of 450 × 800 μm. Moreover, the low-power implementation makes it suitable for long-term battery-operated remote ECG monitoring systems.**

***Index Terms*— Analog signal processor (ASP), asystole, beats per minute (bpm), bradycardia, classification, digital signal processor (DSP), electrocardiogram (ECG), frequency-shift keying (FSK), instrumentation amplifier (IA), ON/OFF keying (OOK), operational transconductance amplifier (OTA), tachycardia.**

I. Introduction

ELECTROCARDIOGRAPHY has evolved as a wellspring of information for detection of numerous cardiac arrhythmia, besides person/mobile identification [1], [2]. Continuous electrocardiogram (ECG) monitoring is indispensable specially in the case of elderly, handicapped and people with recurring cardiac disorders. Furthermore, remote and rural healthcare services demand continuous ECG monitoring of the patient to support preventive and personalized services in real time for stationary patients, both in and out of the hospital. When augmented with an efficient alarm, such systems could alert the nearest emergency medical services and boost the safety of critically ill patients in real time, both in and out of hospitals. The detection of critical alarm types (i.e., asystole, extreme bradycardia and tachycardia, and ventricular tachycardia and fibrillation) is paramount in such a scenario [3], [4], [5].

Contemporary smart ECG monitoring systems, shown in Fig. 1(a), intended for remote healthcare applications consists of an efficient sensing, "analysis," and a wireless transmission platform [6], [7], [8]. The sensing/acquisition consists of a programmable gain amplifier (PGA), a bandpass filter, and an analog-to-digital converter (ADC), and is conventionally implemented on an analog platform. Primarily, "analysis" of the ECG signal includes filtering, feature extraction, and classification, and is conventionally implemented in the digital domain. The required operations are implemented through a digital signal processor (DSP) [9], [10], [11], [12], [13] on a system-on-chip (SoC) platform. Finally, a frequency-shift keying (FSK)/ON/OFF keying (OOK) transceiver is used for transmission of the processed data [14]. The key point in all the traditional implementations is that the "analysis" and transmission parts dominate the distribution of power consumption in the overall system [15].

However, DSP-based techniques are more computationally intensive and consume power in the order of tens or hundreds of microwatts, e.g., the systems in [9] and [10] report a power consumption of 345 and 31.1 μW, respectively. This makes them incompatible with devices requiring long life span and intended for continuous ECG monitoring. Therefore, the recently published works implement the functionality of feature extraction in analog domain [15], [16], [17], [18], rather than on a DSP. This enables a significant reduction of system-level power consumption by minimizing the computational burden on the DSP.

The three abnormalities targeted in this work, i.e., asystole, extreme bradycardia, and tachycardia, are critically significant with respect to patients in the ICU or patients with chronic cardiac disease residing in remote/rural areas. Both extreme bradycardia (heart rate lower than 40 beats per minute (bpm) for five consecutive beats) and extreme tachycardia (heart rate higher than 140 bpm for 17 consecutive beats) [19] occur as a consequence of reduced cardiac output. In the first case,

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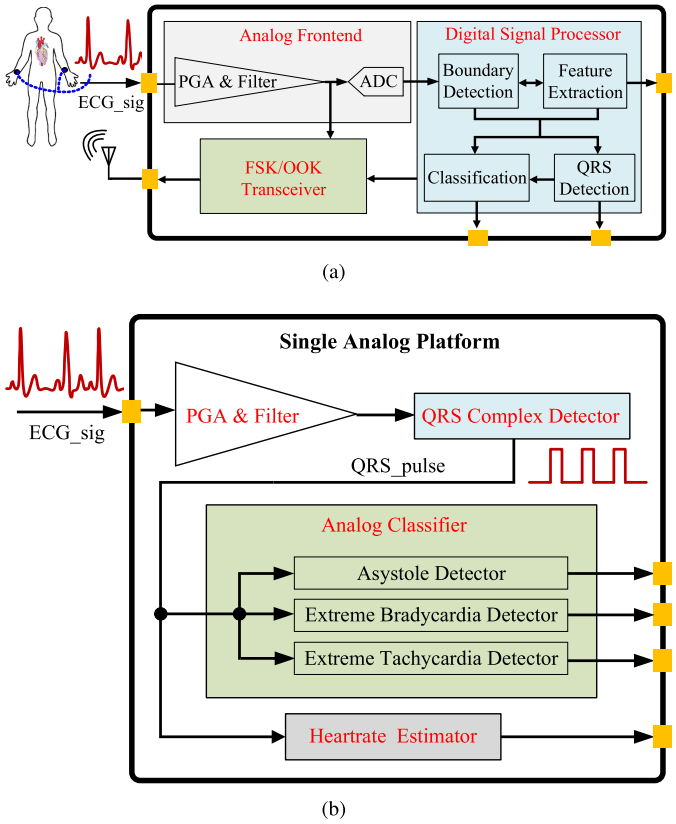

Fig. 1. (a) Block diagram of the conventional ECG recording system. (b) Block diagram of the proposed scheme.

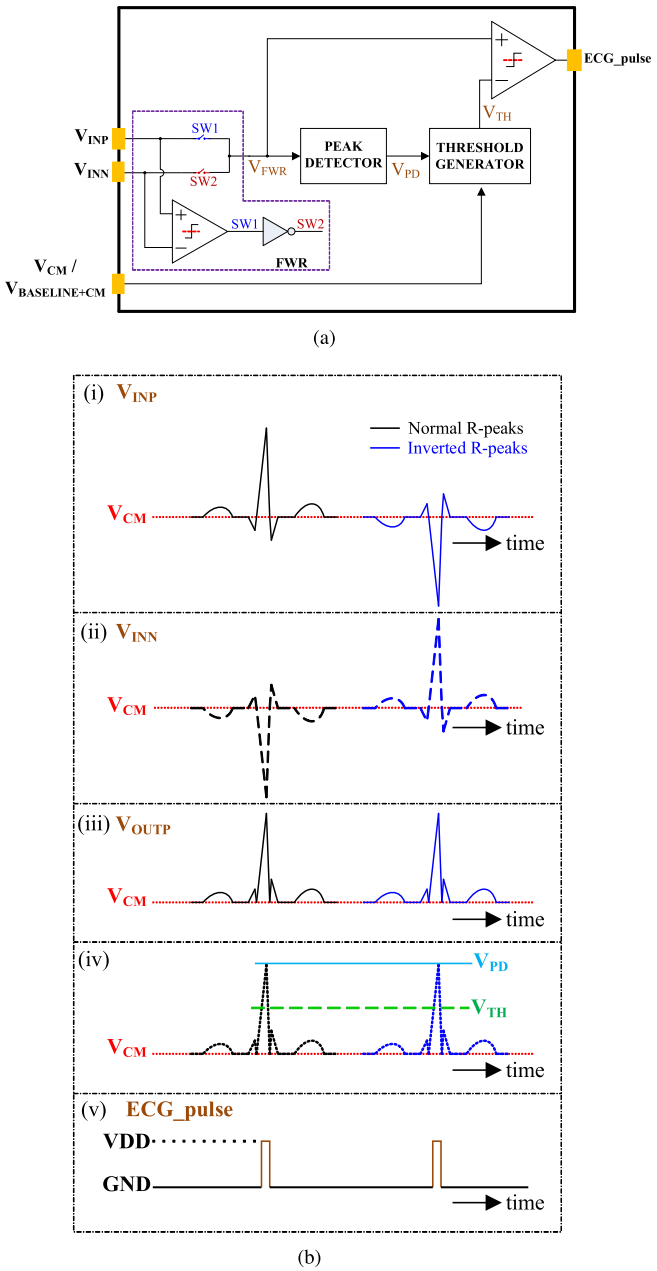

Fig. 2. (a) Schematic of the proposed QRS complex detector. (b) Waveforms explaining the working principle of the QRS complex detector.

the systolic output may not compensate for reduced bpm, and for the latter case, it is reduced by the reduced filling time that is proportionately larger than expulsion time. Moreover, ventricular dysrhythmia (fast rhythms from bottom chambers) is associated with high morbidity and mortality. Symptomatic bradycardia that is likely to progress to asystole is Class 1 indications for pacemakers, certainly needs treatment, and should receive pacemakers. Asystole means "no systole" or no pulse. It is the annihilation of cardiac output and represents the extreme of bradycardia. When the cardiac output is reduced drastically, say less than 3 L/min, then the brain and organ hypoperfusion occurs, which is not a survivable situation without treatment. If cardiac output stops, organs are damaged by ischemia, which becomes life-threatening in 2–4 min. When the heart beats very slowly (extreme bradycardia) or stops beating (asystole), it leaves no more than 2–4 min before irreversible brain damage, which occurs as the result of low cardiac output. Therefore, having an efficient alarming system is essential to prevent death [20], [21]. The significance of detecting these life-threatening arrhythmia is also summarized in [19], [22], and [23].

Motivated by the above discussion, this work presents a fully analog scheme comprising: 1) a low-power online QRS detection circuit using an autonomous dynamic threshold voltage, hence discarding the need of any external microcontroller/DSP and calibration, and 2) a power-efficient analog classifier for the detection of three of the critical alarm types, i.e., asystole, extreme bradycardia, and tachycardia [19]. In the event of detection of any one of the three target cardiac disorders, the system raises an immediate alarm. An important value addition to the acquisition systems such as [24] is that the proposed scheme intends to alert the proximate medical service agency in the case of remote monitoring and alert the hospital staff in the case of in-hospital patients.

The proposed modules are successfully validated through the test signals taken from the MIT-BIH arrhythmia database (MITDB) and [19], [25]. The proposed architecture targets only three alarm types (i.e., asystole, extreme bradycardia, and tachycardia), leaving the other two (ventricular tachycardia and flutter/fibrillation) mentioned in [19]. This can be attributed to the hardware complexity associated with the algorithms meant for the detection of the latter two. Since a full custom analog implementation of such a complex system

would turn out to be an arduous task, their implementation is preferred in the automated digital domain. Also, it is worth mentioning from a clinical application perspective that the prime purpose of this system is to classify and hence assist in the preliminary prognosis of the abovementioned abnormalities. A more accurate, detailed and unequivocal diagnosis of the patient's clinical condition is still assigned to the more computationally intensive and power-hungry DSP. Therefore, the proposed classification scheme presents a useful tradeoff between complexity, accuracy, and power consumption.

This article is organized as follows. Section II emphasizes on the background and motivation of the proposed work. Section III describes the architecture, design intricacies, and implementation of the proposed scheme. Section IV presents the results obtained. Finally, Section V concludes this article. It should be declared that in this article, some sections are reused verbatim from thesis [26] with permission.

II. Outline of Related Published Works

Detection of QRS complexes is the first step for any ECG classification scheme for cardiac rhythm (CR) and heart-rate variability (HRV) analysis. Essentially, the analog signal processors (ASPs) in [15], [16], [17], and [18] include an analog QRS feature extractor (FE), which is a power-efficient substitute for the predominantly employed computation-intensive continuous wavelet transform (CWT). The ASPs in these works assist the subsequent DSP for low-power signal analysis. Yazicioglu et al. [15] used two bandpass filters for extracting the quadrature components of the ECG signal fluctuations within a specified range of frequencies. The DSP calculates the band power by taking the sum-of-squares of the quadrature channels. The peaks in the band power correspond to QRS complexes in the ECG signal. The width of the bandpass filter is determined by the switched capacitor (SC) low-pass filter (LPF) because it offers a good tradeoff between area and noise performance. The center frequency (16 Hz) and bandwidth (4.6–7.8 Hz) of the bandpass filter are optimized over the MITDB to achieve the sensitivity (Se) of 98.8% and the positive predictivity (+P) of 99.8%. Kim et al. [16] and Yan et al. [17] and [18] also implemented a similar FE for R-peak detection, which utilizes an analog first-order bandpass filter with precise bandwidth control. The bandpass filter (10–15 Hz) comprises an SC high-pass filter followed by an SC LPF. The FE inputs to the DSP for band power ($\mathrm{PWR} = \mathrm{FE}^2$) calculation. The DSP runs a beat detection algorithm utilizing an adaptive threshold by taking a low-pass filtered value of the PWR signal to detect the R-peak. It achieves the Se of 96.67% and +P of 100%.

All the above application-specific integrated circuits (ASICs) employ an ADC followed by a DSP to detect the location of R-peak and hence detect heartbeat. As discussed earlier, this is a power-hungry approach. Hence, to remove the requirement of an ADC and signal processor, the topology in [27] proposes a comparator-based topology for heartbeat detection, thereby reducing the overall system complexity, power, and area. The ECG signal after preliminary amplification is fed to two subsequent amplifiers with equal gains, i.e., a QRS complex and baseline amplifier. While the QRS amplifier preserves the features of the QRS complex, the baseline amplifier captures the low-frequency baseline drift emanating from motion artifacts. The low-pass corner frequency of QRS complex and baseline amplifier is kept at 25 and 1 Hz, respectively. Then a positive inline dc offset is added to the output of the baseline amplifier to obtain an adaptive threshold voltage. A comparator generates a pulse whenever the output of the QRS amplifier exceeds the threshold voltage and marks the occurrence of a QRS complex in the ECG signal. The dc offset is controlled by an external microcontroller such that the period between the QRS pulses is regular and matches with that of human beings. The R-wave timing is estimated from the midpoint timing of the QRS pulses. Tested on normal chest ECG records from the MITDB totaling 2304 heartbeats, the technique in [27] estimates the location of R-peaks with a standard deviation of R-wave timing error of only 1.25 ms. In the case of irregular QRS complexes and rapid baseline wandering, the microcontroller reruns the calibration routine. If the recalibration fails after enough number of iterations, then this topology identifies it as a case of arrhythmia. However, this topology involves an external microcontroller, which consumes power in the order of microwatts, even while using the latest low-power modules. Moreover, multiple runs of the calibration routine will further worsen the power budget of the system.

III. Proposed Classifier Topology

The complete scheme is shown in Fig. 1(b). The blocks within the shaded region are the suggested additions to a standard continuous ECG acquisition system. This scheme includes a circuit that generates a pulse at every occurrence of QRS complex in the ECG signal and three low-complexity counter-based modules for the detection of each of the target cardiac disorders. The essence of the proposed architecture is implemented on a single analog platform along with the signal conditioning block. The criteria for detection of each of the target cardiac arrhythmia are adopted from [19]. The working principle of the overall system and each individual module is summarized in Algorithm 1. A detailed explanation of the formulation and working principle of each of the constituent blocks is given in the following.

A. QRS Complex Detector

The QRS detection module implemented in this work consists of a full-wave rectifier (FWR), a peak detector, a threshold voltage generator, and two comparators, as shown in Fig. 2(a). The working principle of the proposed scheme is shown in Fig. 2(b). Presuming that the ECG signal, after being appropriately amplified and filtered by a front-end such as that reported in [24], [26], [28], and [29], has a common-mode voltage and R-peak amplitude of 0.9 V and 100 mV approximately, respectively. Fig. 2(b) (top) shows the ECG signal with normal and inverted (due to some kind of arrhythmia or faulty lead connection) QRS complexes, V_{INP}, riding on an appropriate predefined dc common-mode voltage V_{CM} (or sum of baseline wandering signal and V_{CM}). Its differential

Algorithm 1 Detect Occurrence of Each QRS Complex and Thereby Detect Asystole, Extreme Bradycardia, and Extreme Tachycardia

Let A_detect, B_detect and T_detect be the alarms for asystole, extreme bradycardia and extreme tachycardia respectively

Input: Appropriately amplified and filtered ECG signal ECG_sig

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****** **QRS Complex Detector** ****************

****

Detect event of each R-peak

if R-peak is detected **then**

Generate a logic high pulse ECG_pulse

end if

****

****** **Analog Classifier** *********************

****

Input: ECG_pulse

****** Asystole Detector *******

if No ECG_pulse for at least 4 seconds **then**

$A\_detect \leftarrow logic\ high$

end if

****** Extreme Bradycardia Detector *************

if Heart rate < 40 bpm for 5 consecutive beats **then**

$B\_detect \leftarrow logic\ high$

end if

****** Extreme Tachycardia Detector *************

if Heart rate > 140 bpm for 17 consecutive beats **then**

$T\_detect \leftarrow logic\ high$

end if

****

****** **Heartrate Estimator** *****************

****

Count the number of ECG_pulse occurring in 1 minute i.e. bpm

****

Output: A_detect, B_detect, T_detect and bpm

counterpart is shown in Fig. 2(b) (second from top) and is labeled V_{INN}. An FWR configuration consists of a comparator and a pair of switches and generates V_{FWR}, as shown in Fig. 2(b) (third from top). The comparator compares V_{INP} with V_{INN} and forces SW1 to go high (low) whenever V_{INP} is greater (lower) than V_{INN}. SW2 is the inverted version of SW1. The signal V_{FWR} is toggled between V_{INP} and V_{INN}, using signals SW1 and SW2. This V_{FWR} is fed to a peak detector circuit, generating V_{PD}, as shown in Fig. 2(b) (fourth from top). The threshold generator circuit outputs a suitable voltage V_{TH}. Finally, a second comparator compares V_{FWR} with V_{TH} and forces ECG_pulse to go high (low) whenever V_{FWR} is greater (lower) than V_{TH}, as shown in Fig. 2(b) (bottom). It consumes an average current of 34 nA.

The proposed circuit works on the premise that the QRS complex (or heartbeat) has a higher amplitude compared to other ECG features and hence can be detected whenever the

TABLE I

DEIGN PARAMETERS OF THE TWO-STAGE OTA

Device	**W/L (μm/μm)**	**Device**	**W/L (μm/μm)**	**Device**	**W/L (μm/μm)**
M0a,b	1/2	M0c	0.5/0.47	M1a,M1b	1.5/1
M2a,M2b	0.5/0.5	M3	1.2/0.5	–	–

TABLE II

PERFORMANCE PARAMETERS OF THE TWO-STAGE OTA

Parameter	**Value**
Supply voltage	1.8 V
Current consumption	5 nA
Open loop DC gain	72 dB
UGB for C_L = 1 pF	145 KHz

voltage of the ECG signal is greater than a suitable threshold value. Furthermore, the signal path is expected to introduce circuit-related delay. However, this delay is not a critical issue here because the input ECG is a low bandwidth (or slow) signal and the unity gain bandwidth (UGB) of the loop gain of the feedback configuration within the peak detector is kept very high compared to the input signal's bandwidth. Moreover, this argument is vindicated by the results obtained after the proposed method is tested for multiple ECG records from [19] and MITDB.

The circuit corresponding to each of the blocks in the scheme mentioned above, along with important design aspects of the same, is discussed in the following.

1) Comparator: The block diagram of the comparator is shown in Fig. 3(a). It includes a two-stage operational transconductance amplifier (OTA), a Schmitt trigger, and an inverter-based buffer. While the OTA amplifies the differential input, the Schmitt trigger ensures no unwanted transition of the comparator's output due to OTA offset and spurious glitches. The schematic of the two-stage OTA is shown in Fig. 3(b). While evaluating the noise contribution of each of the constituent transistors in the OTA, the g_m/I_D [30] technique is utilized for sizing the transistors to optimize power consumption and noise. Moreover, the input transistors are operated in moderate inversion to reduce flicker noise. The device dimensions are given in Table I. The performance of this OTA is summarized in Table II.

2) Peak Detector: The peak detector is a negative feedback system, which is responsible for capturing the peak amplitude of V_{FWR} in Fig. 3(c) [31]. The peak detector circuit, shown in Fig. 3(b), consists of an amplifier with high open-loop dc gain [shown in Fig. 3(b)], a current source (M1), current steering transistors (comprising of M2 and M3), and load capacitance C_{LOAD}. When voltage at node VOUT is lesser than the input VIN, the amplifier generates a logical *high* (=1.8 V here) output $V1$ such that the current from M1 is steered to the capacitors via M3. The capacitors continue to get charged until the voltage at node VOUT is just greater than the VIN. Then, the amplifier outputs a logical low (=0 V here) voltage so that the current from M1 is steered to ground via M2, while the capacitors hold the voltage across them. The amplifier is responsible for producing a voltage $V1$ such that the voltage at node VOUT always tracks the input VIN.

The noise contribution of the peak detector is analyzed considering the individual contributions from different noise

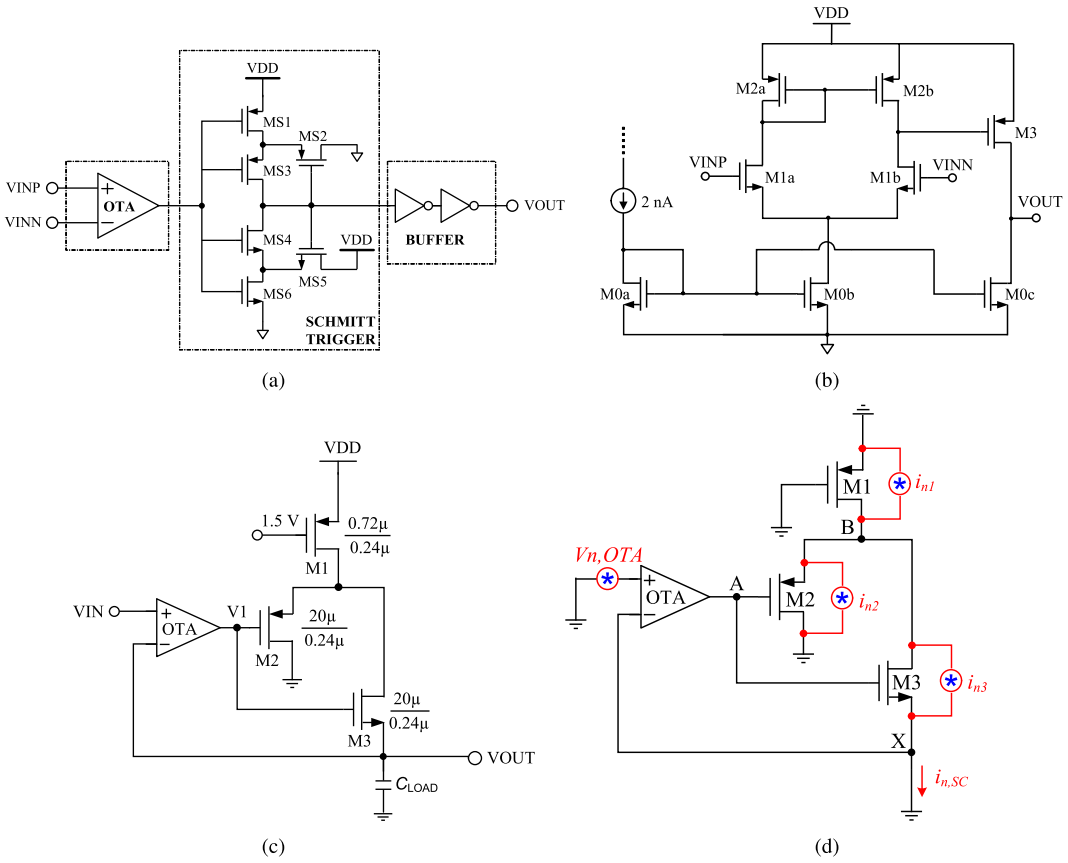


Fig. 3. Circuit diagram of various blocks constituting the QRS detector. (a) Comparator. (b) Two-stage OTA. (c) Peak detector. (d) Noise analysis of the peak detector.

sources (i.e., $V_{n,\mathrm{OTA}}$, i_{n1}, i_{n2}, and i_{n3}), as shown in Fig. 3(d). The total short-circuit noise current, $i_{n,\mathrm{SC}}$, is calculated using superposition of individual short-circuit noise currents and is expressed as

$$i_{n,\mathrm{SC}} = i_{n\mathrm{OTA,SC}} + i_{n1,\mathrm{SC}} + i_{n2,\mathrm{SC}} + i_{n3,\mathrm{SC}}. \tag{1}$$

For the rest of the analysis g_{mi}, r_{0i}, and g_{0i} $(=(1/r_{0i}))$ represent the transconductance, output resistance, and conductance of corresponding transistor Mi, respectively. The short-circuit noise current due to the OTA is given by

$$\begin{aligned} i_{n\mathrm{OTA,SC}} &= A * v_{n,\mathrm{OTA}} * \left(g_{m3} + \frac{1}{r_{03}}\right) \\ &\approx A * v_{n,\mathrm{OTA}} * g_{m3} \end{aligned} \tag{2}$$

where A is the gain of the OTA and $g_{m3} * r_{03} \gg 1$. The short-circuit noise current due to M1 is given by

$$i_{n1,\mathrm{SC}} = i_{n1} * \left(\frac{g_{03}}{g_{03} + g_{01} + g_{m2}}\right). \tag{3}$$

The short-circuit noise current due to M2 is given by

$$i_{n2,\mathrm{SC}} = i_{n2} * \left(\frac{g_{03}}{g_{03} + g_{01} + g_{02} + g_{m2}}\right). \tag{4}$$

The short-circuit noise current due to M3 is given by

$$i_{n3,\mathrm{SC}} = i_{n3} * \left(\frac{g_{03}}{g_{03} + g_{01} + g_{m2}}\right). \tag{5}$$

The Thevenin-equivalent resistance looking into the node X can be represented by

$$R_{\mathrm{out}} = \frac{1}{(1+A) * g_{m3}} \approx \frac{1}{A * g_{m3}}. \tag{6}$$

The rms noise voltage at node X, $V_{X,n}$, is generated by $i_{n,\mathrm{SC}}$ flowing through R_{out} and is expressed as

$$\overline{V_{X,n}^2}\Big|_{i_{n,\mathrm{SC}}} = \overline{i_{n,\mathrm{SC}}^2} * R_{\mathrm{out}}^2. \tag{7}$$

The above equations show that the net noise voltage at the peak detector's output is negligible and does not affect the detection of QRS complexes.

The value of capacitor C_{LOAD} ($C = 10$ μF here) is optimized after evaluation of the performance metrics, i.e., sensitivity and accuracy of the heartbeat detection scheme and classifier. Also, the peak detector is designed such that its total discharge time is higher than the time duration between two R-peaks. Hence, the discharge time is kept greater than 1 s to prevent the digital control logic from varying the gain during low amplitude peaks (P, Q, and T) of the ECG signal.

3) Threshold Generator: The threshold voltage generator circuit, shown in Fig. 4, generates the average of the two input voltages without loading the inputs. A simple current mirror with local negative feedback-based averaging circuit is proposed here. The two input voltages, $V1$ and $V2$, are fed to the gate of M3 and M18, respectively. The body/bulk of the input transistors are locally shorted to their sources

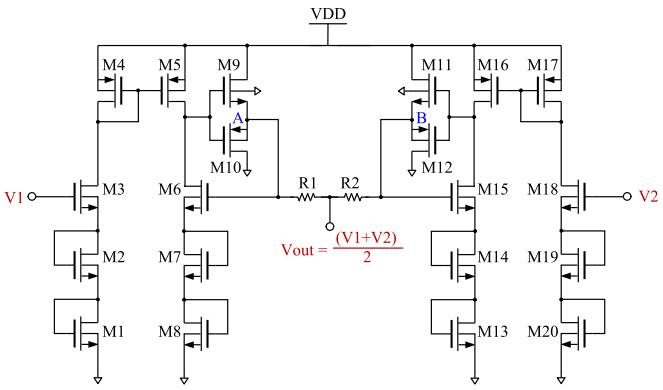


Fig. 4. Circuit of the threshold generator.

TABLE III
DEIGN PARAMETERS OF THE THRESHOLD GENERATOR CIRCUIT

Device	W/L (μm/μm)
M1,2,3,6,7,8,13,14,15,18,19,20	0.24/50
M4,5,16,17	2/50
M9,10,11,12	50/0.18
Resistance	**Value** (Ω)
R1,2	5M

using a deep n-well (DNW) process. Since M2 and M3 carry the same current as M3, they would develop equal V_{GS} $(=(V1/3))$ voltages, neglecting the effect of channel-length modulation. The current flowing through M1–M3 is mirrored to M6–M8 using M4 and M5, so as to obtain $V1$ at the gate of M6. If $V1 > V2$ $(V1 < V2)$, a current equal to $((V1 - V2)/(R1 + R2))$ $((V2 - V1)/(R1 + R2))$ follows the path VDD-M9-R1-R2-M12-ground (VDD-M11-R2-R1-M10-ground), with M9 (M11) and M12 (M10) acting as a current source and sink, respectively. Moreover, the push–pull configuration consisting of M9 and M10 (M11 and M12) forms a negative feedback loop around M6 (M15). The average of the two input voltages is obtained by using two identical resistors $R1$ and $R2$ such that V_{TH} is equal to $((V1 + V2)/2)$.

The aspect ratios of the devices and values of components used for designing this circuit are given in Table III. While the length of the nMOS devices (except for the source follower stages) is kept equal to 20 μm to suppress the effect of channel-length modulation and ensure better matching, the width of all these devices is kept minimum (to ensure low current consumption). However, for source follower stages, a length is set to the minimum value and a width is increased to 50 μm to drive the load current. It is important to mention here that the current flowing in $R1$ and $R2$ is proportional to $V1 - V2$ ($\approx$100 mV for the application considered here). Comparing this to the conventional low-dropout regulator (LDO)-based approach, current flowing in the resistances would be proportional to $((V1)/R1)$ (or $((V2)/R2)$). Since $V1 \approx 1$ V and $V2 \approx 0.9$ V, the LDO-based approach would involve higher resistances (more area cost) for low-power implementation. The design of this structure is also simple since it involves elementary mirroring concepts.

A threshold value of half of the R-peak amplitude is chosen here keeping a safe enough margin over the P- and T-peak excursions. Andresen [32] utilized a threshold value of 40% of the peak value of R-wave for detection. Similarly, variable

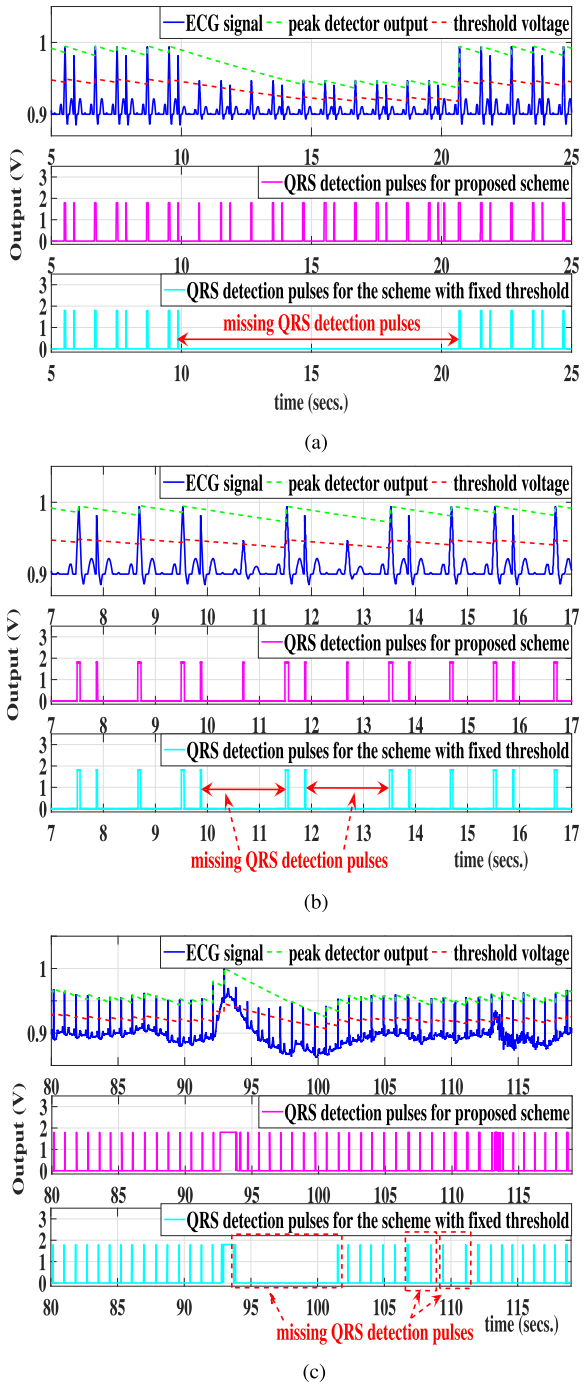


Fig. 5. Comparison between the proposed QRS complex detection circuit and the scheme with fixed threshold voltage (=0.95 V here) using the output pulses for different types of ECG signals. (a) Input with lower amplitude QRS complexes for some duration of time. (b) Input with intermittent variation in the amplitude QRS complexes for short duration of time. (c) Input with baseline wandering.

detection threshold voltages are employed in [33] and [34]. The inputs of this circuit are V_{PD} and V_{CM} from Fig. 2(a). Moreover, if the V_{CM} input is replaced with the sum of baseline wandering component of the ECG signal and V_{CM}, the proposed R-wave detection scheme can also handle ECG signals with large baseline wandering. A scheme to extract the baseline signal is reported in [27].

The QRS complex detection module operates more accurately compared to the scheme with a fixed threshold voltage when the input ECG signal has varying QRS complex amplitudes and rapid baseline wandering. Fig. 5 shows the comparison between the output QRS detecting pulses produced by the proffered QRS complex detection circuit (in magenta color) and the scheme with fixed threshold voltage (in cyan color). The figures also display the output of the peak detector (in green color) and the dynamic threshold voltage (in red color) fed to the comparator to detect the QRS complexes. As shown in Fig. 5(a)–(c), the scheme with a constant threshold voltage fails to detect some of the QRS complexes, while the circuit presented here successfully detects all of them. Moreover, the input ECG signal may suffer baseline wandering even if a baseline wander filter with a fixed cutoff frequency is used in the front end. This is because the spectral content of the baseline wander (typically 0.05–1 Hz) varies significantly, especially considering motion artifacts. Hence, this module was tested for ECG signals with baseline wandering from MITDB. Fig. 5(c) shows the results for record #101 from MITDB. It also shows that the suggested circuit detects QRS complexes with more accuracy compared to the one with fixed threshold voltage since the latter exhibits some missing QRS complex pulses. Furthermore, when the technique in [27] fails to detect QRS complexes with one threshold voltage, it needs to rerun the calibration routine. In the case where the amplitudes of QRS complexes frequently vary significantly, e.g., exercise-induced variations, it might wrongly identify the input ECG signal as arrhythmia. On the contrary, the QRS detection circuit presented here operates autonomously and uses a dynamically adjustable threshold voltage, thereby avoiding such a situation.

This QRS complex detection circuit offers the following improvements over that in [27]: 1) it does not involve a microcontroller; 2) it does not need to be calibrated and hence completely automatic and power-efficient; 3) since the threshold value for comparison is derived from the R-peaks itself, this topology works fine for ECG signals with varying amplitudes and rapid baseline; and 4) the proposed circuit is compatible with the scheme of recovering the ECG R-wave timing from the QRS detection pulses mentioned in [27].

B. Proposed Classification Modules

The proposed classification scheme comprises three individual modules for the detection of asystole, bradycardia, and tachycardia. The working principles of each of these modules are discussed in the following.

1) Asystole Detector: The absence of any QRS complex for at least 4 s is considered as the criterion for detection of asystole [19]. A counter-based technique is applied to identify any event of asystole and raise an alarm [Fig. 6(a)]. Operating at a clock frequency of 10 Hz, a 6-bit counter increments its count by one whenever it encounters a positive edge of the clock. While upcounting, the counter is reset at the instant of arrival of an ECG pulse. If the counter reaches a count of 40 (10 cycles/s $\times$ 4 s) or $(101000)_2$, without getting reset, $A_$detect goes high indicating the occurrence of asystole.

2) Extreme Bradycardia Detector: Heart rate lower than 40 bpm for five consecutive beats is considered as the criterion for identification of extreme bradycardia [19]. The proposed technique estimates the time duration for every five consecutive ECG pulses. A time duration greater than 7.5 s ({60 s/40 beats} $\times$ 5 beats) for any quintuple indicates the above abnormality.

A simplified illustration to explain the working principle of the proposed technique to detect bradycardia is shown in Fig. 6(b). To understand the scheme, let us assume P1, P2, P3, and so on to be the first, second, third, and so on, and ECG pulses generated by the QRS generation circuit.

Also, consider T_1 to be the time interval between any two consecutive positive edges of ECG_pulse signal, T_2 be the time interval between the next two consecutive positive edges, and so on. Then, a clock of higher frequency (30 Hz here) is used to estimate the duration between any two consecutive ECG pulses. Again, consider N_1 to be the count of the number of higher frequency pulses within T_1, N_2 to be the count of the number of higher frequency pulses within T_2, and so on. The aim is to have a count of number of clock pulses for a period of $(T_1 + T_2 + T_3 + T_4 + T_5)$, $(T_2 + T_3 + T_4 + T_5 + T_6)$, and so on. The count of higher frequency pulses for each interval is then added to find SUM_1 $(=N_1 + N_2 + N_3 + N_4 + N_5)$, SUM_2 $(=N_2 + N_3 + N_4 + N_5 + N_6)$, and so on as shown in the diagram. Finally, each of the sums is fed to a comparator, which produces high output when any of these sums is greater than a fixed value. Here, this fixed value is 225 (30 cycles/s $\times$ 7.5 s) or $(11100001)_2$. The transition of the comparator's output from low to high signals the detection of bradycardia.

Next, to have a count of clock pulses within a duration of T_1, an enable signal en1 is derived, which is high for a duration T_1. After T_1, this enable signal should go low so that the count at the end of T_1 can be registered. Then, since the count corresponding to period T_2 is also required, another enable signal en2 should go high for T_2. Thus, to obtain a count corresponding to each interval between heartbeats, en1 and en2 need to work in tandem. This is shown in Fig. 6(c). Two counters are employed to do the required counting. The first and second counters work when en1 and en2 are high, respectively. Also, the first and second counters get reset when en1 and en2 go low, respectively. Moreover, since the second counter should start counting when the first counter stops counting, two counters are imperative here.

Furthermore, it is required to store each of the counts N_1, N_2, and so on using five registers and sum each quintuple of counts. The sequence of values stored in each register with respect to each ECG pulse is shown in Table IV. To find the sum of each quintuple of values as shown in Fig. 6(b), the counts should be stored in the given sequence. Each new value that is stored and the corresponding register are shown in the same color. A state machine (State Machine 1 in Table IV) is required to store each value to the corresponding register in the given sequence. The sequence of transitions of this state machine is shown in Fig. 6(d). Moreover, the color of the output of this state machine and the register into which the new count is to be stored is kept in the same color in Table IV to

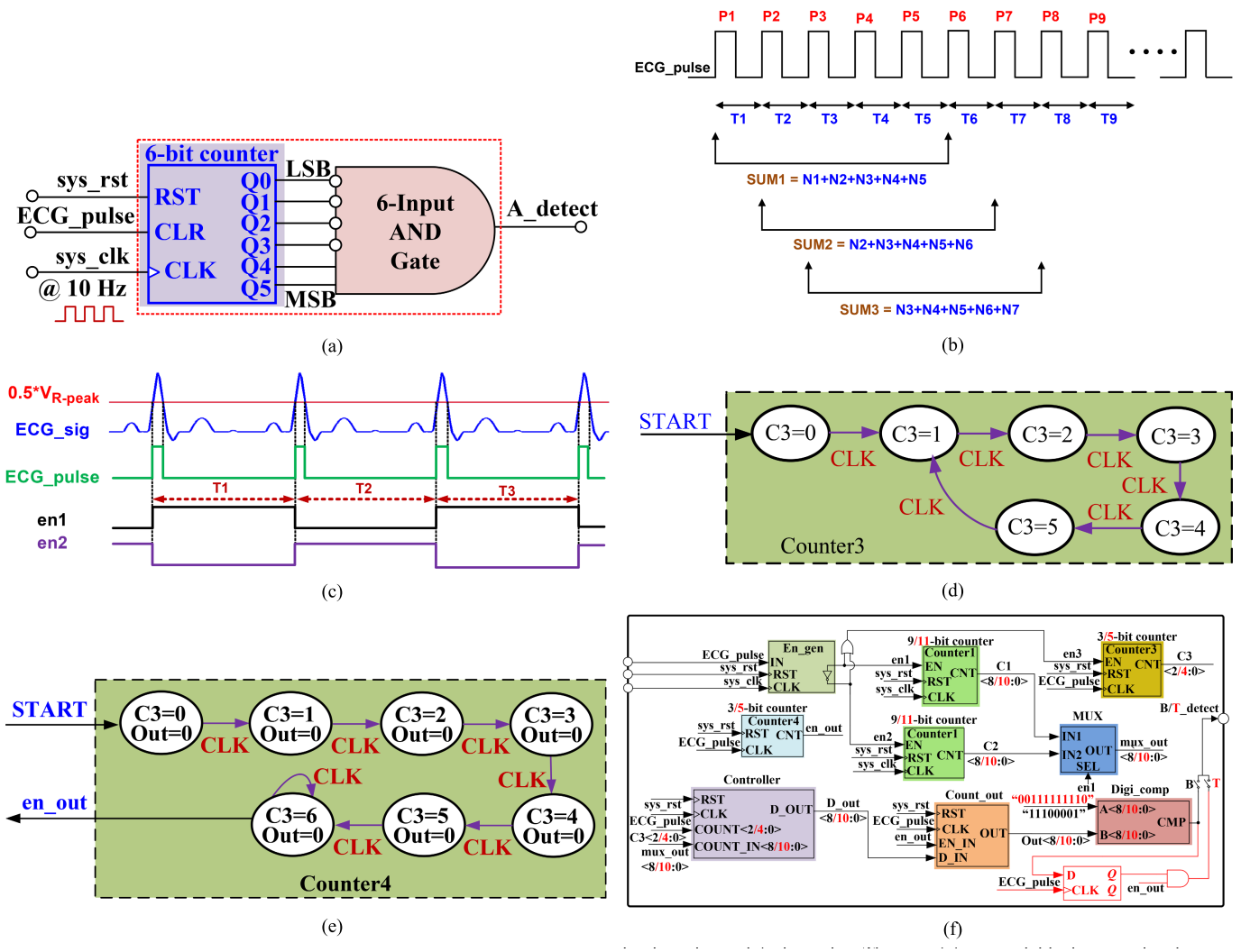


Fig. 6. Digital blocks of the proposed classifier. (a) Scheme for the detection of asystole. (b) Working principle for the detection of extreme bradycardia. (c) Generation of en1 and en2 from ECG_pulse. (d) Sequence of transitions for Counter3. (e) Sequence of transitions for Counter4. (f) Combined block diagram of the modules for the detection of extreme bradycardia and tachycardia. The annotations and blocks in red color are applicable only for the module pertaining to tachycardia.

TABLE IV

SEQUENCE FOR DATA STORAGE IN THE REGISTERS TRANSITION OF STATE MACHINES EMPLOYED WITH RESPECT TO ECG PULSES

ECG_pulse #	RST	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11
Register 1	0	N1	N1	N1	N1	N1	N6	N6	N6	N6	N6	N11
Register 2	0	0	N2	N2	N2	N2	N2	N7	N7	N7	N7	N7
Register 3	0	0	0	N3	N3	N3	N3	N3	N8	N8	N8	N8
Register 4	0	0	0	0	N4	N4	N4	N4	N4	N9	N9	N9
Register 5	0	0	0	0	0	N5	N5	N5	N5	N5	N10	N10
State Machine 1 (Counter3)	0	1	2	3	4	5	1	2	3	4	5	1
State Machine 2 (Counter4)	0	1	2	3	4	5	6	6	6	6	6	6
Data_Ready_for_Comparison Flag	0	0	0	0	0	0	1	1	1	1	1	1

make the understanding of the operating principle easier. The duration for initial few ECG pulses is also worth noticing. It is essential to wait for enough number of ECG pulses before each register has valid data and their sum is sent to the comparator. As shown in Table IV, a valid sum has to be sent to the comparator only after the first five ECG pulses. A second state machine (State Machine 2 in Table IV) is used to implement the same and puts a flag (Data_Ready_for_Comparison) high after five ECG pulses. The sequence of transitions of this state machine is shown in Fig. 6(e).

The circuit implementation of the scheme discussed above is illustrated through a block diagram in Fig. 6(f). The block labeled en_gen generates two mutually complimentary signals, en1 and en2. Operating on a clock at 30 Hz, Counter1 and Counter2, working in relay, count the number of clock cycles within the duration for which en1 and en2 are high, respectively. The two state machines of Fig. 6(d) and (e) are implemented using two counters Counter3 and Counter4, respectively. The controller is responsible for storing the counts generated by Counter1

TABLE V
PERFORMANCE OF THE QRS COMPLEX DETECTOR AND THE CLASSIFICATION MODULES

	Total Beat	FN	FP	Se(%)	+P(%)
QRS complex	109960	2416	1903	97.85	98.30
Asystole	50667	1598	1475	96.94	97.17
Bradycardia	33066	991	709	97.09	97.90
Tachycardia	85578	4013	3099	95.52	96.51
Total	169311	6602	5283	96.25	96.97

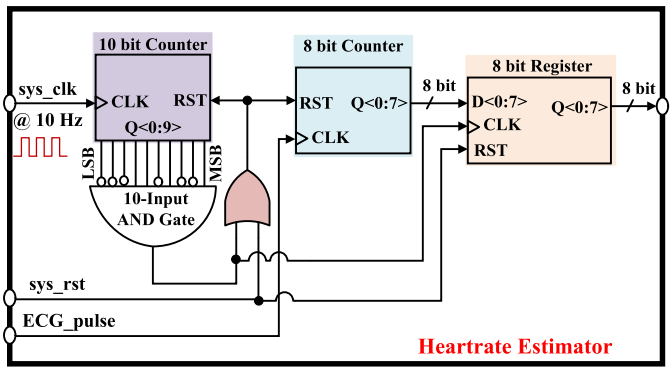


Fig. 7. Heart-rate estimator.

and Counter2, $C1$ and $C2$, in corresponding registers in the sequence explained in Table IV and generating the sum of every quintet of registers' content. The block labeled Count_out acts as a gate and allows the sum of counts to be fed to the comparator only after the output of Counter4, en_out, becomes high. Digi_comp is a comparator, which makes B_detect go high if the output of Count_out is greater than $(225)_{10}$.

The proposed architectures for the detection of extreme bradycardia and tachycardia are very similar to each other, and hence, their diagrams have been clubbed together in Fig. 6(f).

3) Extreme Tachycardia Detector: A heart rate higher than 140 bpm for 17 consecutive beats is considered as the criteria for identification of extreme tachycardia [19]. This technique differs from that for bradycardia only in terms of the word length of the counters and decisive count values. Note that unlike bradycardia, the output of Count_out needs to be lower than a fixed value. Hence, some extra circuitry is required to wait until en_out is high and a valid comparison can be done by Digi_comp.

C. Heart-Rate Estimator

This module provides an estimate of bpm or heart rate. Its operating principle is shown in Fig. 7. Operating with a clock at 10 Hz, a 10-bit counter (10 Hz $\times$ 60 s $=$ 600 cycles or $(1001011000)_2$) gets reset after a duration of every 1 min. Another 8-bit counter counts the number of ECG pulses as long as count from the 10-bit counter is nonzero. This system outputs a valid count whenever the output of the 10-bit counter completes a count of $(600)_{10}$. This module consumes 40 nW of power.

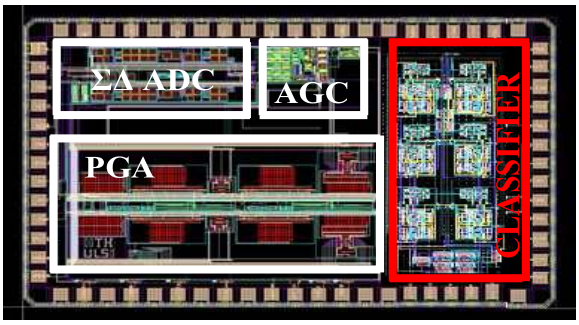


Fig. 8. Layout of the ECG front-end chip including the proposed classification topology.

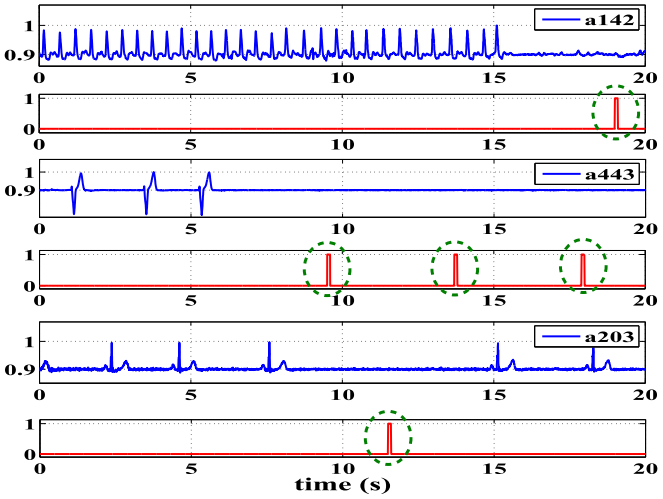
IV. RESULTS AND DISCUSSION

The complete architecture consumes an area of 450 $\times$ 800 μm in 0.18-μm CMOS. The layout of the proposed topology, as shown in Fig. 8, is included with the full system ECG front end. The results reported here are obtained through postextracted simulations in Cadence Virtuoso. Furthermore, the proposed QRS complex detection scheme is evaluated against the recordings of the MITDB. Furthermore, the proposed analog classification modules (for asystole, bradycardia, and tachycardia) are validated using various bedside monitor data of life-threatening arrhythmia alarms in the training set provided at the "PhysioNet/CinC Challenge 2015" database [19]. The performance parameters, i.e., sensitivity (Se) and positive prediction (+P), are summarized in Table V [35]. The obtained performance parameters prove that the possibility of failure is within tolerable limits for the application targeted [36], [37], [38], [39].

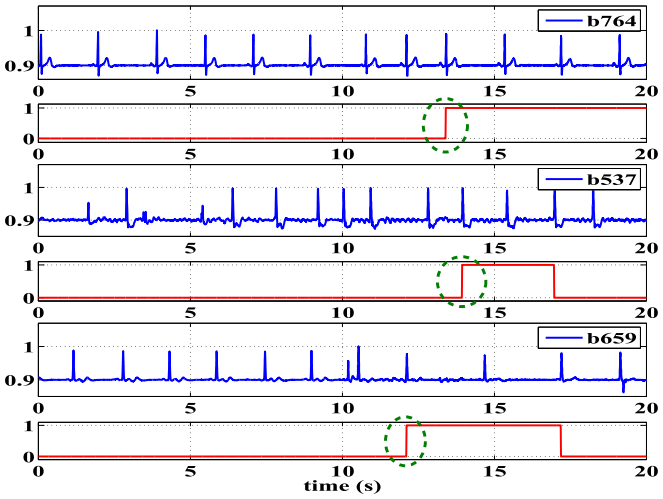
As already shown in Fig. 5, the proposed QRS detection circuit performs more accurately compared to the technique using a fixed threshold voltage. The output waveforms for few test signals for true cases of asystole (i.e., "a142l," "a443l," and "a203l"), bradycardia (i.e., "b764l," "b537l," and "b659l"), and tachycardia (i.e., "t430l," "t156l," and "t249l") are shown in Fig. 9(a)–(c), respectively. Note that the motive of these waveforms is solely to verify the functionality of the logic employed to detect the abnormalities, and the absolute value of the amplitude of the input ECG and logical output of the classifier is inconsequential. Hence, putting any label on the y-axis is skipped here, although all the amplitudes are voltages. The test signals and output of the corresponding abnormality detection circuits are represented in blue and red, respectively. The waveforms show that the proposed scheme successfully detects the three target abnormalities.

Furthermore, this technique detects the QRS complexes while consuming only 34-nA average current, which is significantly lesser than the state-of-the-art DSP schemes with power consumption of tens of microwatts or more. Within the classifier, the asystole, bradycardia, and tachycardia modules consume 12, 32, and 35 nW, respectively. Furthermore, this work can be considered as a proof-of-concept and the power consumption can be further reduced by designing the required gates using the current starving technique, lower supply voltage, and so on.

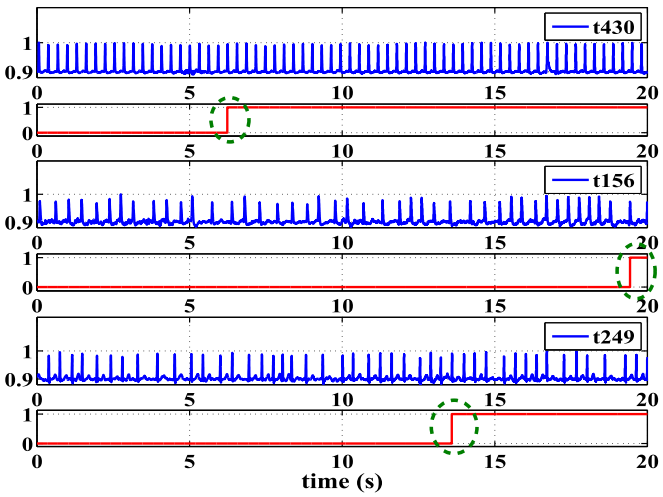
To prove the proposed concept, the architecture was verified in the prototype mode (Fig. 10). It comprises an mbed NXP



(a)



(b)



(c)

Fig. 9. Output waveforms of the classifier for each of the target fatal cardiac disorders for different signals taken from [19]. (a) Asystole. (b) Extreme bradycardia. (c) Extreme tachycardia.

LPC1768 board, a discrete board (with a peak detector built using IC 741 and resistors and capacitors, a buffer, a resistive voltage divider, and a comparator), and a field-programmable gate array (FPGA) board. The verification of the topology is

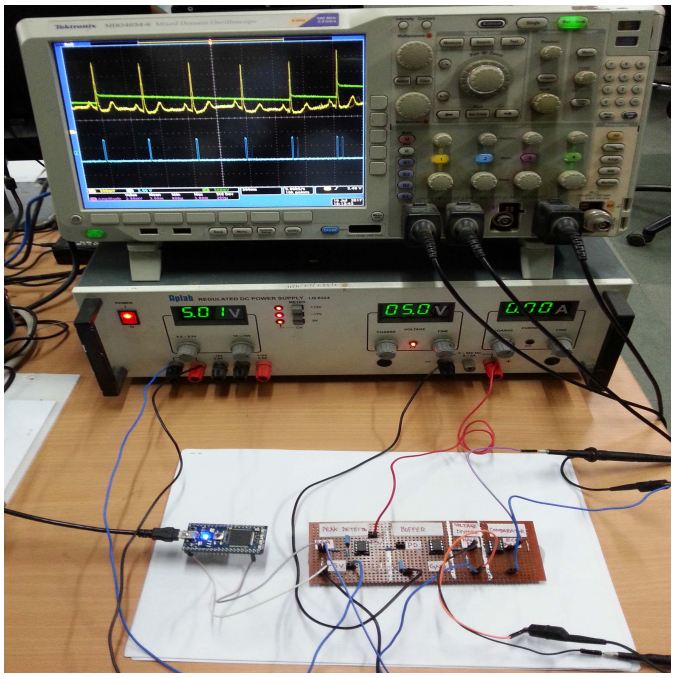


Fig. 10. Verification setup for testing the prototype QRS detector.

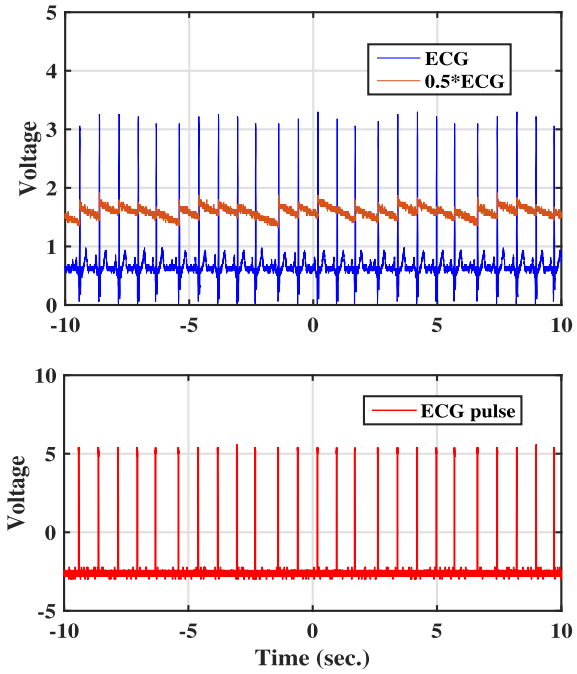


Fig. 11. Verification of the QRS detection scheme through a prototype built using discrete components with regular ECG signal as input.

done using the following steps: 1) input to the peak detector is given through the digital-to-analog converter (DAC) output pin of the mbed board; 2) a peak detector and pulse generation circuit built using discrete components detects the occurrence of an R-peak by generating a high pulse; 3) the pulses generated by the prototype are stored and fed to an FPGA; and 4) the algorithms to detect asystole, extreme bradycardia, and tachycardia are verified using the FPGA. As shown in Fig. 11, the output waveforms match those obtained through simulations in Cadence Virtuoso.

TABLE VI
PERFORMANCE COMPARISON WITH OTHER HARDWARE IMPLEMENTED ECG CLASSIFICATION SCHEMES

Ref.	Technology	V_{supply}	Power	Classification Algorithm	Performance	Type
[7]	0.065 µm CMOS	0.4 V (DSP)	45 nW(FDM) 92 nW(R-R) @ 10 kHz	Frequency Domain Metric (FDM) R-R algorithm	NA	SoC
[35]	0.13 µm CMOS	1.2 V	0.447 µW	Level-crossing sampling	BD: sensitivity→ 98.89%	ASIC
[40]	–	–	–	QRS complex → Embedded Algorithm	Se(%)→99.76%(PRDB), 99.74%(NSRDB) +P(%)→99.71%(PRDB), 99.93%(NSRDB)	–
[41]	–	–	–	Discrete orthogonal stockwell transform SVM for CL	Se(%)→98.82% +P(%)→98.82%	–
[42]	0.13 µm CMOS	1.2 V	43.7 nJ	Discrete wavelet transform (DWT)	CL : ^{a}TPR→0.93; ^{b}TNR→0.89	ASIC
[43]	0.18 µm CMOS	1.2 V	6 µW	4^{th}-order Haar wavelet-based DWT	BD : accuracy→99.44% CL : accuracy→97.25%	SoC
[44]	0.065 µm CMOS	0.7 V	0.11 mJ @ 7 kHz	Wavelet transform	BD: sensitivity →99.72% BD: positive prediction→99.49%	ASIC
[45]	0.065 µm CMOS	1 V	2.78 µW @ 10 kHz	QRS complex → ^{c}PAT Ventricular arrhythmia → naive Bayes	CL : accuracy→86%	ASIC
[46]	0.18 µm CMOS	–	2.21 µW @ 0.5 kHz	QRS complex → ^{c}PAT	Se(%)→95.65% +P(%)→99.36%	ASIC
[47]	0.18 µm CMOS	1.8 V	71 nW	Analog QRS complex → ^{c}PAT	Se(%)→99.24%, +P(%)→99.38%	ASIC
[48]	0.065 µm CMOS	1 V	1.2 nW	Analog QRS complex → ^{c}PAT	Se(%)→99.63%, +P(%)→99.47%	ASIC
This work	0.18 µm CMOS	1.8 V	34 nA 119 nW	Analog QRS complex detection circuit Arithmetic counter based classification module	BD : Se →97.85%, +P →98.30% Asystole : Se →96.94%, +P →97.17% Bradycardia : Se →97.09%, +P →97.90% Tachycardia : Se →95.52%, +P →96.51%	ASIC

^{a}True positive rate, ^{b}True negative rate, ^{c}Pan and Tompkins algorithm, Beat detection → BD, Classification → CL, Pacemaker Rhythm Database → PRDB, Normal Sinus Rhythm Database → NSRDB, Support Vector Machine → SVM

Table VI compares the performances of few relevant state-of-the-art hardware implementations of the ECG classification schemes. Although the proposed topology lags behind in terms of accuracy vis-à-vis others, a stringent comparison would be unfair due to their implementation using different technology nodes, supply voltages, power dissipation, usage of DSP, and most importantly the complexity of the algorithm involved. In a nutshell, the proposed classification scheme for the detection of fatal ECG abnormalities scores overs others as a viable solution with the following traits integrated together: 1) fully analog implementation; 2) reasonably accurate QRS complex detection; 3) low power dissipation; and 4) clinically acceptable accuracy of the classification algorithm. All the above features make the proposed classification scheme suitable for portable long-term monitoring systems intended for preliminary diagnosis of fatal ECG disorders. Morshedlou et al. [47] and Gungor et al. [48] implemented analog circuit for QRS detection, and it is relevant here to compare them vis-a-vis the proposed topology for the same purpose using the following points.

1) The power consumption of the circuit for QRS detection in [47] is 71 nA, whereas in the proposed scheme, the power consumption of the circuit responsible for R-peak detection is 34 nA only. Although Gungor et al. [48] reported a power consumption of 1.2 nW, it is important to note that work [48] is implemented in 65-nm TSMS CMOS technology with a 1-V supply, whereas the proposed circuit is implemented in 180-nm UMC CMOS technology with a 1.8-V supply.
2) The QRS detection scheme utilized in [47] consists of a number of modules, i.e., differentiator, current rectifier, current squaring, three LPFs, a pair of inverters, a level shifter, and a 5-bit binary counter. Similarly, work [48] consists of a bandpass filter, differentiator, squaring, moving window integrator, and comparator. In comparison, the proposed scheme comprises a much simpler (in terms of implementation and analysis) topology consisting of a peak detector, a threshold voltage generator, and a comparator.
3) An input amplitude of 300 mV_{pp} and an amplitude between 200 and 300 mV_{pp} are used for verification in [47] and [48], respectively. The proposed QRS detection topology is verified with a comparatively smaller input amplitude of 200 mV_{pp}. Moreover, Gungor et al. [48] mentioned that the detection performance of a QRS detection circuit is expected to depend on the amplitude of the ECG input and condoned the slightly lower Se(%) and +P(%) performance of the proposed work.
4) In [48], the QRS features are detected by using a constant threshold value of 100 mV, whereas the proposed topology uses adaptive thresholding for the same purpose. Moreover, Gungor et al. [48] mentioned that adaptive thresholding would improve the average sensitivity of QRS detection.

Finally, it is important to note the following points regarding the scheme discussed in this article: 1) as in [27], the QRS detecting circuit here assumes that P/T-wave excursion is significantly lower than the R-peaks. Any P/T-wave with an amplitude greater than the threshold voltage would be identified as an R-peak and 2) nonetheless, as already mentioned in Section I, it is essential to reiterate here that this work focuses on including useful functionalities in the front end with minimal hardware overhead and is intended for preliminary prognosis. Hence, only three out of the five alarm types discussed in [19] are targeted here.

V. CONCLUSION

A low-complexity low-power fully analog classifier for the detection of fatal ECG abnormalities is implemented.

Experimental results based on the test cases taken from the MITDB and [19] show that both the autonomous QRS detection circuit and the classifier modules exhibit acceptable performance. The output waveforms show that the proposed scheme detects any event of the three target abnormalities successfully. This work aims to make important value additions to the standard ECG front ends such as [24] while incurring minimal additional power dissipation and hardware complexity. Hence, this classifier presents a good tradeoff between complexity, accuracy, and power consumption and will be more effective for long-span continuous ECG monitoring rather than DSP-based techniques. This classifier integrated with standard analog ECG acquisition systems would aid the preliminary prognosis of cardiac abnormalities, especially in remote monitoring scenarios. Moreover, since the proposed methodology is first of its kind, it can be considered a proof-of-concept, and the reader is free to extend the same to include the two alarm types (i.e., ventricular tachycardia and flutter/fibrillation) left out here. Furthermore, the system proposed here can be extended to include a module, which can provide a count of number of heartbeats within a period of 1 min (heart rate) and some critical statistical measures intended for R–R interval analysis (HRV), i.e., NN50 and pNN50, and at the same time are feasible to implement fully in analog domain [49].

Data Availability

This manuscript has no associated data.

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