High Voltage Gain DC-DC Non-Isolated Converter with Generalized Stages

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***Abstract*—In this paper, a non-isolated dc-dc converter is proposed to provide a high voltage gain with a low inductance requirement. The circuit can be generalized for multiple stages to realize the desired DC output voltage from a low DC voltage source. In the proposed topology, the capacitors and inductors are charged/magnetized in parallel and discharged/demagnetized in series during switched on and off period respectively to obtain a high step-up voltage gain. The proposed power circuit is suitable for many applications based on renewable energy and energy storage where the desired DC-link voltage requirement can be as high as 560V (three-phase inverter input), and input voltage can be as low as 48V (a string of four batteries or fuel cell). A detailed analysis of the steady-state operation of the power converter is provided in this paper to obtain the voltage gain of the converter. The circuit design is simulated in MATLAB Simulink to verify the results of the analysis of this converter. Further, the design guidelines are provided for the generalized form of the converter to achieve desired steady-state input-output gain.**

***Index Terms*—DC-DC converter, High gain, High step-up voltage gain, Super-lift circuit, Switched inductor technique, Voltage-lift circuit.**

I. INTRODUCTION

Electricity demand has increased multi-fold times in the last two decades and has created a massive impact on natural fuel reservoirs such as coal and petroleum gas. To circumvent this challenge, all the stakeholders have started focusing on renewable type energy sources such as wind, solar PV, fuel cell, biogas, etc. Technological advancement in the area of power electronics allows the feeding of power generated by renewable energy sources into the power grid or converts their characteristics into a form suitable to feed the load. Some of the challenges in conditioning the power generated by renewable energy sources are low terminal voltage, voltage variation, and high intermittency. The science community has delivered several solutions to overcome many of these problems and continued their efforts to increase the performance of the power conditioning units. DC-DC converter topologies employed to boost the terminal voltage of storage and sources to integrate with the front-end voltage source inverter are extensively exercised [1]. Many of them can provide voltage boosting more than the conventional boost converter [2]- [11].

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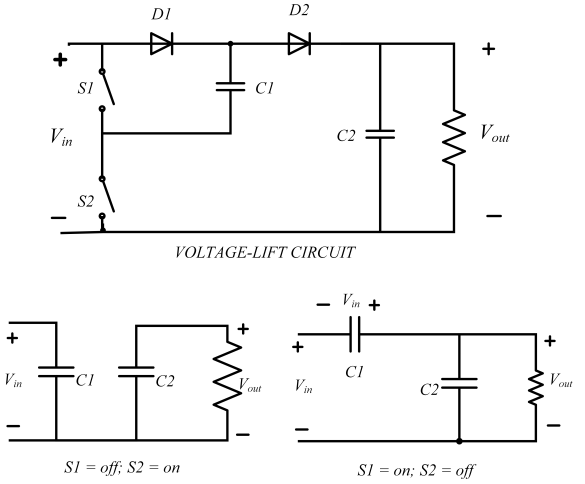
Further, DC-DC converters are in great demand to provide regulated supply to different appliances and devices which are voltage sensitive. Primarily, power conditioning units with high step-up ratios are widely used in renewable energy applications like photovoltaic systems, electric vehicles, UPS, and battery storage. Solar and wind turbine coupled generator produces highly intermittent power and its terminal voltage also varies with environmental conditions. Many power converters have been investigated in order to overcome the voltage variation problem which reciprocated to the load. The voltage produced by PV panels and fuel-cells is not large enough to meet the demands of high capacity power inverters, though PV string connections are popular to increase overall PV source voltage but with difficulties of partial shading and string bypassing problems [3]. Thus, high gain boost converters are implemented to produce the voltage suitable for such applications from small, variable voltages obtained from renewable sources.

The high step-up voltage gain can be established in different ways including a conventional boost converter at high duty-ratio [5]. But this has its own complication, the reverse recovery time of the diode which limits the range of duty-ratio feasible. In the case of isolated dc-dc converters, which are less efficient than non-isolated topology, are bulky and suffer high losses due to the transformer [2], [3], [12]. In order to overcome this problem, several dc-dc converters without transformers are designed to get a high voltage gain at normal duty-ratios. In [5] several non-isolated boost converter topologies like interleaved, cascaded, coupled inductor, and switched-capacitor based converters are reviewed which give higher gain than the conventional circuit. The basic quadratic boost converter is implemented in [13] by using L-switching blocks. A quadrupled dc-dc converter is designed in [6] to obtain high voltage gain and reduced voltage stress on the switches by using the input-parallel, output-series configuration. In [9] high gain is achieved through a super-lift converter, where an elementary circuit of inductors is used to increase gain in a geometric progression from one stage to the next one. Similarly in [8], the high step-up gain is obtained by cascading an elementary circuit made of capacitors known as voltage-lift circuits, but the gain here increases in an arithmetic progression between stages. In [10], the idea of both [8] and

[9] are brought together to design hybrid converters using both inductors and capacitors to get better gain. Traditional boost converter along with charge pumps is implemented in [11] to achieve a boost in output voltage. Using the switched inductor technique, high step-up voltage gain is attained in [7], it has also achieved further higher gains by connecting voltage lift circuits to it.

A non-isolated dc-dc converter is designed in this paper using the elementary circuit of [7] and techniques of voltage-lift (as shown in Fig. 1) [8] and super-lift circuit (as shown in Fig. 2) [9] to enhance the step-up voltage gain of the converter. The voltage-lift technique described in [8] uses the basic circuit shown in Fig. 1 where the capacitors are charged in parallel during the first half of the time period (S1=off, S2=on), and are discharged in series into the load during the second half (S1=on, S2=off) resulting in a higher overall voltage across the load.

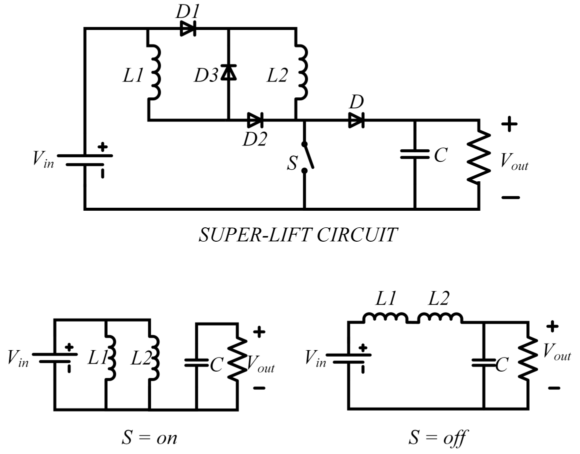


VOLTAGE-LIFT CIRCUIT

S1 = off; S2 = on

S1 = on; S2 = off

Fig. 1. Voltage lift circuit [8]



SUPER-LIFT CIRCUIT

S = on

S = off

Fig. 2. Super-lift circuit [9]

Similarly, in the super-lift circuit [9], inductors with the same inductances are charged in parallel to the source during the switched-on period of the switches and get discharged in series to each other and load during the switched-off period.

The proposed converter uses the switching inductor technique where many inductors are charged in parallel to each other during switch-on period and discharge in series during the off period which is similar to the super-lift circuit. The capacitors are charged and discharged through the voltage-lift technique. As the converter implements both switched-inductor and voltage-lift technique to boost the voltage, the value of inductance requirement in the proposed topology is relatively low compared to other topologies [9].

In the following sections, the proposed converter is described in detail and different modes of the circuit are analyzed, the circuit is generalized for higher voltage gains and the simulation results of the proposed circuit are given verifying the analysis and for further understanding of the circuit operation.

II. CIRCUIT DESCRIPTION

The converter proposed in this paper consists of four MOSFETs: S1, S2, S3, S4, and four identical inductors: L1, L2, L3, L4 as shown in Fig. 3. Further, it contains four voltage lift circuits one across each inductor. The circuit also consists of a diode, an output capacitor, and a load resistor. A single gate pulse controls all the four switches and they turn on and off simultaneously. Galvanic isolations are provided between gate triggering of different MOSFETs.

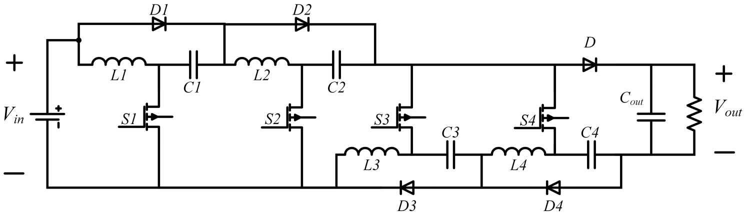


Fig. 3. Proposed High Voltage Gain Power Converter

This paper analyses the circuit while operating in the continuous conduction mode (CCM) only. Typical waveforms of certain voltage and current parameters while operating in CCM are shown in the following Fig. 4.

In continuous conduction operating mode there are only two modes of operation: one while switches are in On condition and the other is switches are in Off condition.

A. Switch On Condition:

The high state of the gate pulse provided to switches (S1, S2, S3, and S4) turns them on and conducts during the time interval (0, t_1). During this interval, the current paths are shown in Fig. 5(a) and the equivalent circuit of the converter is as shown in Fig. 5(b). All the inductors are connected in parallel to the source and store energy. Similarly, the capacitors get charged to the voltage same as that of the source which is the case of switched-capacitor [8]. The path resistance Req is to equivalent on-state resistance of the MOSFET and series resistance of the capacitor. The output capacitor releases the energy stored in it to the load resistor during this interval.

The voltage across the storage of different elements is as follows:

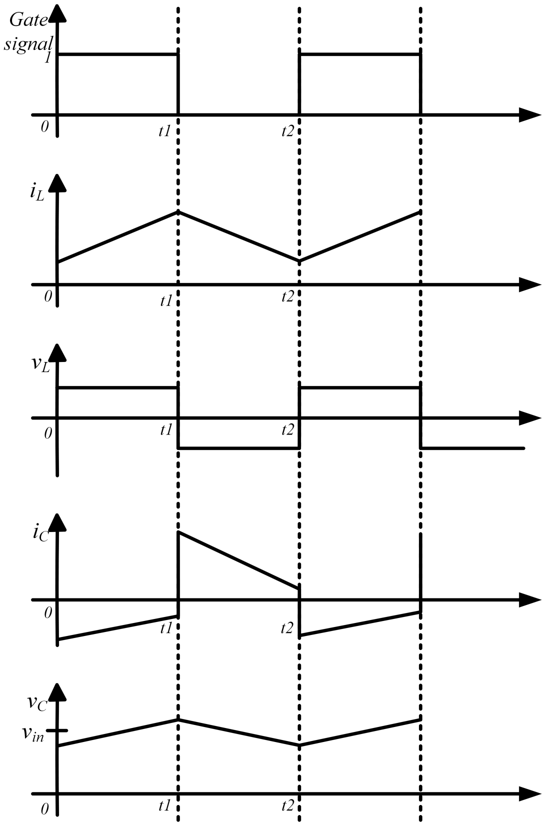


Fig. 4. Graphs depicting the current and voltage behavior in capacitor and voltages.

$$V_{L1}=V_{L2}=V_{L3}=V_{L4}=V_{C1}=V_{C2}=V_{C3}=V_{C4}=V_{IN} \quad (1)$$

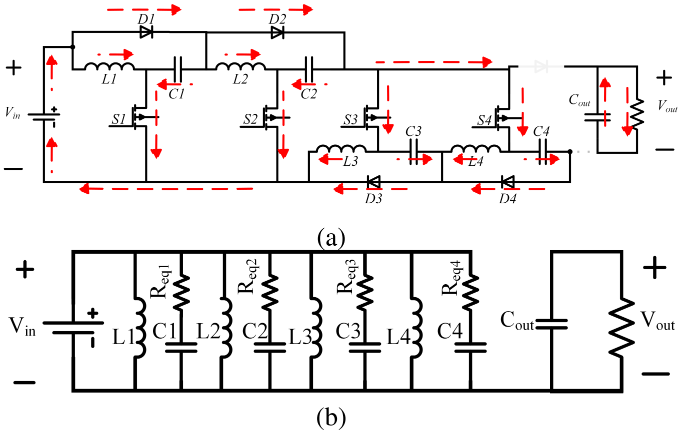


Fig. 5. (a) Switch On-state of the proposed topology (b)Equivalent circuit (Switched on)

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B. Switch Off Condition:

During the time interval (t_1, t_2) all the switches are turned off. The current paths are shown in Fig. 6(a) and the equivalent circuit of the converter is as shown in Fig. 6(b). All the inductors, capacitors and the source are connected in series with one another to release energy into the output capacitor and the load resistor.

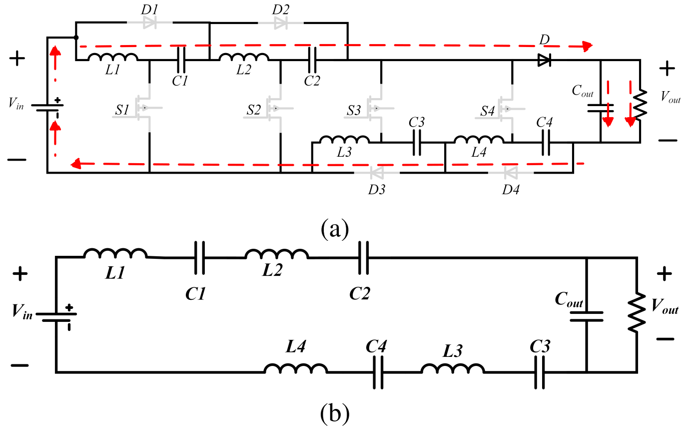

Fig. 6. (a) Switch Off-state of the proposed topology (b) Equivalent circuit (switched off)

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The voltage across the inductors during this period of the cycle is given by:

$$V_{L1}=V_{L2}=V_{L3}=V_{L4}=\frac{\left[\sum_{n=1}^{4}V_{Cn}+V_{IN}\right]-V_{OUT}}{4} \quad (2)$$

$$V_{L1}=\frac{5*V_{IN}-V_{OUT}}{4} \quad (3)$$

Using the volt-second balance technique across the inductor over a complete cycle and using equations (1) and (3), under steady-state condition, the following relation can be established:

$$\int_{0}^{DT_s}V_{L1}+\int_{DT_s}^{T_s}\frac{5*V_{IN}-V_{OUT}}{4}=0 \quad (4)$$

Solving the above equation, the gain of the power circuit can be obtained as follows:

$$Gain=\frac{V_{OUT}}{V_{IN}}=\frac{5-D}{1-D} \quad (5)$$

The gain obtained by this converter, along with some other high step-up voltage gain topologies is given in the following table.

It is observed that of the above mentioned high gain converter topologies, the proposed converter provides higher step-up gain at nominal duty ratios and utilizes comparatively smaller energy storage elements like inductors to achieve the same, which is seen in the following sections. The gain of the converter can also be increased further by generalizing the circuit which is explained in detail in the next section.

TABLE I

COMPARISON OF CONVERTER TOPOLOGIES IN TERMS OF GAIN

Converter Topology	**Gain**
Hybrid step-up converter [13]	$\frac{1+D}{1-D}$
Switched inductor high gain converter [7]	$\frac{3-D}{1-D}$
Switched-capacitor active network converter [14]	$\frac{3+D}{1-D}$
Quadrapler DC converter [6]	$\frac{4}{1-D}$
Proposed Converter	$\frac{5-D}{1-D}$

III. GENERALIZED CIRCUIT

Generalization of a circuit provides the flexibility to use the same converter topology for numerous applications that have variable voltage demands and applicable to a wide range of loads. The proposed circuit can be generalized to a series of converters where the gain of every higher stage increases in an arithmetic progression on the addition of certain blocks to the proposed circuit.

The generalized circuit of the converter topology and the additional blocks needed to increase gain are given in Fig. 7(a) and Fig. 7(b). The generalized circuit can be easily compared with the topology shown in Fig. 3 in the previous section where N=2. The necessary blocks to enable the proposed topology to modify for desired gain are T-switcher with MOSFET and diode as shown in Fig. 7(b).

The similar concept which described in the previous section can be used to determine the gain of the generalized circuit with N-stages as follows:

$$Gain = \frac{V_{OUT}}{V_{IN}} = \frac{(2*N+1)-D}{1-D} \tag{6}$$

Where N is the number of such blocks in the converter. To verify (6), the proposed converter shown in Fig. 3 has two such blocks, thus N=2 and,

$$Gain = \frac{V_{OUT}}{V_{IN}} = \frac{5-D}{1-D} \tag{7}$$

In a case with next higher stage, for N=3, the gain is

$$Gain = \frac{V_{OUT}}{V_{IN}} = \frac{7-D}{1-D} \tag{8}$$

IV. SIMULATION RESULTS

The proposed converter is simulated in MATLAB for a power level of 680 W. The input voltage applied to the converter is 48 V and the switches work at a frequency of 100 kHz for a duty ratio of 50%. The specifications of the converter implemented in this case study are given in Table II.

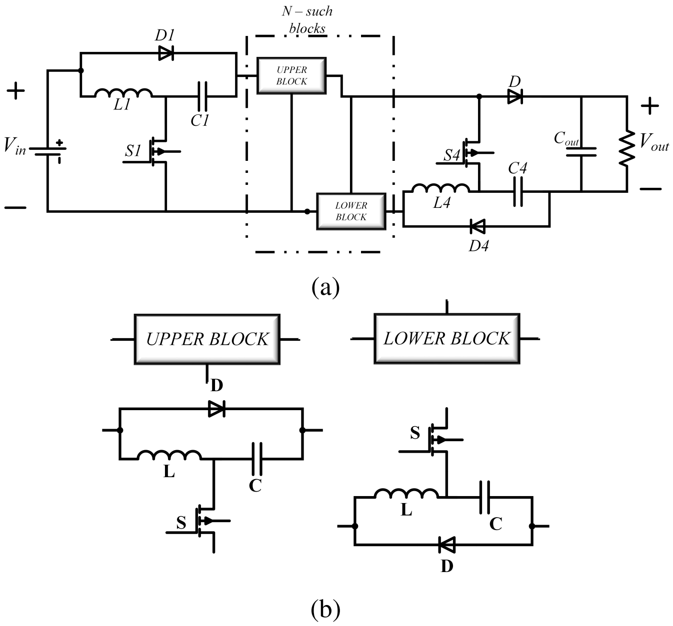

Fig. 7. (a) Generalized circuit diagram (b)Additional blocks to attain higher gains

TABLE II

CIRCUIT PARAMETER UNDER STEADY STATE

Circuit Specifications		
Parameter	**Value**	**Units**
Inductance (L1, L2, L3, L4)	300	μH
Capacitance (C1, C2, C3, C4)	40	μF
Output Capacitor	200	μF
Switching Frequency	100	kHz
Power Level	680	W
Output Voltage (calculated)	432	V
Output Voltage (obtained)	412	V

The diodes and switches used in the simulation are non-ideal with finite voltage drop and on state resistance during On condition. The corresponding difference is observed in calculated and obtained values of the output voltage. The current through the inductors is represented in Fig. 8. It also represents the inductor ripple current of 20% across a mean value of 3.8 Amp. The voltage across the inductors is shown in Fig. 9, which shows inductor is experiencing +48 and -48V during alternate periods of a cycle when it gets magnetized and demagnetized respectively.

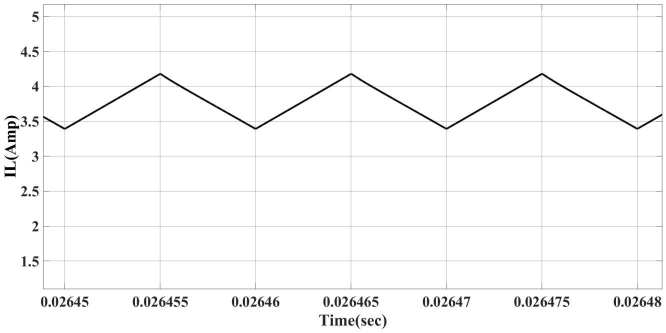

Fig. 8. Inductor current

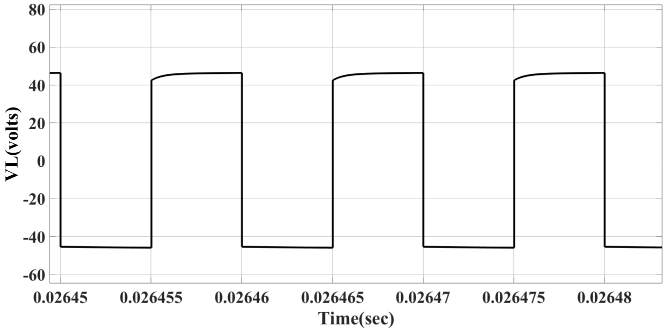

Fig. 9. Inductor voltage

The capacitor allows the ripple part of the current to pass through it as shown in Fig. 10 and gets charged to a voltage equal to the charging input voltage and varies over it during the switching cycle. The capacitor voltage variation is shown in Fig. 11.

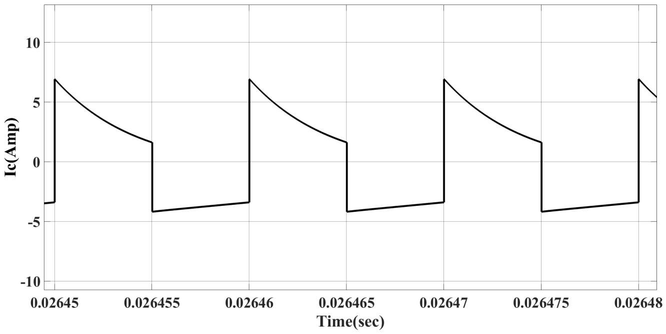

Fig. 10. Capacitor current

For a power rating of 680 W, the output voltage gets settled at a voltage level of 412 V due to drops in diodes and MOSFETs and an output current of 1.65 A is obtained as shown in Fig. 12 and Fig. 13 respectively.

To verify the voltage gain to duty ratio relation, the converter is simulated for various duty cycles. Fig. 14 represents the output voltage obtained for the circuit operating at duty cycles 0.4, 0.5 and 0.6. Further, the converter characteristic is plotted for duty to output voltage relation as shown in Fig. 15.

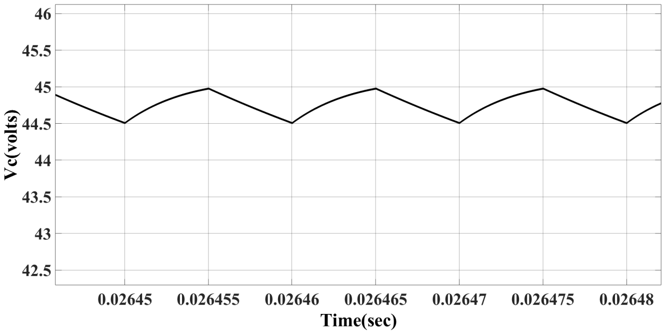

Fig. 11. Capacitor current

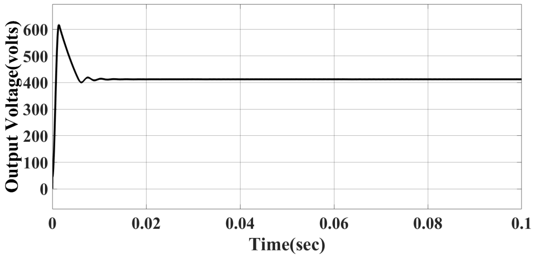

Fig. 12. Output voltage

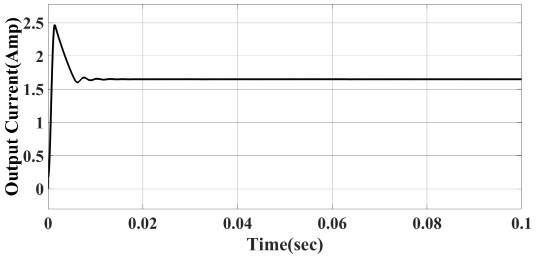

Fig. 13. Output current

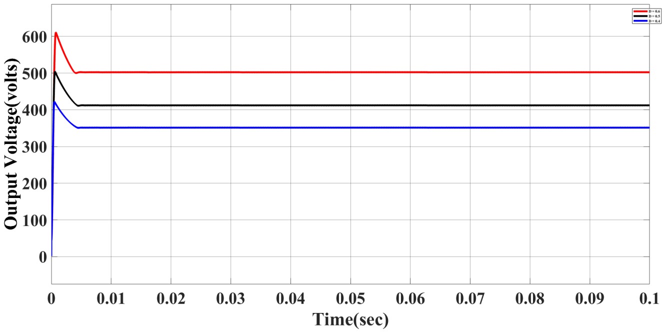

Fig. 14. Output voltage obtained for certain duty ratios

V. CONCLUSIONS

This paper has discussed a non-isolated dc-dc boost converter which has a very high step-up voltage gain than its conventional counterparts. It is implemented using the technique of voltage-lift circuits and super-lift circuits. Even though there are many switches and energy storage elements used in this topology the circuit is less bulky as the MOSFETs are

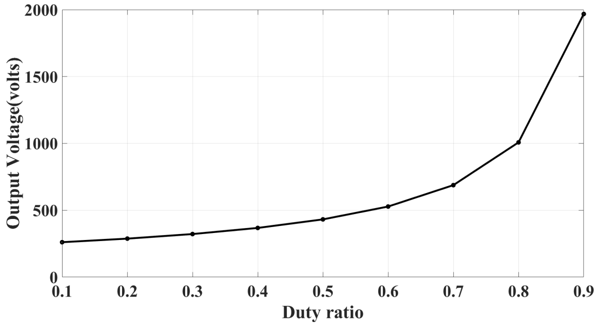

Fig. 15. Output Voltage for different duty cycles

considerably small and less expensive. The detailed analysis of the circuit is performed for its different working modes to derive a relation for the gain of the circuit. The topology is also generalized to provide higher voltage gains, which will be used for numerous applications. The proposed circuit is also simulated in MATLAB to verify the results of the mathematical analysis. The switched capacitor concept used in the proposed converter required to charge the capacitor in parallel to the source and imposed challenges in the large capacity systems due to pulse current demand of the device. Nevertheless, the proposed converter shows promising applications with its large step-up ratio for few to hundreds of watt systems.

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